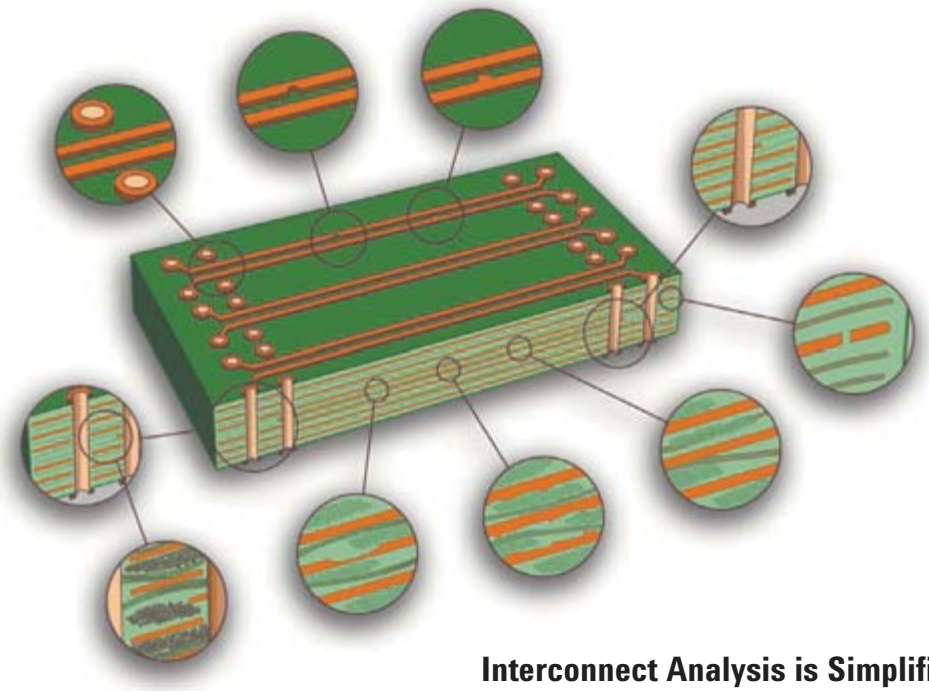
Agilent
Signal Integrity Analysis Series

Part 2: 4-Port TDR/VNA/PLTS

Application Note



Interconnect Analysis is Simplified with Physical Layer Test Tools

Agilent Technologies

Introduction

The Vector Network Analyzer (VNA) has come a long way since it was used to test antenna arrays for military applications. Vector Network Analysis can be used to perform more than 100 critical characterization, modeling, and emulation applications for high-speed, digital design, many of which are illustrated in this application note series.

If your application requires the measurement of very low level signals such as near end and far end crosstalk, using a test system with high dynamic range becomes very important. Unlike a wide bandwidth TDR, a VNA allows the user to set a narrow receiver bandwidth (known as Intermediate Frequency Bandwidth or IF bandwidth). This highly accurate tool provides a window into the performance of high speed digital interconnects which propagate signals with rise times of 500 ps or shorter. The VNA will expand the design validation capability of all signal integrity laboratories around the world and answer important questions such as: what is the limitation of my current design, where do I need to focus my attention to increase my data rate, and will my interconnect survive the next generation application?

The VNA is no longer limited to microwave applications traditionally utilized for aerospace and defense work. Today's commercial electronic designs push the limit of what can be achieved on copper and the power of s-parameters are critical to assure proper performance of these components and systems. Interconnect analysis using a VNA is now simplified with a popular software application called Physical Layer Test System (PLTS). Utilizing a graphical user interface designed for digital designers enables the power of the VNA with the ease-of-use of a TDR. The ultimate in test accuracy can be provided for topology models, S parameter behavioral models, characterization of rise time degradation, interconnect bandwidth, near and far end cross talk, odd mode, even mode, differential and common impedance, mode conversion, and the complete differential channel characterization.

To provide a little order to the wide variety of applications we explore in this application note series, we divided the series into three parts: Part 1: Those which use a single-port TDR, those which use TDR/TDT, and those which use 2-port TDR. Part 2: Those which use 4-port TDR. Part 3:Those which use advanced signal integrity measurements and calibration. The principles of TDR, VNA, and PLTS operation are detailed in other application notes and references listed in the bibliography. We concentrate this application note series on the valuable information we can quickly obtain with simple techniques that can be used to help us get the design right the first time.

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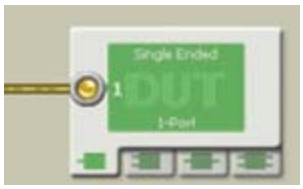
1.0 4-Port Techniques

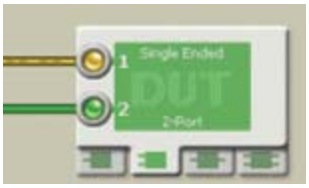
1.1 Complete differential pair characterization

How a TDR can provide valuable signal integrity characterization information about interconnects was reviewed in Part 1. Figure 1 summarizes the various applications for 1-port and 2-port TDR configurations. Though we are able to obtain some information about a differential pair from two port measurements, the complete characterization of a differential pair requires four ports.



Applications: single ended transmission line characteristic impedance, time delay and discontinuity characterization

Applications: single ended transmission line insertion loss, return loss, and materials characterization



Applications: cross talk between two single ended transmission lines, ground bounce, differential and common impedance characterization

Figure 1. TDR configurations and applications.

In a 4-port configuration, each of the instrument's ports is connected to each end of the transmission lines in the differential pair. In practice, it is a coaxial connection made at each end of each transmission line, so that each port has a signal and return connection to the transmission line.

Application: complete characterization of differential pair: differential return loss, differential insertion loss, common return loss, common insertion loss, mode conversion

Figure 2. Differential pair characterization.

In the configuration shown in Figure 2, everything important about a differential pair can be extracted. This includes the differential and common return and insertion loss and all forms of mode conversion. From these measurements, details of the differential or common impedance profiles, material properties, and asymmetries can be extracted.

A 4-port measurement can be performed in the time domain, using a 4-port TDR or in the frequency domain, using a 4-port VNA. To first order, there is exactly the same information content in both measurements. There are differences in the dynamic range, or the noise floor of the measurement, so if higher accuracy measurements are required, you should utilize a Vector Network Analyzer (VNA).

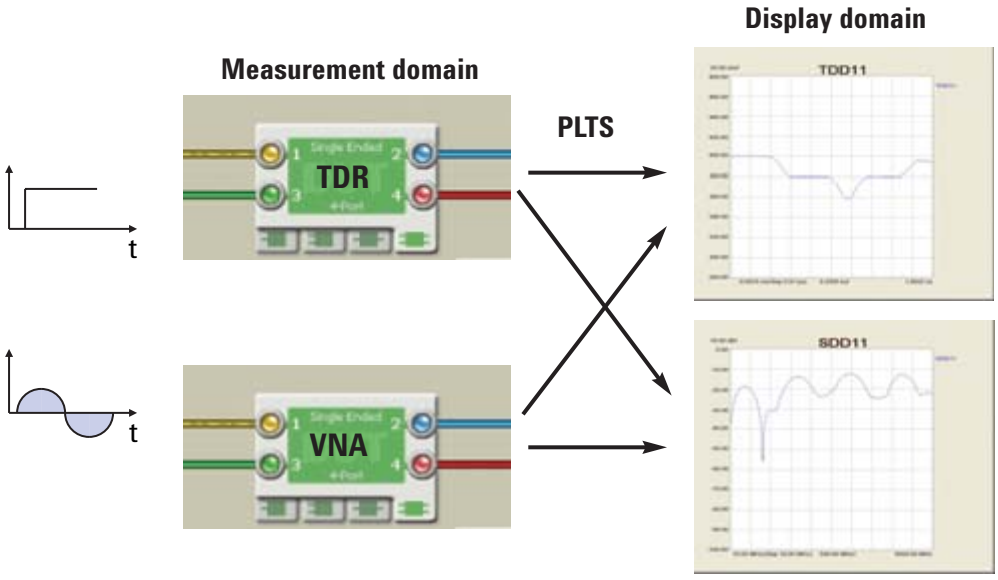


Figure 3. Time and frequency domains.

As illustrated in Figure 3, we can take the measured data from either domain and, using Agilent's N1930 Physical Layer Test System (PLTS), translate it mathematically using Fourier transform techniques, to display the same data in both the time or the frequency domain. These two domains tell the same story. They just emphasize different parts of the story. With PLTS, the display and analysis of the information is completely independent of the instrument used to collect the data. What is important is the information we extract. The flexibility of moving back and forth between the time and frequency domains gives us the flexibility of extracting the most information, as quickly and easily as possible.

The proliferation of high speed serial links has driven the wide spread use of differential pairs. A differential pair is nothing more than two, single ended transmission lines, with some coupling, used together to carry a differential signal from a transmitter to a receiver. Every single backplane produced today, and in the foreseeable future, is composed of multiple channels of differential pairs.

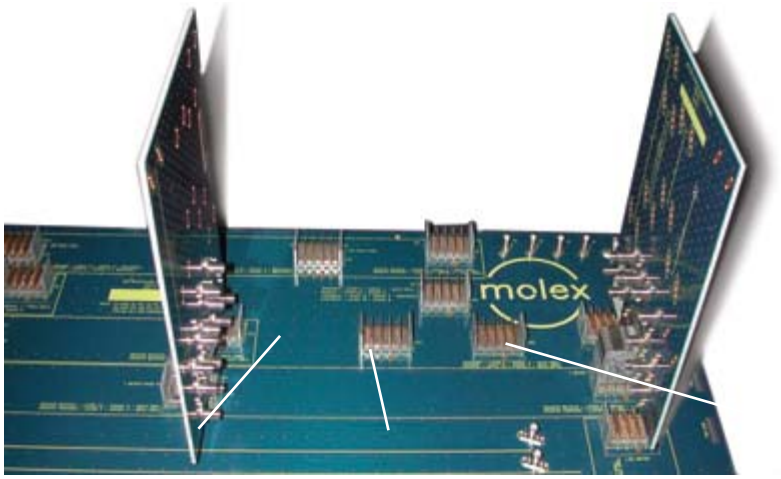


Figure 4. Typical small backplane.

Figure 4 shows an example of a section of a 46 layer backplane, 18 inches wide by 48 inches long, designed to test out many differential pair cross sections and via designs. This backplane, designed with Molex GBX connectors, is similar to many state of the art backplanes in use. All the important properties of differential pairs in backplanes such as these, can be measured with four ports and analyzed with PLTS.

1.2 4-Port single-ended S parameters

There are two commonly used types of 4-port S parameters; single ended and differential. The 4-port single-ended S parameters are an extension of one and 2-port S parameters. In a differential pair, which is really an example of a 4-port device, we conventionally label the ends of the device as shown in Figure 5, with port 1 connected through to port 2 and port 3 connected through to port 4. This is also shown schematically.

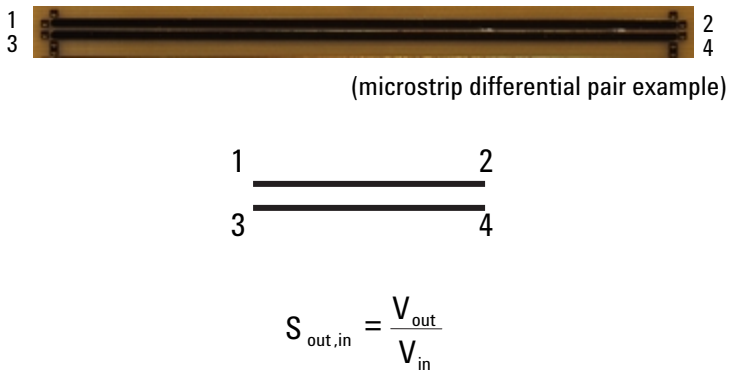


Figure 5. 4-Port, single-ended S parameters definition.

By definition, each S parameter is the ratio of the voltage wave coming out of some port to the voltage wave that was going in. For example, S21 is the ratio of the wave coming out from port 2 to the wave going in at port 1. This is also called the insertion loss. S31 is the ratio of the wave coming out of port 3 to the wave going in at port 1. This is a measure of the near end cross talk. As the ratio of two sine waves, each S parameter is complex with a magnitude and a phase.

The 4-port, single-ended S parameters have become a defacto standard for describing the electrical properties of any 4-port interconnect. There are 16 different possible combinations of waves going in and waves coming out. Conventionally, these 16 terms are described in a matrix representation. The S parameter formalism is not complicated. It is just confusing and somewhat anti-intuitive.

We would expect that the order of the indices that define each term would have the first index being the going in port and the second index the coming out port. For mathematical reasons, the definition is the exact opposite. The first index is the coming out port while the second index is the going in port. The first index of each element, the rows, represent the response sources- where the wave is coming out. The second index, the columns, is the stimulus, where the wave is going in. Figure 6 shows an example of a generic, 4-port S parameter matrix, which includes all 16 elements.

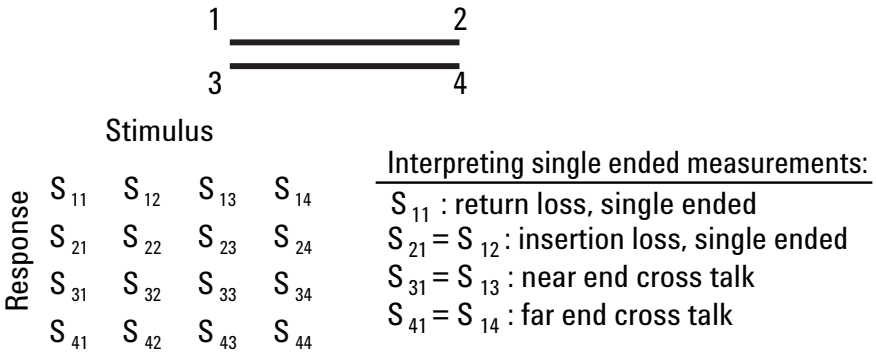


Figure 6. 4-Port single-ended S parameter matrix.

When the interconnect is two transmission lines, each element has special meaning. The diagonal elements are the return loss or reflection coefficients. S11 is the return loss of one line from the left end, while S22 is the return loss for the same line from the right end. Since all ends of the device are terminated into the measuring instrument, they are all effectively terminated into 50 ohms.

The S21 and S43 terms are the insertion loss of each line. This is the ratio of what gets transmitted through the transmission line from one end to the other. S31 is the near end noise and S41 is the far end noise.

Though there is no industry standard for labeling the ends of the lines, there is a commonly adopted practice. When we describe the interconnect as two separate single-ended lines, it is conventional to use the labeling as shown in Figure 6. A signal travels from port 1 to port 2 and from port 3 to port 4. In this way S21 is the transmitted signal coming out of port 2 from port 1. As long as we always use this format, S21 will always refer to a transmitted signal and S31 will be the near end cross talk term.

1.3 S parameters in the time domain

In the complete matrix of measured 4-port S parameters, there is a lot of data. Figure 7 shows an example of the measured single-ended S parameters of two traces in a small backplane. There are 16 elements, each with magnitude and phase information, for each frequency value. Not shown in any individual plot is the phase information for each element.

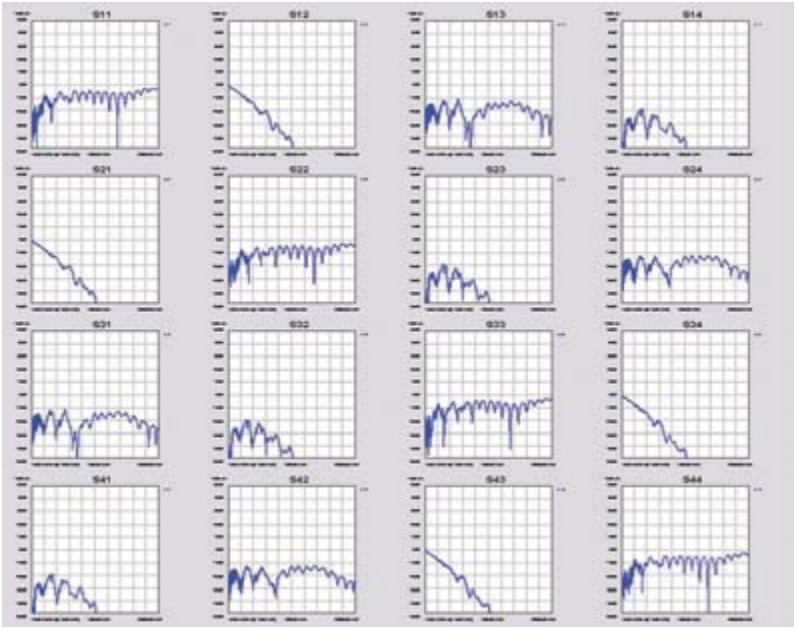


Figure 7. Measured, complete, 4-port single-ended S parameter matrix

Keeping track of all the information can be a difficult task without a tool such as PLTS. This tool will allow us to collect the data from the instrument and display each or all of the elements in precisely the format that will get us to the answer quickly. In this example, we could read the insertion loss of the interconnect at any frequency from the S21 and S43 terms and the near end noise from the S31 and S42 terms.

The same information contained in the frequency domain S parameters can be transformed into the time domain form of the S parameters. The frequency data in each element can be converted into the time domain response of the same element. A return loss becomes a reflected signal. An insertion loss becomes a transmitted signal.

By convention, when the S parameters are displayed in the frequency domain, they are called S parameters, but when displayed in the time domain, they are referred to as T parameters. S11 in the frequency domain becomes T11 in the time domain.

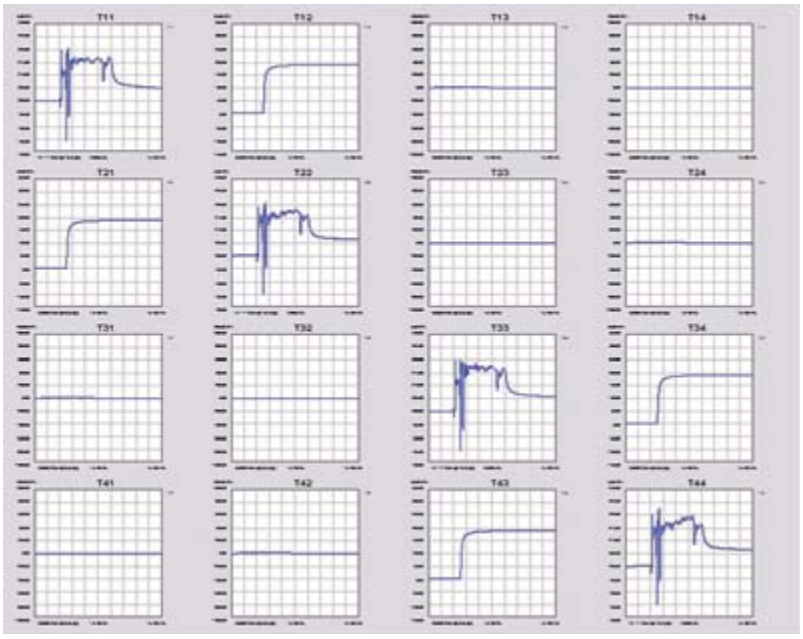


Figure 8. Time domain S parameters

With the 16 single-ended T parameters displayed in a matrix, as shown in Figure 8, many of the important performance questions can be answered at a glance.

In its simplest form, T11, when displayed as the step response with a 200 mV incident voltage applied, is identical to the TDR response we are used to seeing on the front screen of a TDR instrument. Figure 9 shows an example of the T11 step response for one trace in a short backplane, on a time base of 1 ns/div, with 10 mV/div on the vertical scale. While the general features can be seen, it is difficult to quantify the impedance profile on this scale.

Figure 9. T11 as reflected voltage and impedance profile.

However, the reflected voltage can be converted into a reflection coefficient, and from this, the first order impedance profile can be directly displayed so that the general features of the interconnect can be extracted right from the screen. In the example shown in Figure 9, the scale is 5 ohms per division. We can see the impedance of the daughter card trace is about 55 ohms, while the single-ended impedance of the backplane trace is about 58 ohms.

Everything we ever wanted to know about the behavior of these two single-ended lines can be found in one form or another in the S parameter matrix or the T parameter matrix.

1.4 4-Port differential S parameters

As demonstrated in Figure 10, two individual transmission lines with coupling are also, at the same time, a single, differential pair. As two single ended transmission lines, we described their electrical properties in terms of their single ended characteristic impedance and time delay and their near and far end cross talk.

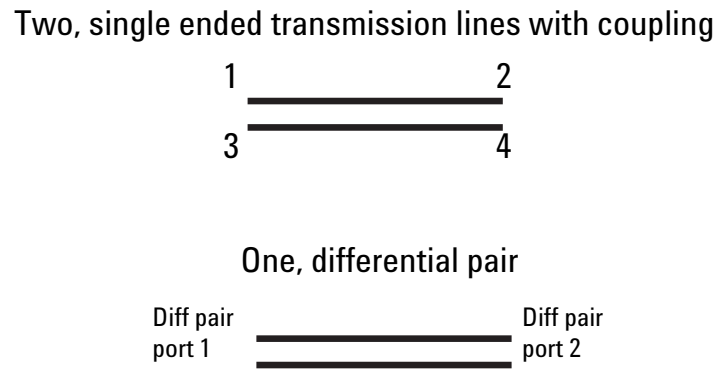


Figure 10. Two equivalent views.

As a differential pair, we are interested in how differential and common signals interact with the pair. When we look at these same two lines as a single, differential pair, we describe the differential pair in terms of a differential impedance, a common impedance, and a differential or common time delay. Since we are describing the exact same interconnects, these two views must be exactly equivalent. For linear, passive devices, which includes all interconnects except ferrites, the single-ended S parameters can be mathematically transformed into differential S parameters.

When describing a single differential pair, the stimulus and response can only be a differential signal or a common signal. There are four possible outcomes. A differential signal enters the differential pair and a differential signal comes out, a differential signal enters and a common signal comes out, a common signal enters and a common signal comes out or a common signal enters and a differential signal comes out.

			Stimulus			
			Differential signal		Common signal	
			port 1	port 2	port 1	port 2
Response	Differential signal	port 1	SDD11	SDD12	SDC11	SDC12
		port 2	SDD21	SDD22	SDC21	SDC22
	Common signal	port 1	SCD11	SCD12	SCC11	SCC12
		port 2	SCD21	SCD22	SCC21	SCC22

Figure 11. Differential S parameters

Each of these four outcomes is partitioned into a different quadrant of the differential S parameter matrix, as shown in Figure 11. To distinguish these quadrants, we use the same index format as the single ended S parameters, using a D or C to designate differential or common, stimulus or response. The first index is the coming out index, while the second index is the going in index.

The SDD quadrant describes differential signals going in and coming out, the SCC quadrant describes common signals going in and coming out. The SCD quadrant in the lower left corner of the matrix describes differential signals going in and common signals coming out, a form of mode conversion, and the SDC quadrant, in the upper right, describes common signals going in and differential signals coming out, a form of mode conversion.

Everything you ever wanted to know about the electrical properties of a differential pair is contained in these 16 differential S parameter matrix elements. They are also sometimes called the balanced or mixed mode S parameters. These are all different names for exactly the same set of terms.

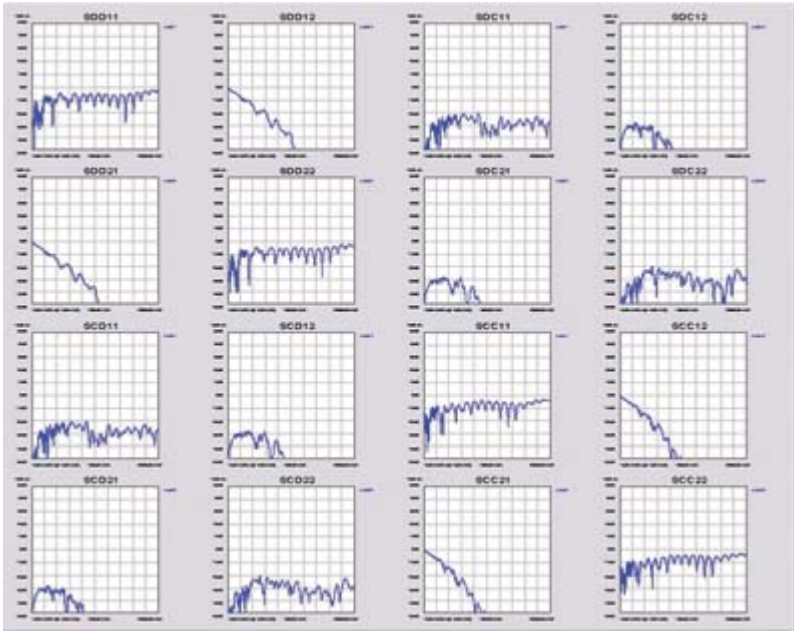


Figure 12. Balanced or differential S parameters.

When all 16 elements are displayed as in Figure 12, it is conventional to display them in the same orientation as the matrix elements previously described. The four elements that make up the upper left quadrant are the SDD terms, the four on the lower left are the SCC terms, the four in the upper right are the SDC terms, relating mode conversion, and the lower left quadrant are the SCD terms.

Since these are S parameters, in addition to having a magnitude for each S parameter plotted as a function of frequency, we also have the phase of each term. For compactness, the phase terms are not displayed in this set of plots but are easily accessible, when needed.

Of course, just as we were able to convert the single ended S parameters into the equivalent time domain, T parameters, each of these differential S parameter elements can be converted mathematically into their equivalent time domain T parameters.

The resulting matrix is the balanced or differential T matrix. An example of the differential T matrix for a 16 inch differential pair through a motherboard, and two daughter cards, is shown in Figure 13. The diagonal elements are all reflection terms, and relate to the differential or common impedance profiles.

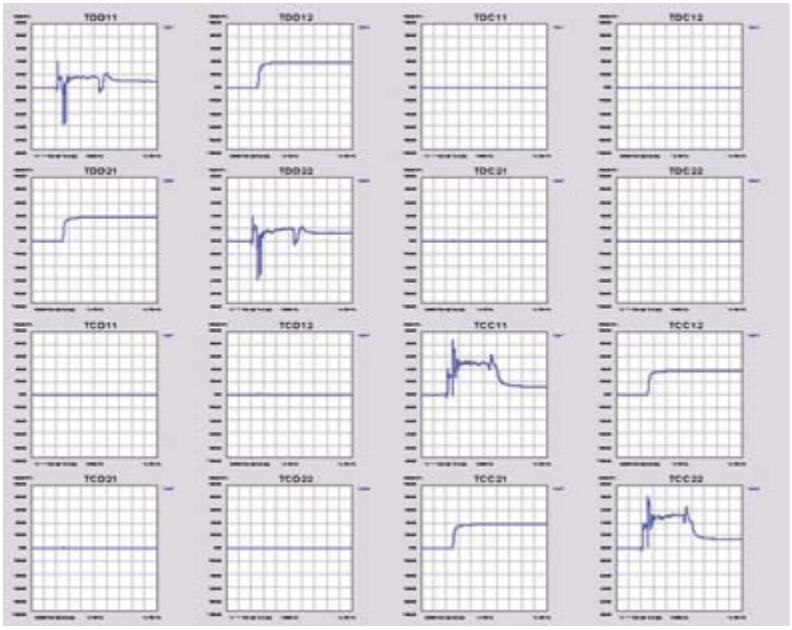


Figure 13. Balanced time domain matrix elements.

It is important to keep in mind that the various formats to display the S parameters are all completely interchangeable. As illustrated in Figure 14, the measurements can be taken in either the time domain with a TDR or in the frequency domain with a VNA and mathematically, using PLTS, converted equivalently into the four different formats and two special conditions, and displayed in the time or frequency domains, or as single ended or differential parameters.

Measurements: TDR, VNA	→	Displayed: PLTS
Time domain		Single ended frequency domain
Frequency domain		Single ended time domain
		Differential frequency domain
		Differential time domain
		Eye Diagram
		W-element RLCG

Figure 14. Summary of measurement and display options.

Depending on the question we are trying to answer, one format or a specific element might be more efficient at getting us to the answer faster. In this application note, we focus on those formats that can provide the most valuable information about differential channels used in high speed serial links.

1.5 High-speed serial links applications

The information provided by 4-port differential S parameters, either in the time domain or the frequency domain, is ideally suited to analyzing the performance of the differential channels used in high speed serial links. Figure 15 lists some of the most important problems that can be solved using the techniques outlined in this application note.

1. Characterizing the differential and common impedance profile of a differential channel
2. Characterizing the time delay and group delay of the differential and common signal in a differential channel
3. Measuring the bandwidth of a differential channel
4. Measuring the rise time degradation of a differential channel
5. Direct simulation of eye diagrams
6. Estimating taps for pre-emphasis from transmitted impulse response
7. Estimating possible EMI resulting from mode converted common signal on external cables.
8. Identifying the root cause of mode conversion in a differential pair
9. Extracting first order transmission line models of a differential pair in RLCG format

Figure 15. Some of the problems that can be solved using S and T parameter analysis.

In addition to just the general characterization of the interconnect, by using the information contained in the 4-port S and T parameters, the resulting performance of the differential channel can be emulated. Direct measurements of the interconnect bandwidth and expected eye diagram can be evaluated.

The rise time of a transmitted signal will be degraded due to loss in the interconnect from the dielectric and conductors, and from impedance discontinuities. By looking at the differential impedance profile, the discontinuities can be isolated and their root cause identified.

If the information displayed by PLTS can't answer every question directly, the behavioral model of the channel, described by the 16 element differential S parameter matrix can be used directly in some circuit simulators such as Agilent's ADS or the circuit simulator HSPICE. Using the actual device driver models and the behavioral model of the interconnect, the system performance can be evaluated. Likewise, if a circuit simulator is used that cannot input S parameter behavioral models, a simplified, uniform differential transmission line model can be exported based on RLGC matrix elements. This can be used by most circuit simulators.

The combination of features in PLTS is a powerful tool to extract the most possible information from any differential channel used for high speed serial interconnects.

1.6 Differential impedance profile

In this first application example, we will look at the differential impedance profile of a differential pair, using the differential time domain response. The first device under test is a uniform differential pair, 4 inches long, fabricated in FR4 as a microstrip, and shown in Figure 16. This particular pair was designed with very tight coupling, having a spacing about one half the line width. Data is courtesy of GigaTest Labs.

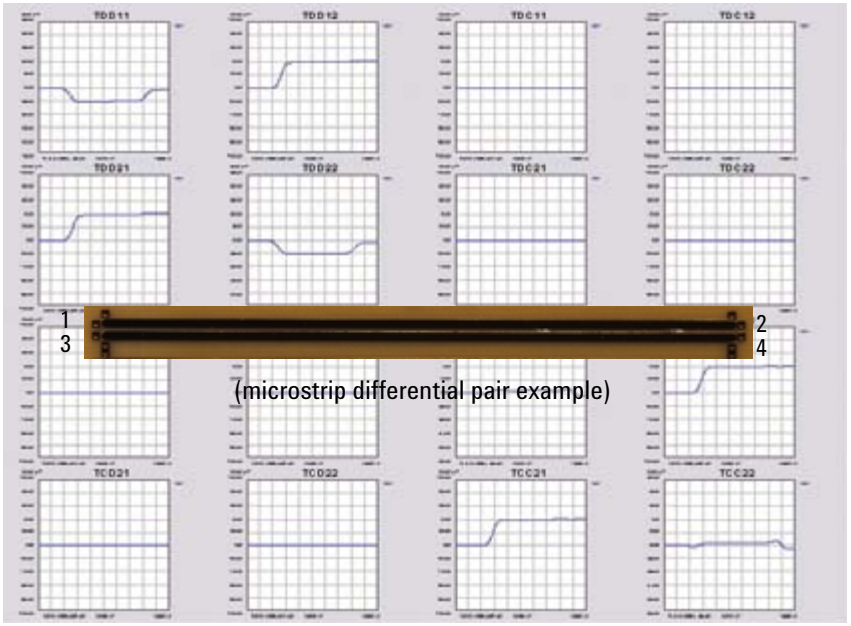


Figure 16. Differential time domain response for uniform tightly coupled differential pair.

All the balanced time domain measured data is displayed in Figure 16. All the information about how differential and common signals interact with this differential pair in the time domain, are contained in these 16 elements. The upper left quadrant has information about how differential signals enter and come out. The lower right quadrant has information about how common signals enter and come out. The two off diagonal quadrants have information about how differential signals or common signals enter the differential pair and are converted to the opposite type of signal and come out of the differential pair.

To describe the differential impedance profile, we would want to send a differential signal into port 1 and measure the reflected differential signal coming back out of port 1. The reflected signal would be due to encountering changes in the instantaneous differential impedance along the way. This information is found in the TDD11 matrix element, in the upper left quadrant.

The source impedance of each channel of a VNA or a TDR is 50 Ohms. However, when they are sourcing a differential signal, the source impedance is now the series combination of the two impedances, or 100 ohms. This means that any reflected signal is due to encountering a differential impedance other than 100 ohms.

The TDD11 term can be displayed with three different scales: as the reflected differential voltage, assuming a 400 mV incident differential signal, as the reflection coefficient, or as a first order calculation of the instantaneous impedance. In Figure 17 is an example of the measured TDD11 element, first as the reflected voltage on a scale of 20 mV/div out of 400 mV incident signal, or five percent reflection coefficient per division and then as the extracted impedance, on a scale of 10 Ohms/div.

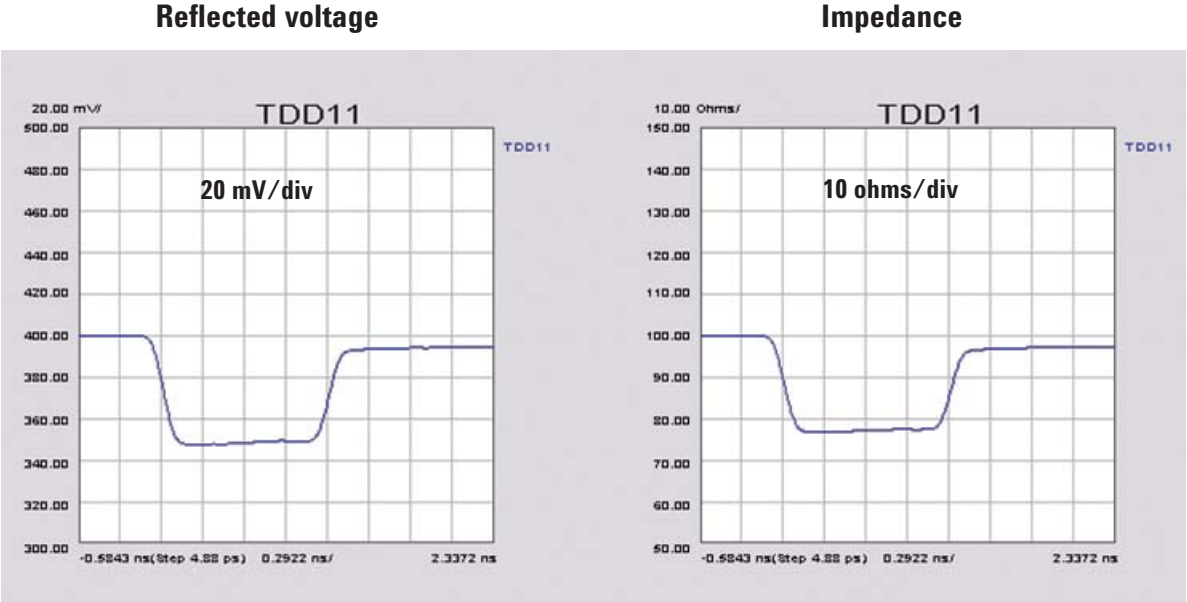


Figure 17. TDD11 of uniform pair.

The differential impedance profile of this interconnect can be read off the right impedance screen as about 77 ohms; very constant from the beginning to the end of the interconnect, as expected for a uniform differential pair.

The beginning of a 22 inch differential channel on a motherboard is shown in Figure 18. The impedance profile can be read directly off the screen with the aid of the markers.

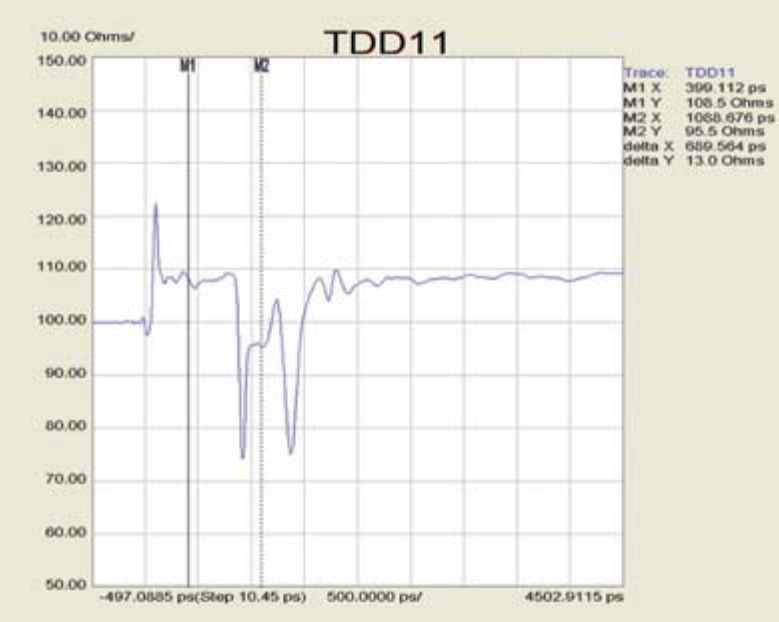


Figure 18. TDD11 of motherboard trace.

The very first peak is due to the inductance of the SMA launch. With too much antipad area around the signal pin, it has a higher impedance. The flat region, which marker M1 intersects, has an impedance read on the scale to the right of 108 ohms,. This is the trace on the daughter card which is relatively constant in impedance.

The first large dip, going as low as 75 ohms on this scale, is the capacitance of the via field where the connector attaches to the daughter card. The next dip is the capacitance of the via field where the connector attaches to the motherboard. The region between them, where marker M2 spans, shows an impedance of roughly 95 ohms. This is the region through the connector itself.

The rest of the trace, to the right of the last dip, is the trace on the motherboard, showing an impedance of roughly 108 ohms. This is the typical performance of a motherboard, which shows an impedance within 10 percent of the target impedance of 100 Ohms. The connector itself is a well matched connector. Its just that the vias the connector is inserted into have an excess capacitance which dramatically degrades the performance of the differential channel. It is not the component causing the problem, but how it has been designed into the board.

1.7 Impact from stimulus rise time

The same differential channel is shown in Figure 19 on an expanded scale of 1 ns per division, now showing the connector on the other end of the channel. However, the right end of the differential channel clearly does not match the left end. The impedance miss match is clearly larger on the left end. Is it possible the connector is different on each end and has a different impedance profile?

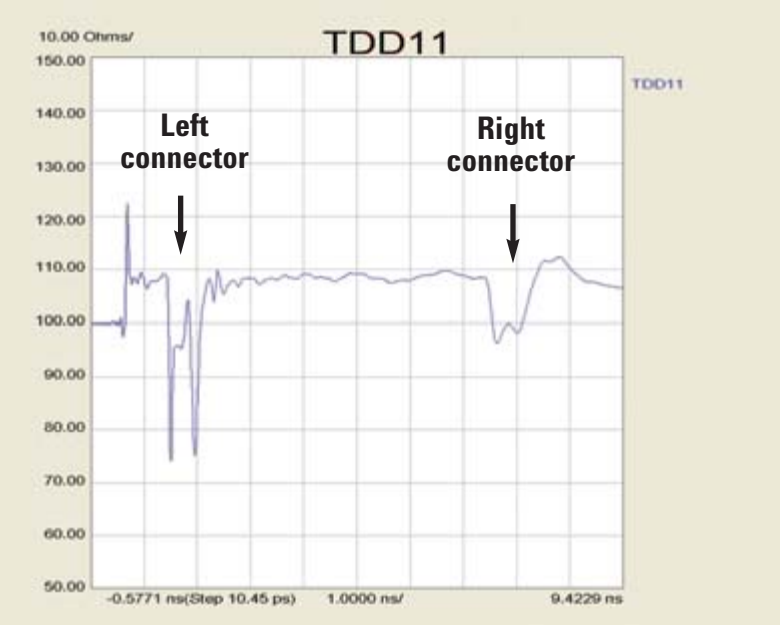


Figure 19. TDD11 of motherboard trace on expanded scale.

When the time delay of the impedance discontinuity is short compared to the effective rise time of the incident signal, the magnitude of the reflected signal will depend on the rise time. Referring to the peak value of the reflected signal on the impedance scale, and interpreting this as an impedance, is only meaningful if the rise time of the signal at that point is known. To interpret impedance, it is important to know the rise time of the system.

When the data is taken in the time domain with a TDR, the 10-90 rise time of the stimulus entering the device under test can often be read right from the screen of the TDR. When the data is taken in the frequency domain with a VNA and transformed to the time domain, it is not always obvious what the rise time of the signal is that is entering the device under test.

There is a simple way of estimating it, but it will depend on the setting under the Time Domain Window, as shown in Figure 20. There are three settings that affect the effective rise time of the signal. However, there is a trade off between shorter rise time and artificial ripple. This is a natural consequence of the digital filter that is part of the Fourier transform that translates the frequency domain data into the time domain.

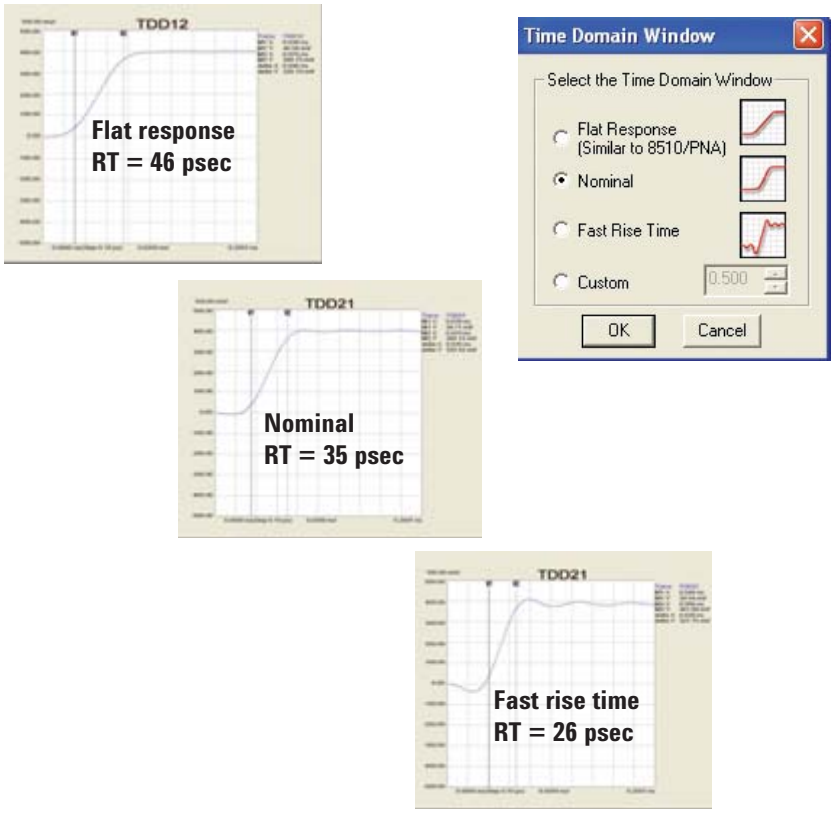


Figure 20. Time domain window.

In this example, a thru measurement was measured on a VNA with a frequency range up to 20 GHz. The 10-90 rise time of the received signal, TDD21, was measured using markers, on the screen. As a rough approximation, the 10-90 rise time for the "flat" setting is 46 ps. This corresponds to roughly RT = 0.9/BW. For the nominal setting, which is the default setting for PLTS, the RT = 0.7/BW and for the "fast rise time" setting, the RT = 0.54/BW.

While a rough approximation to the rise time of a signal, given the bandwidth of the signal is RT = 0.35/BW, the effective rise time is actually longer in PLTS because of the bandwidth overhead of the digital filter.

This approximation allows us to estimate the rise time entering the DUT if we know the highest frequency in the VNA measurement. Using a nominal setting, and a measurement bandwidth of 20 GHz, the rise time entering the DUT is 35 ps. Though this is the rise time entering the DUT, as the incident signal travels down the interconnect, the rise time quickly increases due to the impedance discontinuities and the losses in the channel. Past the first discontinuity, it is not possible to interpret the impedances with any meaning from the screen because the rise time at the location of the discontinuity is unknown. If a faster rise time than 35 ps is desired, then a VNA with higher bandwidth can be used in the measurement (i.e 50, 67, or 110 GHz).

One way to verify the connectors are identical on the two ends is to compare the TDD11 response with the TDD22 response. This is the differential TDR response, looking from the other end of the differential channel. In Figure 21, the TDD11 response and the TDD22 response are both displayed superimposed on the same scale of 1 ns per division.

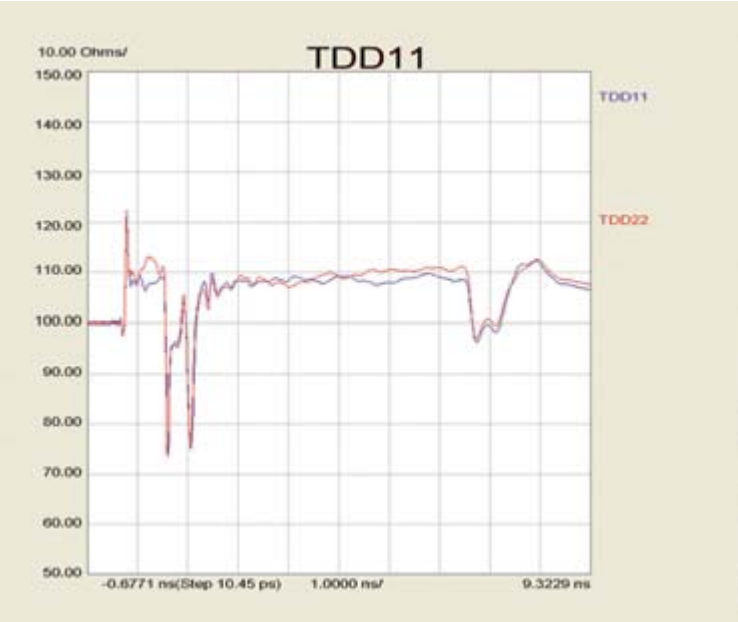


Figure 21. Differential TDR response of both ends of the interconnect.

We see that the TDD response for each daughter card and connector are almost identical when viewed from the closest end. The connector on the far end of the interconnect also appears identical. In this particular interconnect example, the interconnect is symmetrical. It can look like the connectors are different on the two ends because of the rise time degradation of the signal in propagating down the length of the interconnect, smearing out the reflected signal.

1.8 Differential or single-ended measurement

It is often believed that a single-ended measurement is good enough and the extra effort of a differential measurement is not necessary. By comparing the TDD11 response with the T11, single-ended response, we can do a direct comparison of the signal-ended and differential response. By definition, the differential impedance is twice the odd mode impedance. If there were no coupling between the two lines that make up the differential pair, the odd mode impedance of either line would be identical to the single-ended impedance of either line. How different the two impedances are, is a measure of the degree of coupling.

Figure 22 shows the same motherboard trace displayed as the differential response, TDD11, and the single-ended response, T11. The time base is identical in the two plots, and the impedance scale for the differential signal is 10 ohms/div while the single-ended response is on a 5 ohms/div scale.

Figure 22. Differential and single-ended impedance profiles.

The odd mode impedance of the daughter card is 108/2 = 54 ohms. The single-ended impedance of the daughter card is seen to be 56 ohms. This suggests that the two ohms lower impedance of the odd mode is due to the coupling on the daughter card.

The odd mode impedance of the connector is seen to be about 100/2 = 50 ohms, a well matched connector. The single-ended impedance of the same path is roughly 59 ohms. If we had used this single-ended measurement to evaluate the connector for differential applications, and incorrectly called this impedance the odd mode impedance, we would have estimated the differential impedance was 59 x 2 = 118 ohms. This large difference is an indication of the strong coupling in the connector.

Connectors used in differential applications are typically designed for tight coupling. To get a realistic measure of the differential impedance of a connector, it would be terribly misleading to use a single-ended measurement. The error in this case would have been about 18 percent.

The odd mode impedance of the trace on the motherboard is about 110/2 = 55 ohms. The single-ended impedance of the same trace on the motherboard is about 59 ohms. The four ohms reduction in the odd mode impedance suggests tight coupling of the traces on the motherboard interconnect. If the single-ended impedance were used to characterize the motherboard, there would be an error of about four ohms out of 55 or 7 percent. This is why differential impedance measurements are so important in coupled, differential pairs.

1.9 Common impedance profile

When the stimulus is a common signal, the two ports on each side of the device under test are in parallel and the effective source impedance is 25 ohms. The TCC11 response can be converted into the common impedance profile. It will be sensitive to impedance changes from the 25 ohm reference impedance.

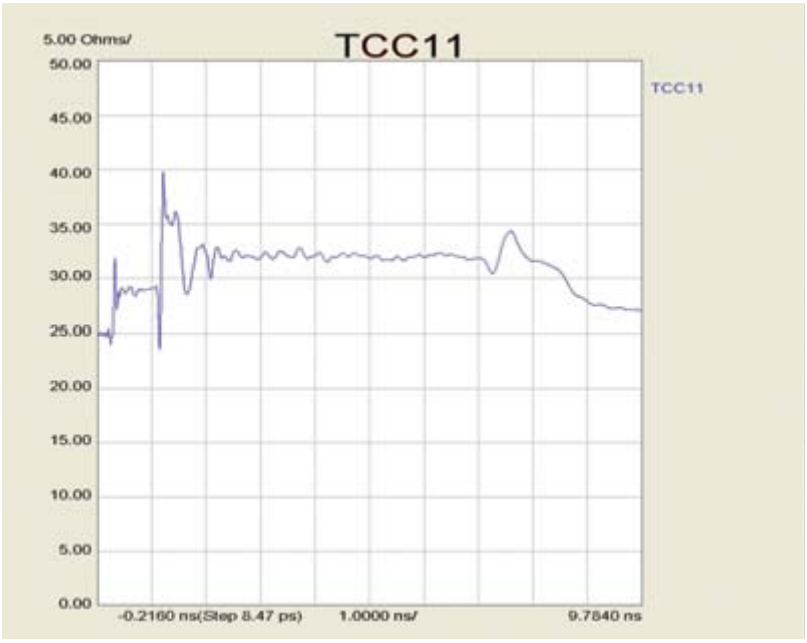


Figure 23. Common impedance profile.

Figure 23 shows the common impedance profile for the differential channel through the motherboard. The daughter card is roughly at 28 ohms, the connector at 35 ohms and the motherboard differential pair at 32 ohms. Though it is straightforward and easy to display the common impedance profile of a differential pair, rarely is it of any consequence.

1.10 Time delay and dispersion

Due to the finite speed of light, there is a time delay between the signal entering a differential channel and that same signal appearing at the far end. This is the second important parameter for a differential channel. To first order, the time delay is related to the length of the interconnect and the speed of light in the interconnect medium. And, to first order, the speed of the signal is due to the dielectric constant of the material. The time delay can be measured in both the frequency domain and the time domain, returning a slightly different piece of information in each domain.

In the frequency domain, the time delay is related to the phase delay of a sine wave entering the interconnect at the reference plane (determined by the calibration set up) and being received at the second differential port. The total phase delay is the number of "unwrapped" wave cycles through the interconnect. The phase delay divided by the frequency is the time it takes for that individual sine wave frequency to travel from one end to the other.

The derivative of this sine wave time delay is called the group delay. It is the time it takes for the shape of a combination of sine waves to travel down the interconnect. Group delay is the term that corresponds most closely to the time delay of a signal through the interconnect, and can be displayed directly by PLTS for any differential channel.

In an interconnect composed of a laminate material that is nondispersive, where the dielectric constant is constant with frequency, the derivative, or slope of the phase delay to the frequency, is exactly the same as the group delay. All frequency components travel at the same speed. To first order, group delay is constant at all frequencies for virtually all differential channels. If the interconnect has a constant impedance and is perfectly matched at the ends to the measuring instrument, the measured group delay is exactly related to the time delay of a signal entering the interconnect and appearing at the far end. It would be constant at all frequencies.

However, if there is any impedance mismatch at particular frequencies, resulting in reflections of the sine waves, the time delay for the reception of the phase at that frequency will be distorted. The measured, transmitted phase is no longer due to just the speed of light in the medium, it is also related to the multiple reflections.

In the frequency domain, the multiple reflections will give rise to variations in the group velocity. In the time domain, the multiple reflections will give rise to a distortion of the leading edge of the signal as it comes out of the interconnect. Some frequency components will arrive at different times compared to others.

In Figure 24 is an example of the measured group delay for a one meter long backplane differential channel, composed of two daughter cards and 28 inches of backplane trace. The vertical scale is 1 ns delay per division, and the horizontal scale is 2 GHz/div. We see the typical delay is about 6.7 ns for the 40 inches, which is 6 in/ns, exactly the same as the rough rule of thumb that the speed of a signal in an interconnect is 6 in/ns.

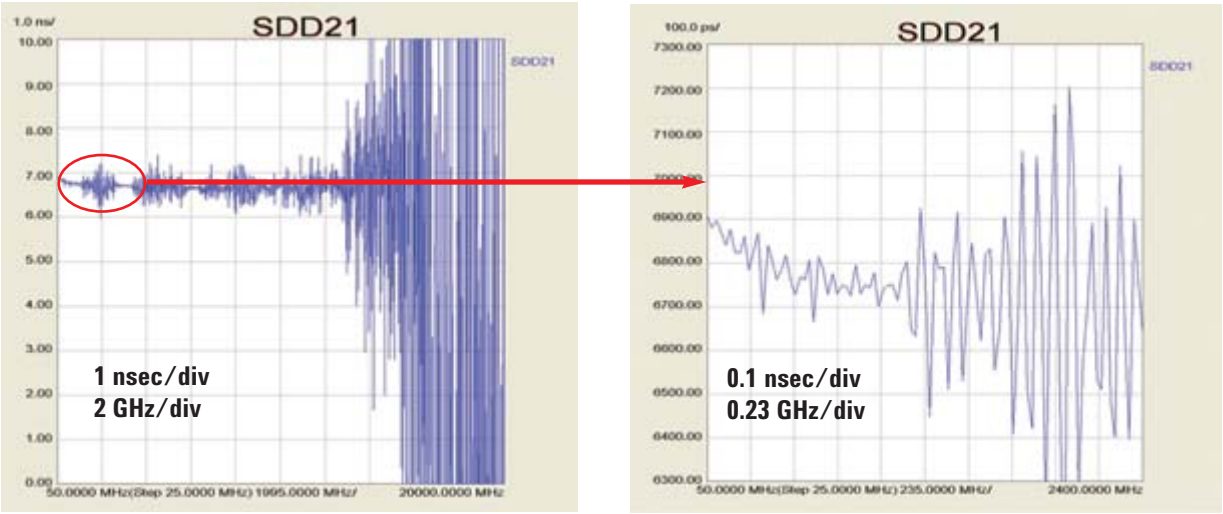


Figure 24. Group delay of one meter long backplane channel in the frequency domain.

However, it is not perfectly constant. The rapid noise and variation after about 13 GHz is due to the large attenuation. After 13 GHz, there is not much signal coming through to be able to measure the phase delay. In addition, there is some noise on the group delay even above 2 GHz. This is due to the multiple reflections from the elements of the differential channel such as the connectors and SMA launches. These multiple reflections will contribute to some distortion of the transmitted signal.

None of these features arise from the natural dispersion of the dielectric material that makes up the multilayer backplane. There is, in fact, dispersion in the laminate, but it occurs only at very low frequencies and has a very small magnitude. By expanding the scale, as in the figure to the right, and zooming in on the first 2 GHz, we see a small drop off of the group delay.

At 50 MHz, the group delay is about 6.9 ns. By 500 MHz, the group delay has dropped to 6.75 ns and is there after relatively constant. This is a change of about 0.15 ns out of 6.8 ns or two percent. Of course, by 500 MHz, the multiple reflections in the differential channel totally swamp any dispersion in the laminate. This is why worrying about dispersion and frequency dependence to the dielectric constant is often more of a distraction from worrying about the real problems that will cause performance complications.

The time delay through the interconnect can also be measured in the time domain by observing the received differential signal. This is the TDD21 term of the T parameters. Figure 25 shows an example of the measured TDD21 signal coming out of the same 40 inch backplane trace that was shown previously in the frequency domain.

Figure 25. Time delay of one meter long backplane channel.

In this example, the bandwidth of the measurement is 20 GHz and the setting for the time domain window was nominal. This means the effective rise time of the incident signal is 0.7/20 GHz or 35 ps. On this scale of 200 ps per division, the input stimulus would have a 10-90 rise time of less than 0.2 divisions. Clearly the rise time of the leading edge of the output signal has increased considerably. This is due mostly to the attenuation, and to a lesser amount, the group velocity dispersion created by the multiple reflections.

Where do we draw the line to say the time delay of the signal is some value? Which part of the rising edge do we use to measure the time delay? In the frequency domain, we were able to get an average value of 6.8 ns, even though there was as much as ± 0.5 ns of noise. In the time domain, what part of the wave do we use to measure as reference to arrive at one value for the delay of the signal?

This is why the delay of a signal is only a rough metric of performance. The delay will depend on where we define the reference level of the received signal. This will vary depending on the pattern of bits in the stream and gives rise to a form of jitter classified as deterministic jitter.

As a rough approximation to the delay, we can use the mid point of the signal as the reference level. This is where the received signal will cross the 50 percent voltage point. With a 400 mV incident signal, this threshold is 200 mV. Using markers on the front screen, we can directly read the time delay to the 50 percent point as 6.84 ns. This is very close to our estimate of 6.8 ns from the frequency domain.

The previous example determined the time delay associated with the differential signal. For high speed serial interconnects, the differential signal is the only component that the receiver is sensitive to. However, another term that also characterizes the interconnect is the time delay for the common signal component.

While this is typically an unimportant term, it is trivial to measure and might sometimes offer insight into the interconnect with a quick look. In a uniform differential pair, with homogenous dielectric, the common signal and differential signal will see the same dielectric distribution and hence, the signals will travel at the same speed and have the same group delay.

Figure 26 shows the group delay of the differential and common signal as having exactly the same delay. With a few minor variations due to the different impedance profiles and different multiple reflections, the general features of the group delay are identical for the differential and common signals, as expected for stripline interconnects.

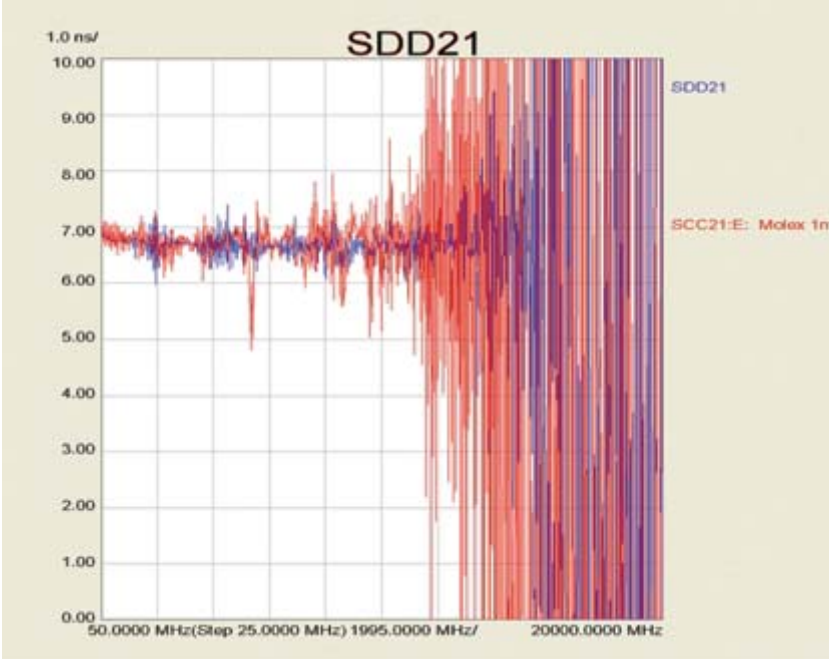


Figure 26. Group delay of differential and common signal.

In the time domain, the received signals will appear at the receiver at roughly the same time as well. In a homogenous material, the two signals are impacted exactly the same way by the dielectric.

Figure 27 shows the measured received signal for the differential and common signal in the time domain. This is the TDD21 and TCC21 terms in the differential T matrix elements. On this scale of 200 ps per division, the two received waveforms are virtually identical.

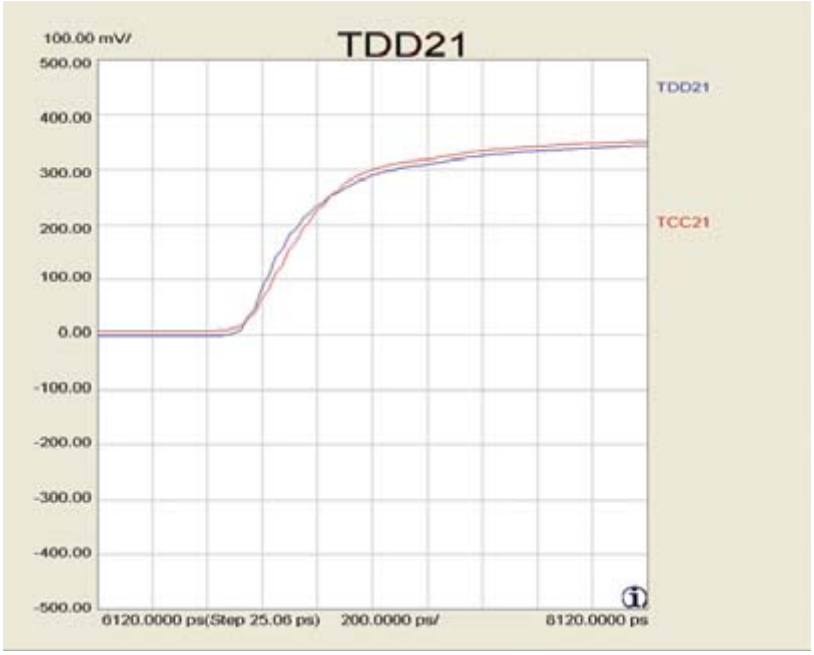


Figure 27. Time delay of the received differential and common signals.

However, if there were any asymmetry in the distribution of dielectric materials, so that the electric fields associated with the common signal saw a different effective dielectric constant than for the differential signal, there would be a difference in the group velocity and time delay for the two types of signals.

For a microstrip differential pair, the differential signal will have more field lines in air than the common signal. This will give the differential signal a lower effective dielectric constant, a higher speed, and a lower group delay, compared to the common signal.

Figure 28 shows the measured group delay of the common signal transmitted through the four inch microstrip differential pair, as SCC21, and the group delay of the differential signal, SDD21. We see the general features of the noise from the non 100 ohm differential impedance and the non 25 ohm common impedance. On top of this is the clear offset between the average group delay of the common signal at about 680 ps and the group delay of the differential signal of about 600 ps.

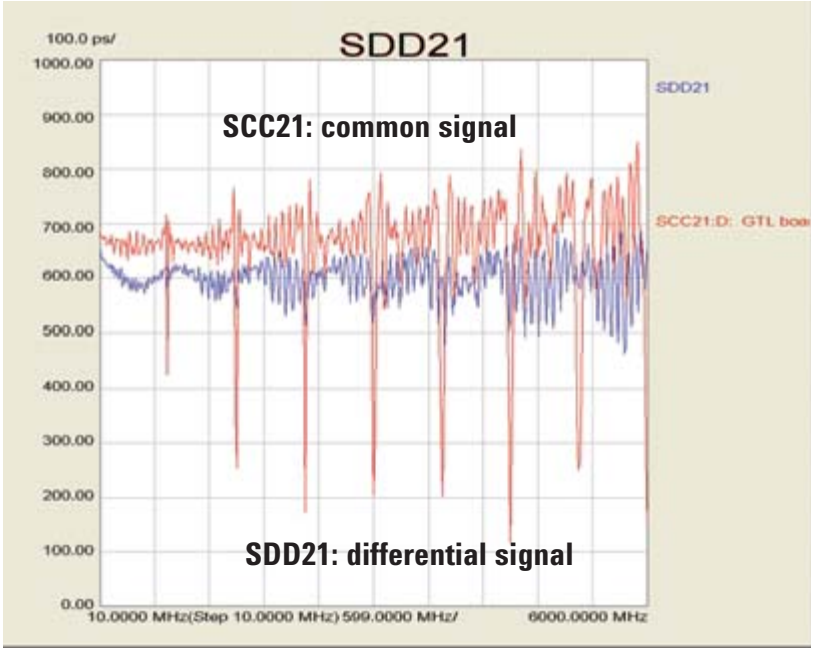


Figure 28. Group delay in a microstrip differential pair.

Based on these delays and the four inch long interconnect, we can estimate the speed of the common signal as 4 in/0.68 ns = 5.9 in/ns while the speed of the differential signal is 4 in/0.6 ns = 6.7 in/ns. While this difference does not affect the differential signal, it is the effect which ultimately gives rise to far end noise, when this differential pair is considered as two single ended transmission lines with cross talk.

Viewed in the time domain, the different arrival times of the common signal and the differential signal in a microstrip is very clear. Figure 29 shows the TDD21 term and the TCC21 term for the four inch long microstrip.

Figure 29. Common and differential time delay in microstip.

This time delay difference can be read off the screen using the markers as 54 ps, out of a total delay of 600 ps.

1.11 The bandwidth of an interconnect

The most important role of an interconnect is to transmit a signal from one point to another with acceptable distortion. It is impossible to transmit a signal with no distortion, so it is often a question of how much is too much.

One metric of the distortion imposed by the interconnect is the attenuation of the signal, and how much amplitude is left coming out of the interconnect. Because the attenuation is different at different frequencies, it is often easier to evaluate the attenuation in the frequency domain. The term that most effectively characterizes the signal degradation in transmission through the interconnect is the SDD21 term. This is also called the differential insertion loss.

Figure 30 shows the measured differential insertion loss of a 22 inch channel on a motherboard up to 20 GHz. This defines the behavior of the interconnect. This plot also indicates the noise floor of the measurement as about –70 dB.

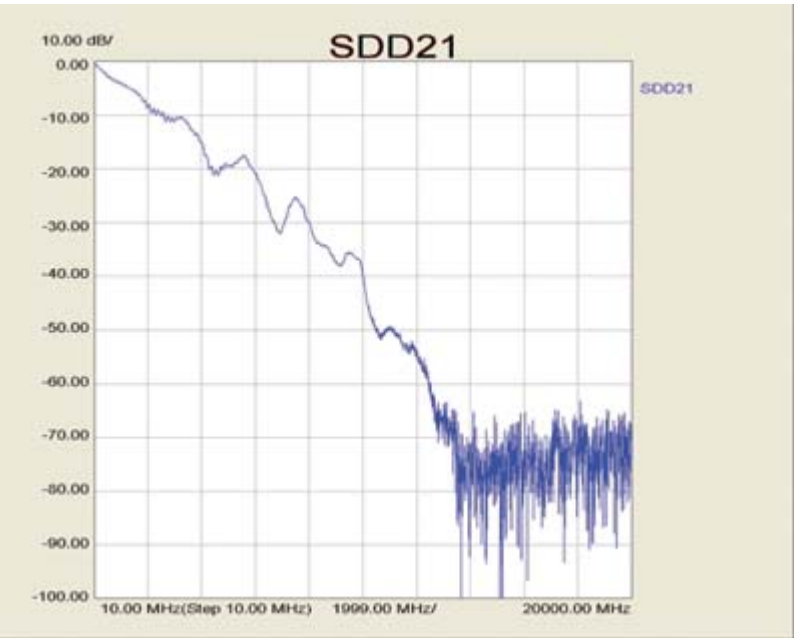


Figure 30. Differential insertion loss in 22 inch motherboard differential channel.

From this insertion loss, we can estimate the highest useable frequency, or the bandwidth of the interconnect. To do this, we need to know how much attenuation is acceptable. This depends on the type of drivers and receivers used in the application. These devices are typically called SerDes chips, which is short for serializer and deserializer chips.

A low end driver might work with a differential insertion loss of –10 dB. A mid range SerDes with some pre-emphasis capability might require at least –20 dB, while a high end device, with integrated pre-emphasis and equalization, might allow as much as –30 dB. Which device family is used will ultimately determine the usable bandwidth of the interconnect. This is why it is conventional, when referring to the bandwidth of the interconnect, to refer to the –10 dB or –20 dB or the –30 dB bandwidth of the interconnect.

In this example of the 22 inch long motherboard trace, the –10 dB bandwidth is 2 GHz, while the –20 dB bandwidth is about 4 GHz and the –30 dB bandwidth is 7 GHz.

There are three critical terms that influence the differential insertion loss of a differential channel: the length, the dissipation factor of the laminate, and the presence of impedance discontinuities.

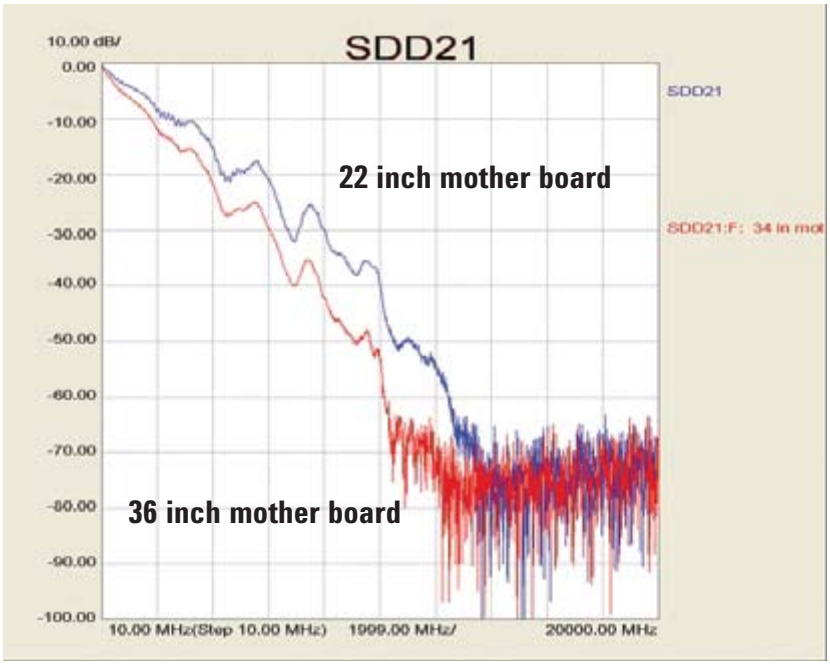


Figure 31. Differential insertion loss of two different length motherboard traces.

Usually, there is little that can be done in the design to change the length. This is fixed by the system architecture selected. All things being equal, a longer length interconnect will result in higher insertion loss and lower bandwidth. Figure 31 shows an example of two differential channels on the same motherboard, using the same daughter cards, but with total lengths that are 22 inches and 36 inches. The drop in –20 dB insertion loss is not 60 percent lower in the longer interconnect compared to the shorter one. It is only about 10 percent lower. This is because a large fraction of the insertion loss is due also to the impedance discontinuities.

1.12 Rise time degradation

The drop off in insertion loss with frequency is a direct measure of the higher attenuation seen by the higher frequency components. The effective rise time of the signal incident to the device is 35 ps for a measurement bandwidth of 20 GHz and time domain window setting of nominal. If this rise time came out, the insertion loss would be above –3 dB all the way through to almost 20 GHz. The losses in the interconnect remove the highest frequency components of the signal and decrease the bandwidth of the signal.

By the time the signal comes out of the interconnect, the –3 dB frequency has shifted from 20 GHz to closer to 1 or 2 GHz. This means the rise time of the signal will be significantly increased from 35 ps to much higher, into the 200 to 500 ps range.

Figure 32 shows an example of the transmitted differential signal in the time domain, the TDD21 term, on a scale of 100 ps per division. When the edge is no longer close to a Gaussian shape, it is difficult to use one number to describe the rise time. The 10-90 rise time has little significance since the tail is so long. The 20-80 rise time or the time to reach the 50 percent point might have more meaningful significance, though both values are only rough approximations to the actual behavior of the edge.

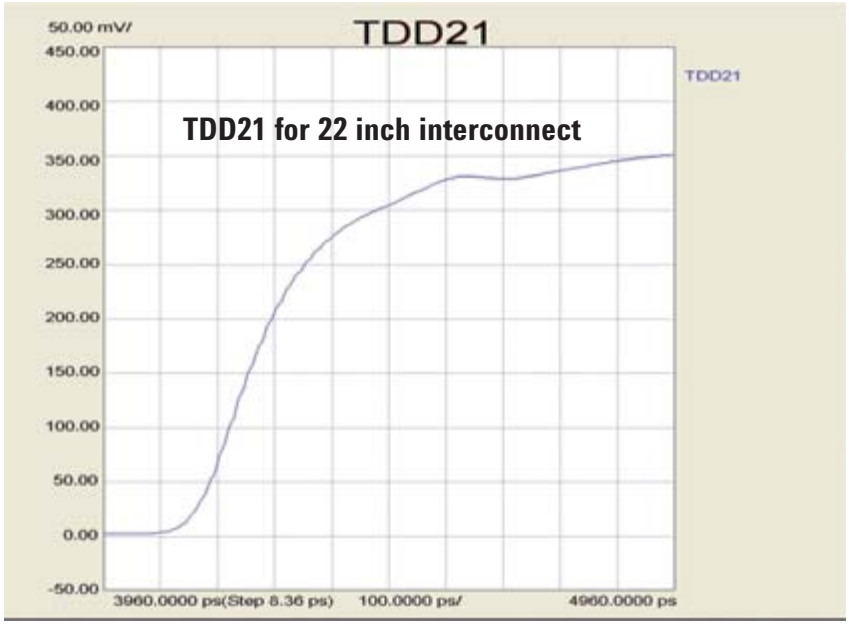


Figure 32. Rise time degradation of transmitted signal through 22 inch long motherboard.

What is more significant is how far the signal rises during a bit period. This will strongly influence the amount of intersymbol interference (ISI) and collapse of the eye to be expected. For example, a 1 Gbps bit stream will have a bit period of 1 ns. From the measured TDD21 display in Figure 32, we see that in 1 ns, the received signal will reach more than 85 percent of its final value in 1 bit period. There will be virtually no ISI and the bit quality should be excellent.

A 5 Gbps signal will have a bit period of 200 ps. In this short a time, the final signal will reach only 250 out of 400 mV or 62 percent of the final value. This is 50 mV above the midpoint voltage. If the bit pattern had been all highs for a long period, the next low bit would extend only 50 mV below the midpoint. The combination means the maximum eye opening we would expect to see is 100 mV. This is probably below the noise margin of most receivers. This interconnect would have a problem supporting a 5 Gbps bit stream.

As was apparent looking at the SDD21 differential insertion loss term, all things being equal, a longer interconnect means a higher insertion loss. This will also result in a longer rise time of the transmitted signal, and offer worse high bit rate performance.

Shown in Figure 33 is the measured signal at port 2 for a 22 inch long interconnect with a 36 inch long interconnect superimposed to begin at the same location. The much longer rise time, on the order of 300 ps, for the longer interconnect is all due to the drop off of the insertion loss from dielectric loss and impedance miss matches. The longer rise time will have a bigger impact on high bit rate signals than the shorter rise time signal.

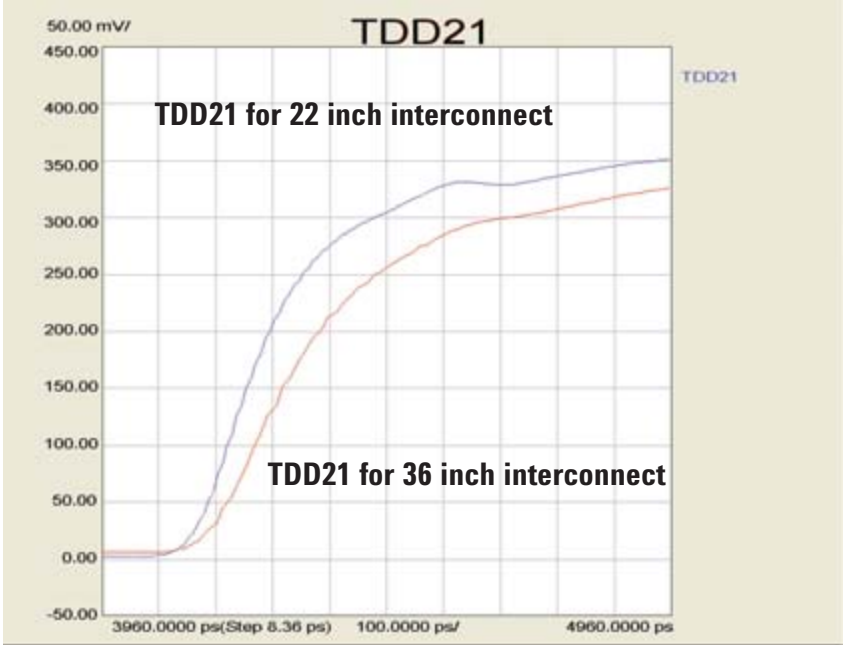


Figure 33. Rise time degradation of transmitted signal after 22 and 36 inches.

A signal with a rise time of 300 ps has an equivalent bandwidth of roughly 0.35/0.3 ns or about 1 GHz. This is a pretty good estimate of the –3 dB insertion loss of the interconnect as seen in Figure 32. Of course, the concept of bandwidth is inherently an approximation. If knowing the bandwidth to 10 percent accuracy is important, one should not use the concept of bandwidth, but the entire spectrum of the signal.

1.13 Eye diagrams

One of the most important ways of evaluating the performance of a high speed serial signal is converting the data stream into an eye diagram. A bit stream is a series of hi and low signals, synchronous with a clock. Using the clock as the trigger, each bit is extracted from the stream and superimposed. The resulting combination of all possible bit patterns looks a little like a human eye and has been called an eye diagram. An example of an eye diagram is shown in Figure 34. This is created from the measured TDD21 element of a 34 inch long mother-board interconnect.

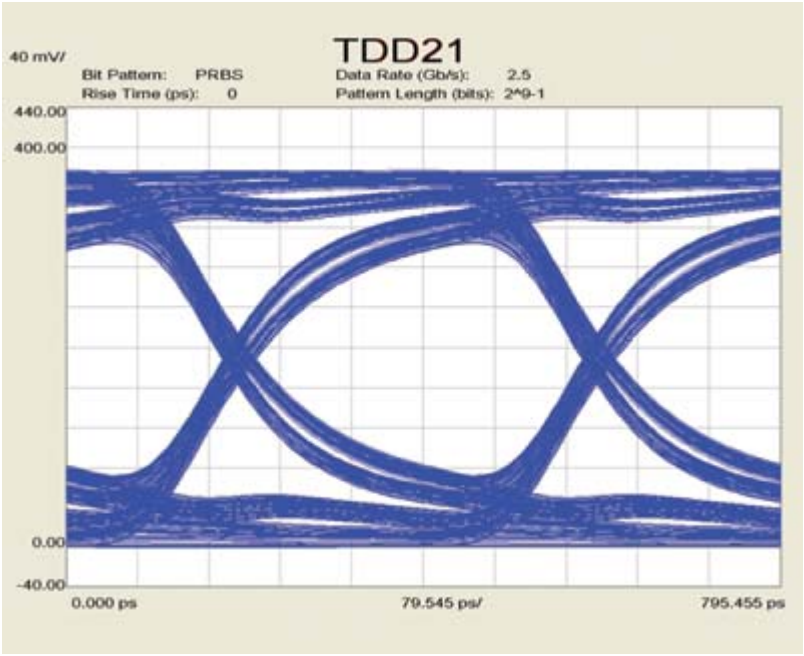


Figure 34. Eye diagram of 34 inch long motherboard interconnect.

The two most important features of an eye diagram are the height of the opening on the vertical scale and the width of the cross over regions on the horizontal scale. Depending on the noise margin of the receiver, the opening of the eye must be at least 150 to 200 mV, while the cross over widths should be only a small fraction of the period. This width is often called the deterministic jitter. These two terms fundamentally limit the highest bit rate that can be transmitted down an interconnect.

The eye diagram of a pseudo random bit stream (PRBS) can be simulated for an interconnect based on the measured S parameter behavior model. PLTS can synthesize a PRBS signal and simulate the impact on this signal from the interconnect and display the output signal in the form of an eye diagram.

In generating the PRBS signal, one of the parameters is the number of bits that should appear in the signal before it repeats, or the word length. In principle, it could be infinite, but there is always a trade off between how accurate the answer needs to be and how long to run the simulation.

Figure 35 illustrates the difference in the simulated eye diagram for a 2.5 Gbps PRBS signal, with $2^7 - 1$, $2^9 - 1$ and $2^{11} - 1$ as the word length. Based on this analysis, as a good rule of thumb, $2^9 - 1$ bits in the pattern is a good value to start with and take quick looks, while a final simulation might be done with $2^{11} - 1$ bits. The computation time is only a few minutes for most situations.

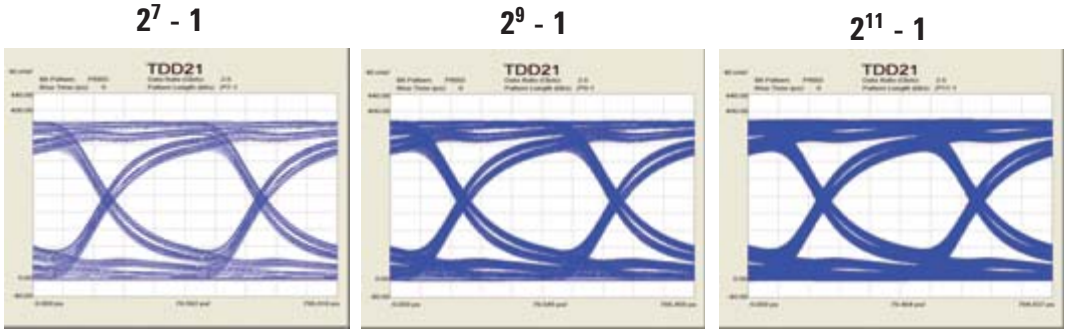


Figure 35. Eye diagram and PRBS word length.

For the same 36 inch long motherboard interconnect, the eye diagram for different bit rates can be simulated to identify the performance of the interconnect. It is important to note that in this simulation, there is no pre-emphasis or equalization of the signal. It is only a simulation of the eye diagram performance of the interconnect, assuming a PRBS bit stream is incident with a rise time, based on the measurement bandwidth. For 20 GHz, it is roughly 35 ps. The rise time is dramatically increased by the interconnect and contributes to the deterministic jitter and the collapse of the eye diagram.

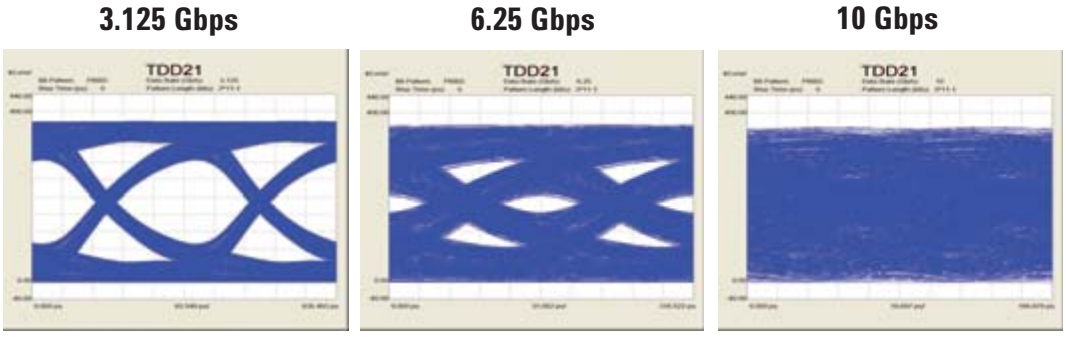


Figure 36. Bit rate collapse of the eye.

This particular interconnect would be perfectly suitable for XAUI type signals at 3.125 Gbps, but would probably not work for XAUI 2 interfaces at 6.25 Gbps. As can be seen from Figure 36, it is completely unusable for 10 Gbps signals unless pre-emphasis or equalization were used in the SerDes chips.

The differential insertion loss is a good indication, but not a total indictor, of the collapse of the eye diagram. The larger the insertion loss, the more the eye will be collapsed. However, it does not directly indicate the impact from the deterministic jitter which will close the eye in from the sides.

Figure 37 shows an example of the differential insertion loss of three different, differential channels in various backplanes. The lowest loss is for an interconnect eight inches long, the next greater loss is from a 25 inch interconnect, and the highest insertion loss is from a 40 inch long backplane.

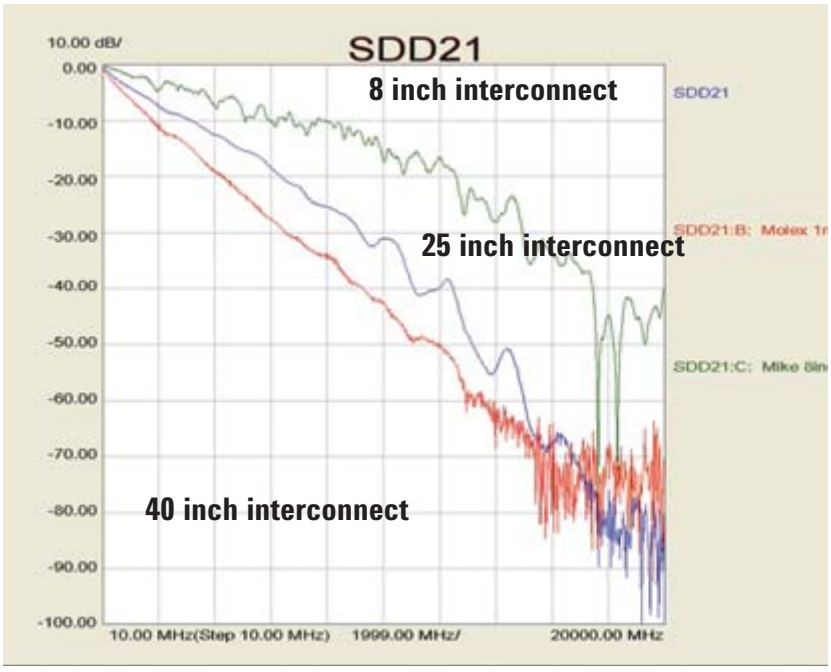


Figure 37. Insertion loss of three different length interconnects.

By taking the measured S parameter data from these three interconnects, the PRBS eye diagram can be simulated for a bit rate of 6.25 Gbps. This corresponds to the increasingly popular XAUI 2 interface. It's clear from Figure 38 that at this bit rate, the 40 inch backplane has no hope of supporting XAUI 2 without the use of SerDes features such as pre-emphasis and equalization.

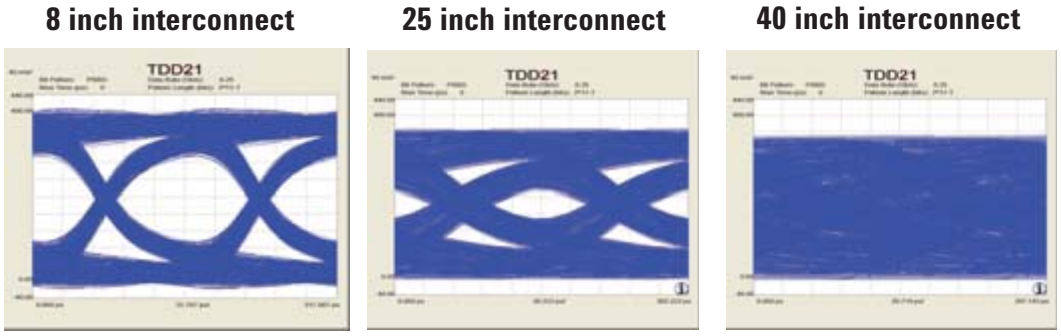


Figure 38. Eye diagrams for PRBS patterns at 6.25 Gbps.

In general, the shorter the interconnect and the lower the insertion loss, the higher the bit rate that can be supported. Even with the insertion loss measurement, there is no substitute to simulating the eye diagram itself.

1.14 Impulse response and pre-emphasis taps

Typical backplanes can exceed 40 inches. This includes six inches on both daughter cards and 36 inches on the backplane itself, for a total of 48 inches. As illustrated earlier, even a 40 inch interconnect can have 100 percent eye closure at 6.25 Gbps. This would seem to limit the use of FR4 based backplanes to applications less than 6.25 Gbps.

One solution is to use lower loss laminates. This will increase the cost of the backplane, but may increase the usable bit rate by 50 percent depending on the material selected. Another popular method of increasing the bit rate, while still using a low cost laminate, is by using pre-emphasis in the SerDes driver. This method adds extra high frequency components to the signal launched into the interconnect. It is implemented by adding an extra amplitude to the bits based on the specific bit pattern in the signal.

In some versions of SerDes drivers, pre-emphasis is added to not just the first bit in the sequence, but to the next one, two, or three bits, either as positive or negative signals to compensate for multiple reflected signals. Using the TDD21 signal, displayed as an impulse response, we can estimate which consecutive bits should have additional signals added or subtracted to them to compensate for the interconnect.

Figure 39. Impulse response of the incident signal, time domain window set to nominal.

The time domain response of the interconnect can be simulated as either a step response or an impulse response. The frequency components of a step response drop off like those of a square wave, inversely with frequency. The frequency components of an impulse response are constant with frequency. The full width, half maximum (FWHM) width of the impulse response is the 10-90 rise time of the incident signal. For a 20 GHz measurement bandwidth, the impulse response of the incident signal into the interconnect is about 35 ps. Figure 39 shows an example of the incident signal impulse response having a FWHM of 35 ps.

Of course, due to the losses and impedance discontinuities in the interconnect, this 35 ps wide impulse signal quickly spreads out by the time it exits the interconnect. Shown in Figure 40 is an example of the output impulse response from traveling through 36 inches of a motherboard, on a scale of 200 ps per division. The incident signal would be less than a fifth of a division wide on this scale.

Figure 40. Impulse response after 36 inches through a motherboard.

In addition to a spreading out of the pulse, there are multiple steps appearing after the main peak, due to the multiple bounces of the signal against impedance discontinuities. If the bit rate were 5 Gbps, the bit period would be 200 ps. This profile of the impulse response is a rough measure of what one bit of data would look like at the far end of the line.

If this response is known ahead of time, the data stream can be modified to minimize the amount of cross talk between successive bits, or intersymbol interference, generated due to the multiple reflections. Different SerDes technologies allow adding or subtracting voltage levels to successive bits in the series. Each successive bit is called a tap and three taps is the typical limit.

For example, if the first bit has pre-emphasis added to it, we would want to subtract about 20 percent of the signal amplitude to the first tap, the second bit, nothing on the second tap, and subtract possibly 10 percent of the signal to the third tap. With this sort of signal, the pulse propagating through the interconnect will have components that help to cancel out the multiple reflections. Using the impulse response of the transmitted differential signal can help guide the design process to quickly reach the optimum pre-emphasis and tap pattern for minimum ISI and maximum opening of the eye.

1.15 Mode conversion and EMI

One of the most difficult problems to fix in high speed product design is EMI. The largest source of EMI is radiation from common currents which get out on unshielded twisted pair cables, such as cat5 cables.

Normally, the signals launched on twisted pair cables are supposed to be differential signals. A pure differential signal on an unshielded twisted pair will not radiate very much at all. It poses no problems for EMI. It's when unwanted common signals get into the twisted pair cable that radiated emissions can happen.

As a rough rule of thumb, the radiated field strength, at the three meter distance in an FCC class B type open field test, from common current on a twisted pair, is about 40 mV/m x V x f, with V the voltage of the common signal and f the frequency in GHz. The typical FCC certification failure threshold near 1 GHz is a field in excess of 0.4 mV/m. This suggests that to pass an FCC certification test, the maximum allowable common signal on an external twisted pair should be less than 10 mV at 1 GHz.

In principle, if the drivers produce a perfect differential signal with no common signal, and it passes through an ideal differential pair, there should be no common signal generated. In practice, any asymmetry in the interconnect, such as nonequal line widths in the pair, or different lengths in the two lines, or different local effective dielectric constant, as due to the glass weave of the laminate, will convert some of the differential signal into common signal. We call this process mode conversion.

As long as none of this common signal gets out of the box, it will not affect EMI. Of course, if the mode conversion is significant, it may affect the quality of the differential signal's edge, which will have an impact on the eye diagram. But, the common signal will do no harm. It is only if some of this converted common signal gets out on twisted pairs that an EMI problem might arise.

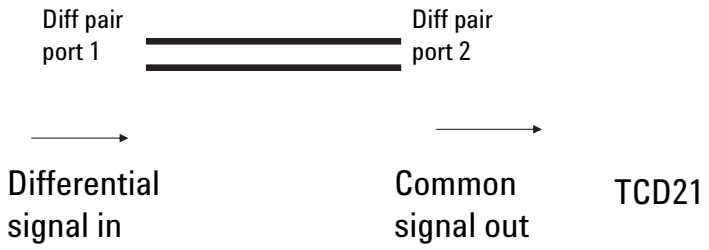


Figure 41. Mode conversion.

The amount of common signal converted from the differential signal by asymmetries in an interconnect can be measured directly by one of the differential T parameters. This is illustrated in Figure 41. Mode conversion is measured by sending a differential signal in at port 1 and looking at how much common signal comes out of port 2. This is the TCD21 term. Measuring the magnitude of TCD21, compared with the 400 mV incident signal, is a measure of the common signal converted.

For the case of a 20 inch backplane, Figure 42 shows the measured TCD21 signal. This is the signature of the common signal that comes out of the interconnect, with a pure 400 mV differential signal step edge going in. This suggests about 1.2 percent of the differential signal is converted into common signal.

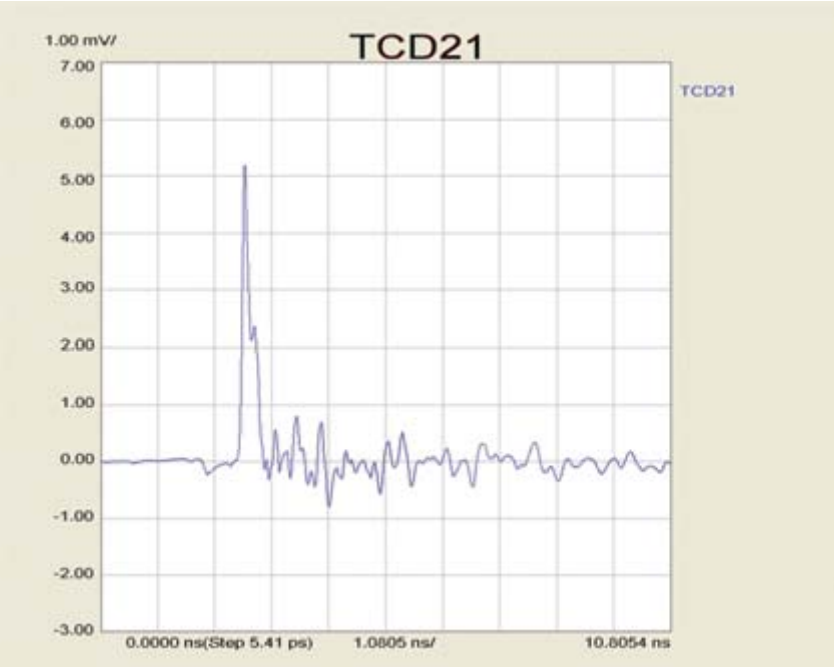


Figure 42. TCD21 from 20 inch backplane.

Every bit edge that gets transmitted to external cat5 cable will have 1.2 percent of the differential signal as common signal and contribute to EMI. If the incident voltage is 1 V, approximately 12 mV of common signal may get on the external twisted pair. By itself, this is close to the threshold that would fail FCC certification. In addition, any skew between the drivers will also convert the differential signal into common signal and add to the radiated emissions. This amount of mode converted common signal might cause a problem.

The first step to solve any design problem is to understand the root cause and optimize the design to fix this problem. To fix this problem, we'd like to find out, where in the interconnect path is the asymmetry that might be generating this common signal. To find this, we can take advantage of another one of the differential T parameters.

As illustrated in Figure 43, if we send a differential signal into port 1, we can look at the converted common signal that comes back out of port 1 as TCD11. The key feature of this signal that enables us to use it to debug the root cause of the mode conversion is its time dependency.

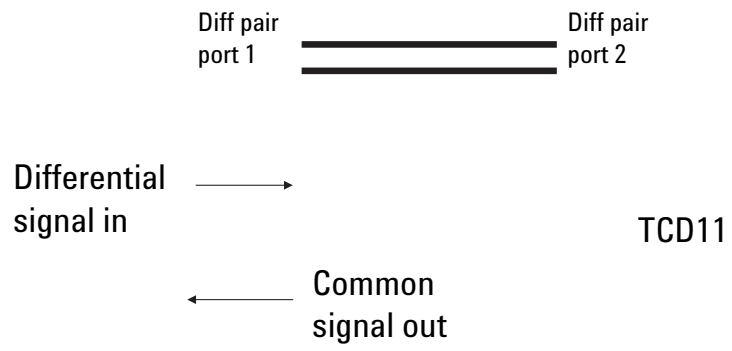


Figure 43. Mode conversion.

We are effectively launching a step edge into the interconnect. As this edge propagates down the differential pair and encounters any asymmetry, a common signal will be generated. Some of this common signal will propagate in the forward direction, and will be picked up at port 2 as the TCD21 signal, but at the same time, some of this common signal will be sent in the backward direction, back toward port 1. This is the TCD11 signal.

The time between sending the signal into port 1 and picking up the common signal that comes back is the round trip time of flight for the incident differential signal to reach the asymmetry and then for the common signal to travel back to port 1. By comparing the time response of the TCD11 signal to the TDD11 signal, we can look for what features of the interconnect which we can identify in the TDD11 signal are coincident with the TCD11 signal.

In Figure 44, the bottom trace is the TCD11 response. The top trace is the TDD11 response. In this signal, we can identify the negative dips from the via fields of the connectors in the daughter card and the motherboard. The region between them is the connector.

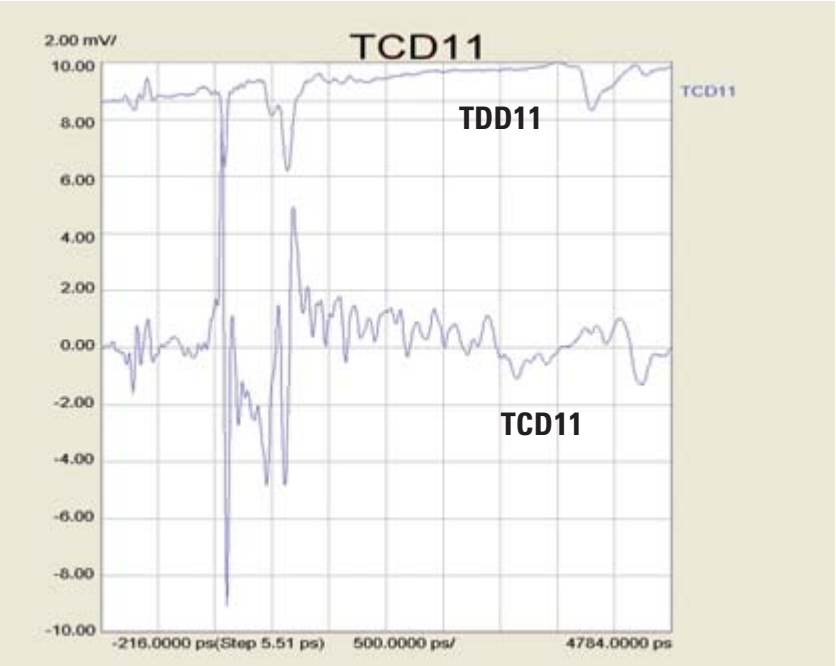


Figure 44. 20 inch motherboard TDD11 response.

The TCD11 response shows a large peak in the generated common signal coincident with the via field in the daughter card and a smaller one in the motherboard side. In addition, a negative common signal is generated and sent back to port 1 by the connector itself. This suggests that an improvement could be made by minimizing the capacitive discontinuities of the connector attach region and adjusting the connector design to be more symmetrical.

Most differential channel interconnects composed of daughter cards and backplanes, will show the dominant source of mode conversion to be in the via field of the connectors. Figure 45 shows another example of a 25 inch backplane interconnect. The common voltage signal as measured by TCD21 is almost 8 out of 400 mV or 2 percent.

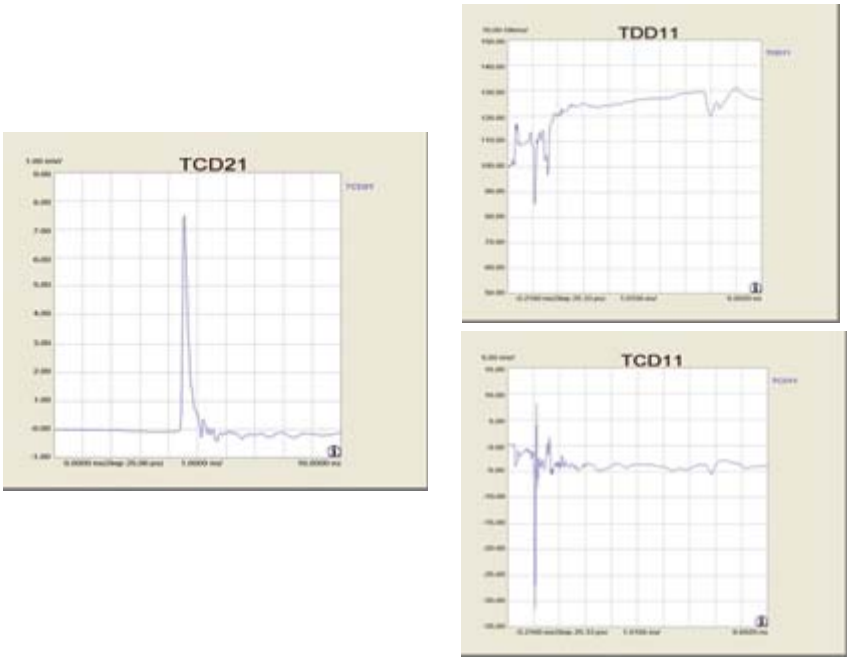


Figure 45. 25 inch backplane example.

The comparison of TDD11 and TCD11 shows the source of the common current to be the via field in the connectors. Unless they are optimized to minimize the impedance discontinuity of the excess capacitance of the vias and pads, there will always be asymmetries in the signal-return current flow. These asymmetries will convert the differential signals into common signals. By minimizing the impedance discontinuity by back drilling the via stub, for example, the bandwidth of the interconnect will be increased and the converted common signal will be decreased.

1.16 Modeling differential channel interconnects

The S parameters of an interconnect, whether measured in the time or the frequency domain, represent a behavioral model of the interconnect. They contain all the information about how a signal entering one port will behave when it exits another port. Depending on the question we are asking about the interconnect, one or more of the S or T parameters, either as singled-ended or balanced, might get us close to the answer.

In those cases where more detailed information is needed, we can use the exported S parameters as a behavioral model and integrate them directly into some circuit simulators. This would allow us to perform a system level simulation of the behavior of the drivers, interconnect, and receivers.

Not all EDA tools allow the use of S parameter behavioral models. Instead, a commonly used model format to approximate a real differential pair is as two, lossy, single ended, coupled, transmission lines. This model, sometimes called a W element model, as it is referred to by HSPICE, describes a pair of coupled transmission lines in terms of their RLCG (resistance, inductance, capacitance, conductance) elements. This model assumes a uniform, coupled, lossy, pair of lines. The distributed elements are defined as their per unit length values. The default units are ohms/m, H/m, F/m and S/m.

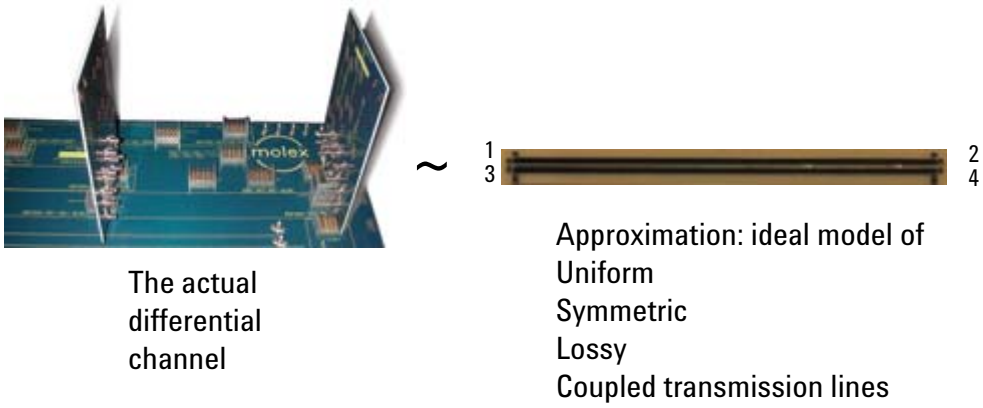


Figure 46. Modeling a real interconnect as an ideal, uniform interconnect.

It is important to keep in mind, as illustrated in Figure 46, that what we are doing is taking the real, measured S parameter behavior of the differential channel, and approximating it as a single, uniform pair of coupled lines. This is not always a good assumption, but can sometimes help get us a satisfactory answer quickly.

The W element model can be generated and exported from the S parameters, with one click of the mouse,. As illustrated in Figure 47, there are a few intermediate steps that might sometimes offer useful information.

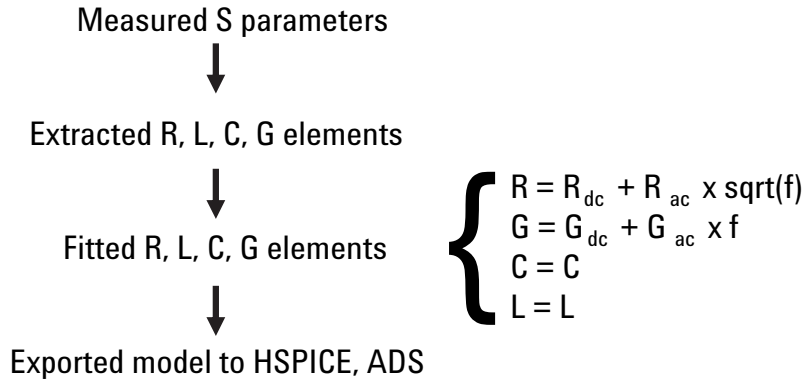


Figure 47. Modeling process.

From the measured S parameters, an ideal, uniform, symmetric, pair of coupled transmission lines is used to analytically extract the model parameters of the ideal line. These parameters can be combined transparently back and forth into a number of different formats, to describe either a pair of single ended coupled lines, or one differential pair. However, in all cases, the model is simplified to assume the lines are perfectly symmetric. This means mode conversion cannot be simulated by this model.

From the extracted circuit element terms, a simple frequency dependent model is fit for each of the elements based on the assumption of skin depth limited currents and constant dissipation factor material. This results in the resistance varying like a constant term, plus a term that increases with the square root of frequency, and the conductance being a constant term, and a term that increases proportional to frequency. The capacitance per length and inductance per length are both assumed to be constant with frequency.

It is these terms, as the single-ended and coupled terms, that are exported as the W element. In addition to approximating the real differential channel interconnect as a uniform differential pair with no asymmetry, the additional assumption to generate the W element is the simple frequency dependence, as shown in Figure 47. In fact, these are often very good assumptions for most real backplane interconnects.

The measured S parameters are used to extract the line parameters for an ideal, uniform, symmetrical pair of coupled transmission lines. This model can be used to extract a description in terms of the differential or common signal behavior of the ideal transmission line. The assumption made is that the line being measured is uniform.

Figure 48 shows the parameters extracted for the case of the differential signal behavior. Of these, the term that has the most value is the real part of the complex impedance. This term is a direct indication of the average differential impedance of the trace. In this example of a uniform differential pair, the extracted differential impedance is seen to be very constant with frequency, up to the full 6 GHz of the measurement. We can read right off the screen that the equivalent differential impedance of this line is 77 ohms.

It is no coincidence that when this same line is displayed as the TDD11 element, on an impedance scale, that we also measured a uniform differential impedance of 77 ohms.

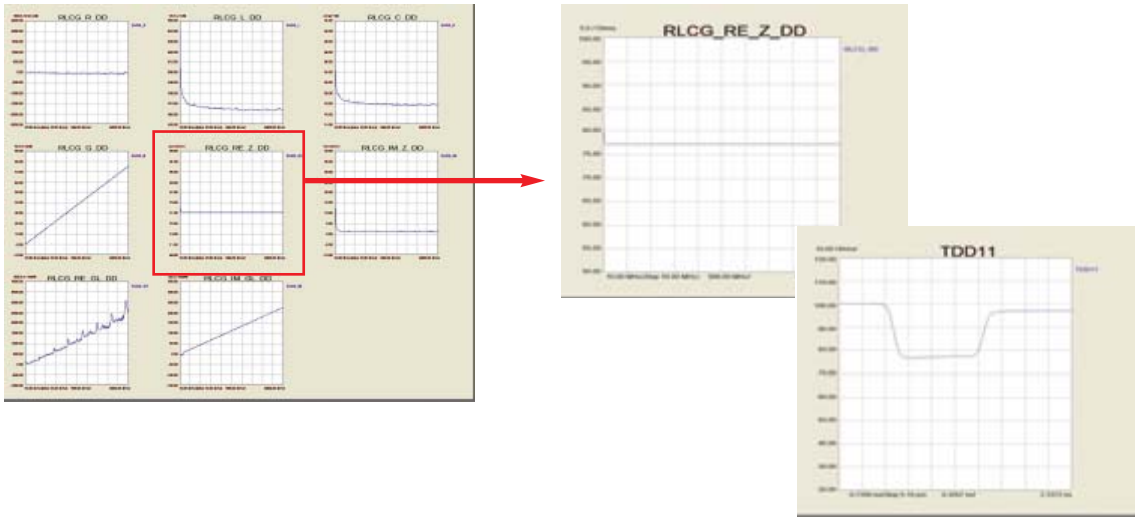


Figure 48. Uniform four inch long differential pair.

When the interconnect is not a uniform differential channel, the extracted real part of the complex differential impedance term can be used to fit, directly from the screen, the effective, average differential impedance.

Figure 49. Extracted differential impedance of 40 inch long backplane interconnect.

Figure 49 is an example of the differential impedance extracted from a 40 inch long backplane. The average differential impedance is about 102 ohms, very close to the target 100 ohms. However, this includes the effects of the daughter cards and connectors in addition to the long trace on the motherboard.

From the extracted values of the line parameters, the W element terms are fitted. By comparing the actual extracted parameters based on modeling the real interconnect in terms of a uniform, symmetrical, coupled pair of transmission lines, we can get an estimate of how well the interconnect obeys the frequency dependent description used by the W element.

In the ideal model, the R11 term, often referred to as the self-resistance, is the resistance per length of one of the lines that makes up the differential pair. Both lines are assumed to be identical as part of the approximation. The self-resistance is extracted from the measured S parameters, based on assuming a uniform pair of coupled transmission lines. It is extracted at each frequency value. If the interconnect were really a uniform line, the self resistance would increase smoothly with frequency. The nonuniformities, such as connectors, vias, and different traces on the daughter card and motherboard, give rise to the jaggedness of the extracted value of the self resistance.

As shown in Figure 50, the extracted self-resistance shows some frequency dependence. For this 40 inch backplane, it has a very low resistance, at close to 5 ohms/m at the lowest frequency, but steadily increases with frequency through 12 GHz, the limit to the display. This increase in resistance can be explained, if we assume the current is skin depth limited. In this case, we would expect the resistance to behave as the W element model, being a constant term plus a term that increases with the square root of frequency.

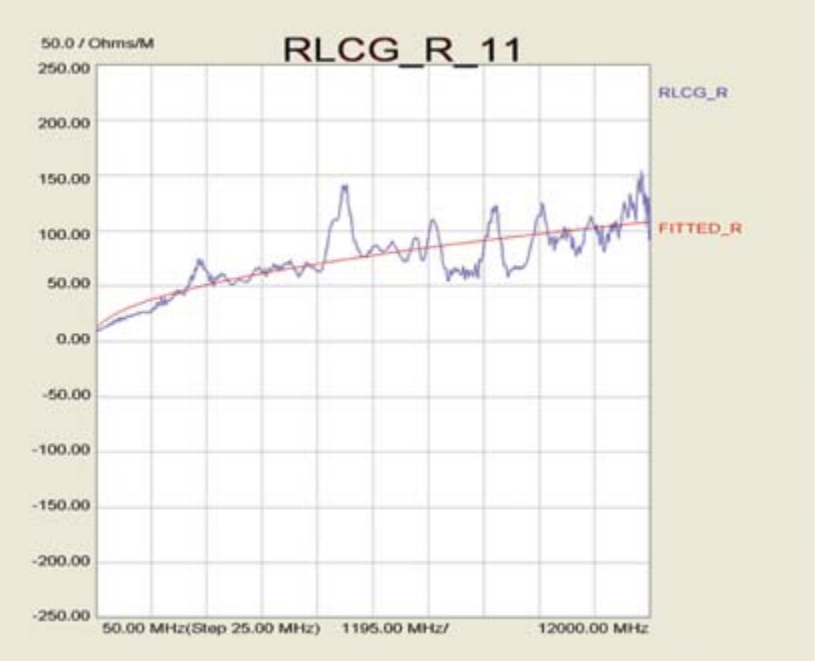


Figure 50. Extracted series resistance per length of either line in the 40 inch backplane interconnect compared with the W element model for resistance.

When we use this model, and find the best values of the DC term and the AC term that fits the data, we get a resistance behavior, shown in Figure 50, as the smooth curve. This model is a very good approximation to the extracted resistance. This suggests that the series resistance of the actual differential channel really is skin depth limited.

We see that the W element for the self-resistance is a very good approximation for this real interconnect.

The second loss term in the W element model is the conductance per length. This is the leakage conductivity through the dielectric from the dissipation factor of the material. If the dissipation factor of the laminate is constant with frequency, the conductance will, by definition, increase linearly with frequency.

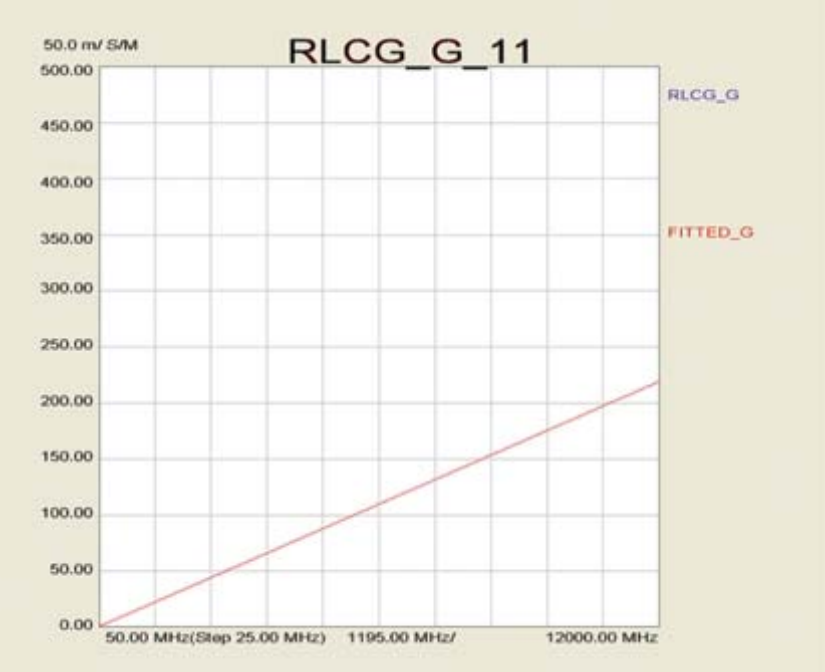


Figure 51. W element model for the conductance per length.

Figure 51 is an example of the extracted and fitted value for the conductance per length for the 40 inch backplane trace. The units are milliSiemen/meter. Two qualities are evident from the extracted terms: it fits the model of an ideal, lossy transmission line with constant dissipation factor really well, and it is a very low value, roughly 50 mS/m at 2.5 GHz.

The W element model of an ideal, lossy, coupled pair of transmission lines assumes the inductance per length and the capacitance per length are both constant with frequency. From the measured performance of a 40 inch long interconnect in a motherboard, as displayed in Figure 52, we see that this is a pretty good assumption.

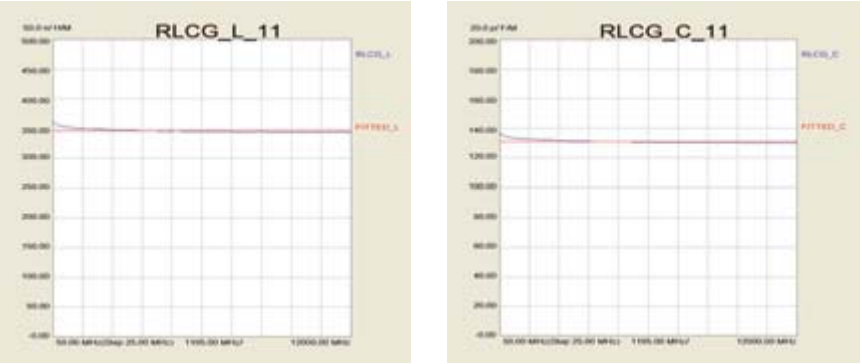


Figure 52. Frequency dependence of L and C.

The extracted capacitance per length and inductance per length show a small amount of frequency dependence at the low frequency end, but quickly reach a constant value and stay there up to the 12 GHz span of the display.

The loop self-inductance per length of one line in the pair can be read off the screen as 350 nH/m, while the self-capacitance per length of one line in the pair can be read off the screen as 130 pF/m. These are the terms that are exported as the W element coefficients.

The six parameters that define the W element, the two for the resistance, the two for the conductance and the capacitance and inductance terms, can be exported into a text file that can be read directly by HSPICE or other compatible circuit simulators.

```
* RLCG parameters for a 2-conductor lossy
* frequency-dependent line

* N (number of signal conductors)
**************************************
2

* Lo
3.462510e-007
9.231448e-010  3.462510e-007

* Co
1.309606e-010
5.198448e-014  1.309606e-010

* Ro
4.52537
-8.83241e-005  4.52537

* Go
1.249961e-012
-7.500219e-013  1.249961e-012

* Rs
0.000946094
0.000123051  0.000946094

* Gd
1.829429e-011
2.163884e-012  1.829429e-011
```

Figure 53. W element model for the 40 inch backplane differential channel.

Figure 53 shows an example of the W element model for the 40 inch backplane trace described previously. Because of the limitation that this model must be symmetric, the diagonal elements of each term are identical. For each of the six elements, there are only two unique terms, the self values and the coupled values. The lower the coupling is, the smaller these off-diagonal terms will be. The units used to describe each term are the default units in SPICE.

1.17 Summary

Everything you ever wanted to know about the electrical properties of a differential channel are contained in the 4-port S parameters. These can be transformed into the time or frequency domain, either as single-ended or balanced terms. The variety of options means we can usually find a format that will display the data so that we can extract the most valuable information quickly and effortlessly.

In this application note, we have described nine different applications for the analysis of a differential channel to characterize its performance and optimize its design. As the final approach, if we can't get the required information directly off the screen of the analyzer, we can always use a system simulation tool to predict the precise behavior of a real signal using the measured S parameters as a behavioral model.

- Characterizing the differential and common impedance profile of a differential channel
- Characterizing the time delay and group delay of the differential and common signal in a differential channel
- Measuring the bandwidth of a differential channel
- Measuring the rise time degradation of a differential channel
- Direct simulation of eye diagrams
- Estimating taps for pre-emphasis from transmitted impulse response
- Estimating possible EMI resulting from mode converted common signal on external cables.
- Identifying the root cause of mode conversion in a differential pair
- Extracting first order transmission line models of a differential pair in RLCG format

References

[1] Many of the principles described in this application note are introduced in detail in the book, *Signal Integrity-Simplified* by Dr. Eric Bogatin, published by Prentice Hall, 2003

[2] Additional application notes can be found at **www.BeTheSignal.com** and are available for free download

[3] Many of the examples of transmission line structures are available in the circuit boards provided with the Master Class Workshops listed on **www.BeTheSignal.com** and reviewed in the online lectures which can be found on this web site

[4] *Signal Integrity Solutions,* Brochure, Literature Number 5988-5405EN, Aug. 29, 2005

[5] *Limitations and Accuracies of Time and Frequency Domain Analysis of Physical Layer Devices,* Application Note, Literature Number 5989-2421EN, Nov. 1, 2005

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