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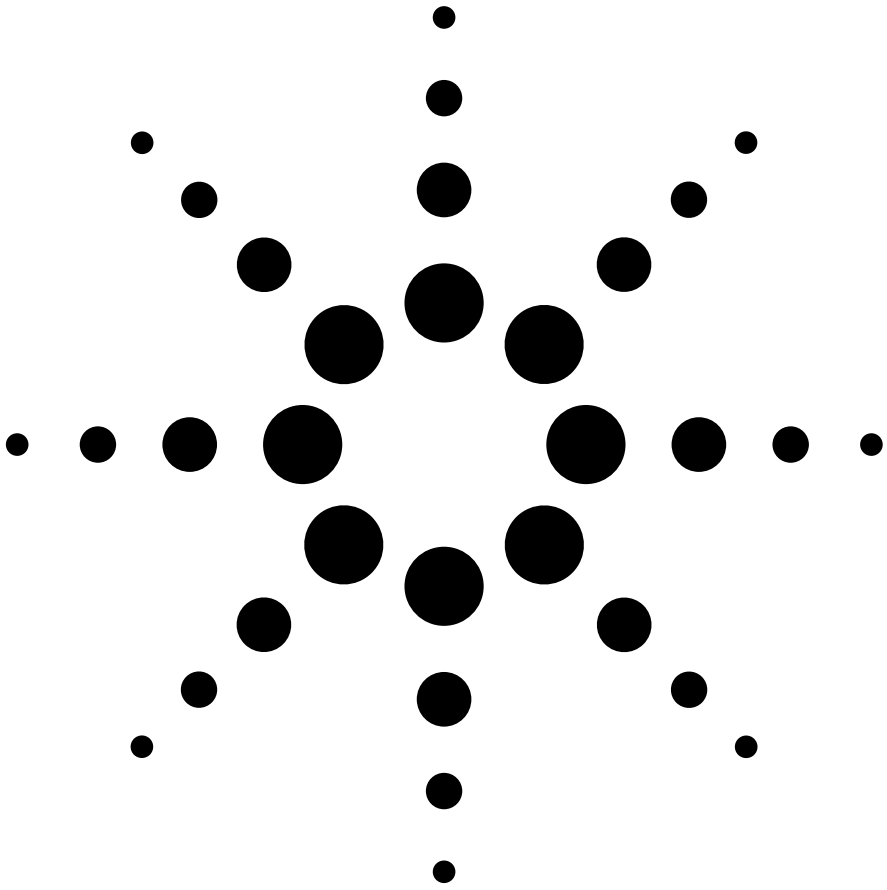
Stripline TRL Calibration Fixtures for 10-Gigabit Interconnect Analysis

White Paper



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Introduction

The design of today's gigabit interconnects require sophisticated measurements; however error correction techniques described to date have been overly theoretical. This paper will illustrate the practical steps required to create a stripline thru-reflect-line (TRL) calibration kit for a vector network analyzer. The creation of a real world stripline TRL cal kit will result in discovering more interconnect performance margin than originally expected. Example elements will be illustrated for a 6-layer Rogers 4350 PCB and an 8-layer Rogers 4350 PCB.

As communication speeds push beyond 10Gb/s, the need for accurate measurements of components of the physical layer becomes critical. Backplanes, printed circuit boards, and connectors must be characterized with precision in order to gain the performance margin required for the industry's highest data rates. A number of pre- and post-measurement error correction techniques can be utilized to obtain the appropriate figure's-of-merit for a specific component. Time-domain gating, port extension, reference plane calibration, normalization, short-open-load-thru (SOLT), thru-reflect-line (TRL), load-reflect-match (LRM) and de-embedding are a few of the most popular techniques used today. One of the most useful calibration techniques that can yield accurate measurements with less effort than most is the TRL calibration. Thru-reflect-line is a pre-measurement error correction that is primarily used in noncoaxial environments, such as waveguide testing, using test fixtures or making on-wafer measurements with probes. TRL uses the same 12-term error model as a SOLT calibration, although with different calibration standards. The SOLT calibrations standards are provided by the equipment manufacturer, whereas the TRL standards must be designed, developed, fabricated and characterized by a signal integrity engineer. Since these TRL standards often consist of stripline printed circuit board fixtures, the need for via structures and connectors creates design challenges that can degrade the calibration accuracy.

When designing a TRL calibration kit, the relationship between the calibration elements and the TRL fixture must be considered. To achieve good measurement results, the fixture and the calibration kit must share several common elements. These connectors include the SMA to stripline interface (the launch) and a specified length of transmission line. Minimizing variation between the fixture elements and calibration kit elements should be a design goal for proper measurement, as well as careful attention to vias, yielding gains in the calibration kit and fixture design efficiency. If proper design methods are used, the load used can be from DC to several GHz and the SMA launch used can be to approximately 20 GHz. This allows for fewer lines, simplifying the calibration kit. It will be shown how it is possible to calibrate a VNA from DC to 24 GHz using a single line element. Fewer connections to accomplish a calibration will result in fewer mistakes and better calibrations. Our goal is to present a case study that will emphasize practical tools and techniques that help ease the burden of creating a TRL calibration kit using common stripline PCB processing methodologies.

Why Calibrate?

Why do we need to calibrate a network analyzer? Isn't this expensive equipment good as it is? To answer these questions, we need to examine the key building blocks of a network analyzer, what it measures, and the major contributors to measurement errors. Only perfect test equipment would not need correction. Imperfections exist in even the finest test equipment and cause less than ideal measurement results. Some of the factors that contribute to measurement errors are repeatable and predictable over time and temperature, and can be removed, while others are random and cannot be removed. The basis of network analyzer error correction is the measurement of known electrical standards, such as a thru, open circuit, short circuit, and precision load impedance. Typical VNA measurements errors are shown in Figure 1.

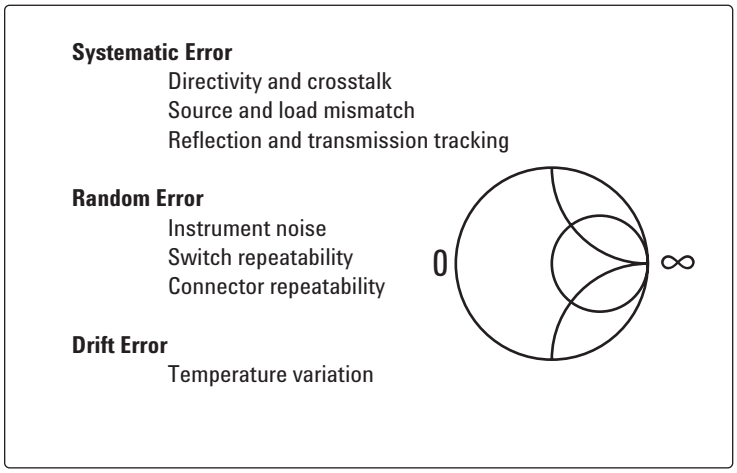

Figure 1. Calibration considerations in vector network analyzers.

Linear 2-Port Network Analyzer Measurements

The foundation for understanding VNA measurement errors lies within understanding the general architecture of this test instrument. The most basic network analyzer, shown in Figure 2, consists of an accurate sine wave signal source and a high frequency switch that routs the signal to either the forward measurement or reverse measurement direction. A signal separation device called a coupler is used to sample the incident signal and the reflected signal at the input port of a device under test. Another coupler is used in a similar fashion to separate the signal at the output port of the device under test. The sampled signals, ao, bo, a3 and b3 can be processed to obtain the input reflection and forward transmission characteristics of the device under test (DUT).

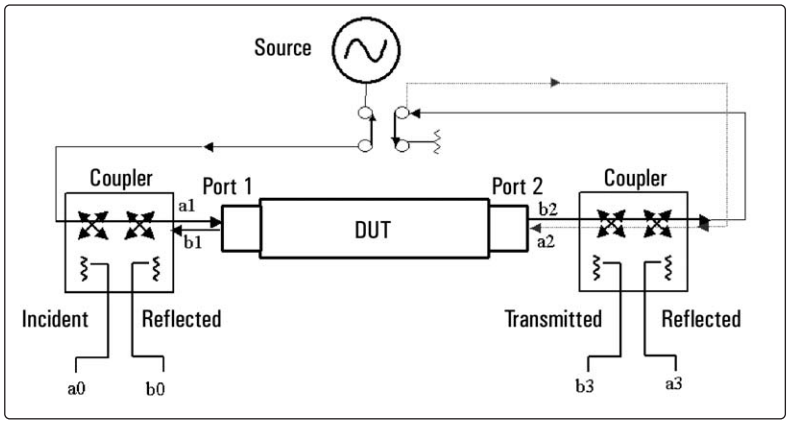

Figure 2. Calibration considerations in vector network analyzers.

Two port S-parameters defined

These input and output signals can be represented by a signal flow graph and expressed mathematically. The signal flow graph shown in Figure 3 is a good picture of what happens in a stimulus/response type of measurement. The formulas for relating the measured quantities to the S-parameters of a DUT are also shown. The definitions of terms are as follows: S = scattering, a1 =incident wave at port 1, a2=incident wave at port 2, b1=reflected/transmitted wave at port 1, and b2=reflected/transmitted wave at port 2. The relationship between these parameters can be expressed in a matrix math equation.

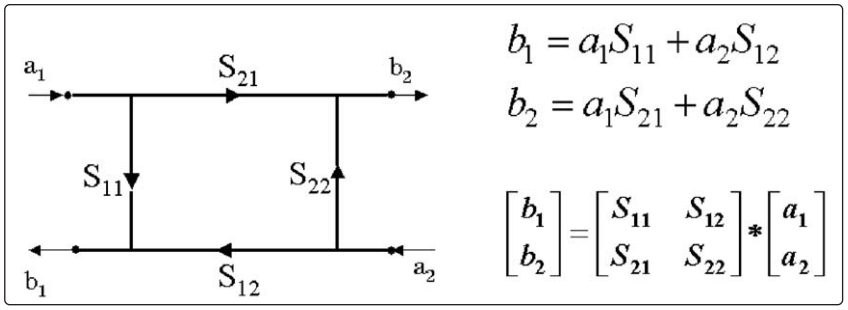

Figure 3. Two port S-parameters defined.

VNA Measurement Errors

All measurement systems, including those employing network analyzers, can be plagued by three types of measurement errors: systematic errors, random errors and drift errors. Systematic errors are caused by imperfections in the test equipment and test setup components such as cabling. If these errors do not vary over time, they can be characterized through calibration and mathematically removed during the measurement process. There are six types of systematic errors: directivity and crosstalk errors relating to signal leakage, source and load impedance mismatches relating to reflections, frequency response errors caused by reflection, and transmission tracking within the test receivers.

Random errors vary randomly as a function of time. Since they are not predictable, they cannot be removed through calibration. The main contributors to random errors are: instrument noise (e.g., sampler noise, and the IF noise floor), switch repeatability, and connector repeatability. When using network analyzers, noise errors can often be reduced by increasing the source power, narrowing the IF bandwidth, or using trace averaging over multiple sweeps.

Drift errors occur when a test system's performance changes after a calibration has been performed. They are primarily caused by temperature variation and can be removed by additional calibration. The rate of drift determines how frequently additional calibrations are needed. However, by constructing a test environment with stable ambient temperature, drift errors can usually be minimized. While test equipment may be specified to operate over a temperature range of 0 °C to +55 °C, a more controlled temperature range such as +25 °C °±5 °C can improve measurement accuracy (and reduce or eliminate the need for periodic recalibration) by minimizing drift errors. Figure 4 shows the block diagram of various components that are susceptible to these errors.

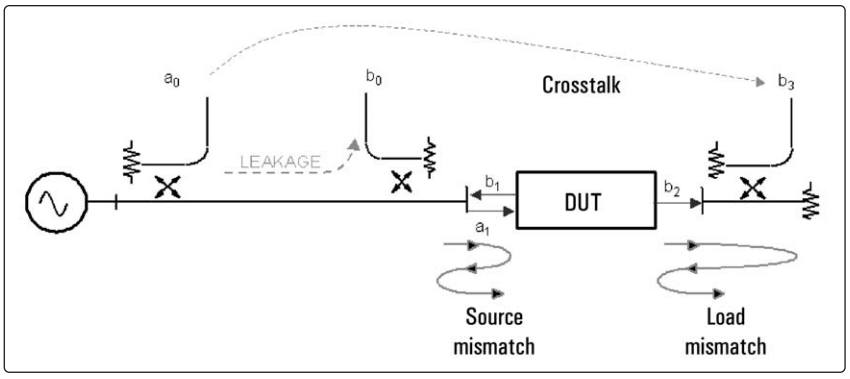

Figure 4. VNA measurement errors.

Vector Network Analyzers with 4 Ports

The four-port VNA shown in Figure 5 has a single swept frequency source that is switched to each port to make a reflection and transmission measurement. The source is sampled by the reference receiver. The switches are set to route the incident signal through the directional coupler to the desired test port. The directional coupler separates the reflected signal from incident signal and switches route the reflected signal to the "A" sampler. The S11 measurement is the ratio of A/R which is equivalent to a TDR measurement in the time domain. Transmission measurements are the ratio of B/R and are equivalent to the TDT measurement. The source reflected and transmitted signals are appropriately routed to complete the set of 16 S-parameter measurements for a 4-port DUT.

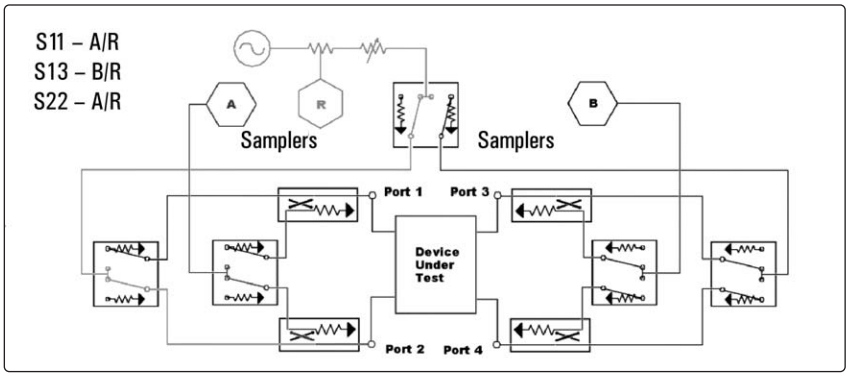

Figure 5. Vector network analyzer Block diagram with 4 ports.

N-Port S-parameters defined

As shown in Figure 6, the S-parameter definition can be expanded to N-ports for multiport applications. Many new high-speed, digital protocols now recommend measurements that require the use of more than four ports, such as differential crosstalk on Serial ATA, PCI-X, HDMI (high-density multimedia interface) and rapid IO. The most efficient way to make these measurements is with a physical layer test system that has more than 4-ports. By implementing this type of measurement technique, all device ports are connected at once for multiple differential channels. For example, a 12-port measurement system can be connected to 3 adjacent differential channels. This facilitates all near-end and far-end crosstalk combinations by eliminating the need to perform multiple calibrations and manage all the S-parameter data. Without the appropriate data management software, this can be an overwhelming task because a 12-port system will produce 144 S-parameters.

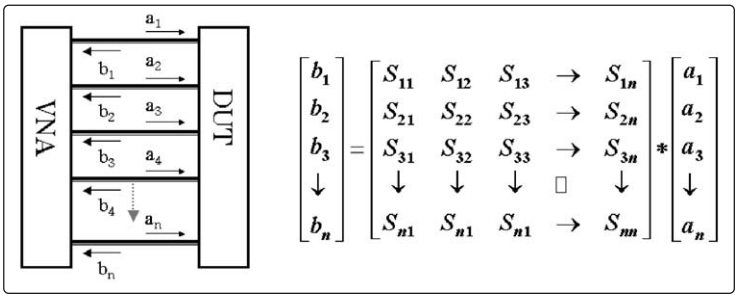

Figure 6. N-Port S-parameters defined.

A Real World VNA Block Diagram Example – The Agilent N5230A

Network Analyzer (Option 240/245)

An interesting example of a real world multiport network analyzer is the Agilent N5230A PNA-L Option 240/245. High-speed digital data transmission is composed of differential signals, so four ports are now a requirement for measuring important performance parameters such as differential insertion loss in interconnects. This 4-port vector network analyzer, shown in Figures 7 and 8, has all of the standard microwave components of a 2-port VNA with inherently lower system noise floor (trace noise of 0.006 dB rms at 100 kHz bandwidth) and higher dynamic range (up to 120 dB at 2 GHz). By utilizing advanced over-sampling techniques, the system architecture enabled a large improvement in stability and drift errors over previous generations of VNAs. High-quality couplers and switches allow for better error correction resulting in very low measurement errors.

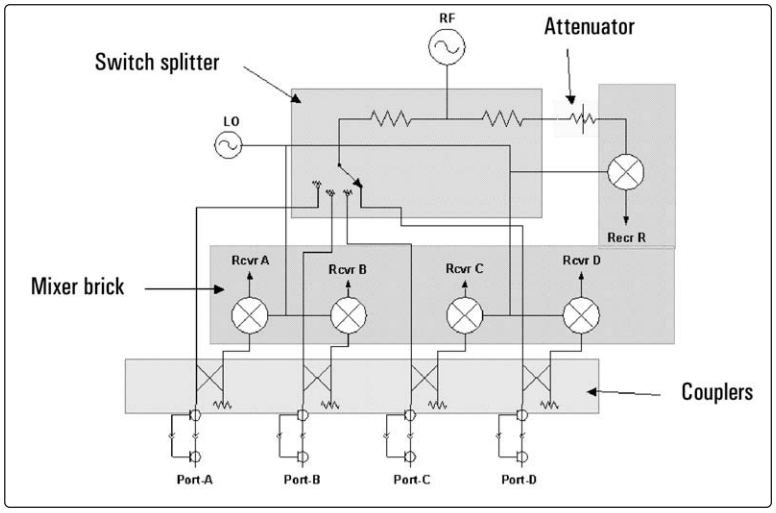

Figure 7. Functional block diagram of 4-port vector network analyzer.

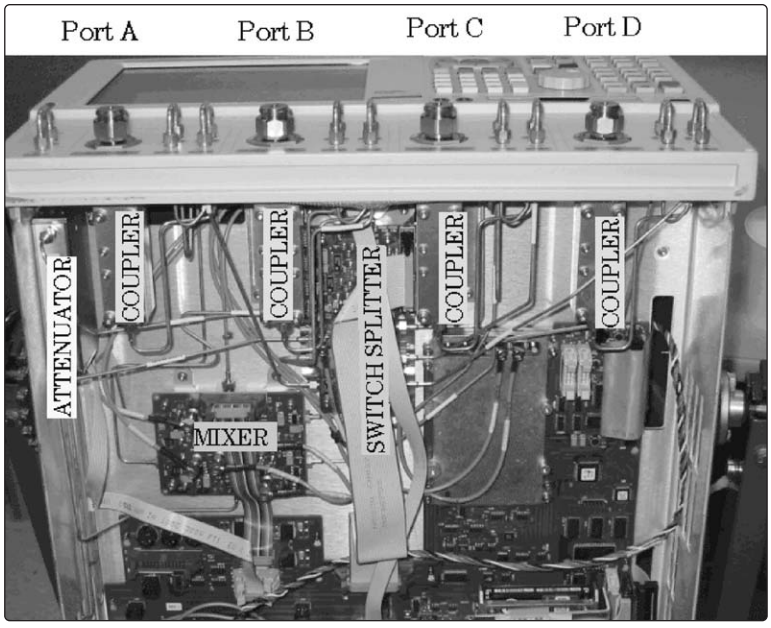

Figure 8. Hardware layout of 4-port vector network analyzer.

Thru-Reflect-Line (TRL) Calibration Types

A major problem encountered when making network measurements in microstrip or other non-coaxial media is the need to separate the effects of the transmission medium in which the device is embedded for testing from the device characteristics. For example, testing a high-speed backplane connector requires the use of PCB test fixtures that adapt the test equipment 3.5 mm connectors to the mated connector pair. While there is a desire to predict how the connector will behave in the environment of its final application, it is difficult to measure without the appropriate test fixture. The accuracy of this measurement depends on the availability of quality test fixtures. Unlike standard 3.5-mm connectorized coaxial measurements, a set of three distinct well-characterized impedance standards are often impossible to produce for non-coaxial transmission media (like the connector). For this reason, an alternative calibration approach may be useful for such applications. The TRL calibration technique relies only on the characteristic impedance of a short transmission line. From two sets of 2-port measurements that differ by this short length of transmission line and two reflection measurements, the full 12-term error model can be determined. Due to the simplicity of the calibration standards, TRL can be applied in dispersive transmission media such as microstrip, stripline and waveguide. With precision coaxial transmission lines, TRL currently provides the highest accuracy in coaxial measurements available today. Many different names have been given to this overall approach: self calibration, thru-short-delay, thru-reflect-line, thru-reflect-match, line-reflect-line, line-reflect-match, quick-short-open-load-thru, short-open-load-reference line and others. These techniques are all variations on the same basic approach and are shown in Figure 9.

Cal Type	2-port Std 1	2-port Std 2	2-port Std 3	Port 1 Std 1	Port 1 Std 2	Port 1 Std 3	Port 2 Std 1	Port 2 Std 2	Port 2 Std 3
TRL/LRL	Thru line		Delay line	Unkn# reflect			Unkn# reflect		
TRM/LRM	Thru line			Unkn# reflect	Match		Unkn# reflect	Match	
TRA/LRA	Thru line		Attenuator	Unkn# reflect			Unkn# reflect		
TNA/LNA	Thru line	network	attenuator						
QSOLT 1	Thru line			short	open	load			
QSOLT 2	Thru line			short		load	short		
QSOLT 3	Thru line				open	load			open
QSOLT 4	Thru line			short		load			load
LRRM	Thru line			Unkn# short	Unkn# open	load	Unkn# short	Unkn# open	
unkn thru (SOLR)	Unknown thru			short	open	load	short	open	load

Figure 9. Various types of TRL calibration variations are used today by microwave engineers around the world.

A Stripline TRL Fixture – A Design Case Study

Many electrical interconnect manufacturers have the need to accurately measure the performance of their devices. The challenge for high-speed, interconnect measurements is to not let the test fixturing itself interfere with obtaining accurate data. Very often, poorly designed test fixtures have poor signal integrity and display excessive impedance discontinuities, high-series loss due to conductor skin effect and high-shunt loss due to dielectric materials. This all translates into a low-bandwidth measurement that makes the interconnect look much different that it is in reality. This design case study will step the reader through the process of creating a TRL standard for avoiding these measurement errors. The authors have purposefully chosen a simple and straightforward tone when describing the methods used, including highlighting the pitfalls. However, great detail is provided in many specific areas. Hopefully, this practical approach will encourage more engineers to experiment with this calibration method and implement it in their next project. Design for testability is a discipline that will reap large rewards if the time investment is made early in the design cycle.

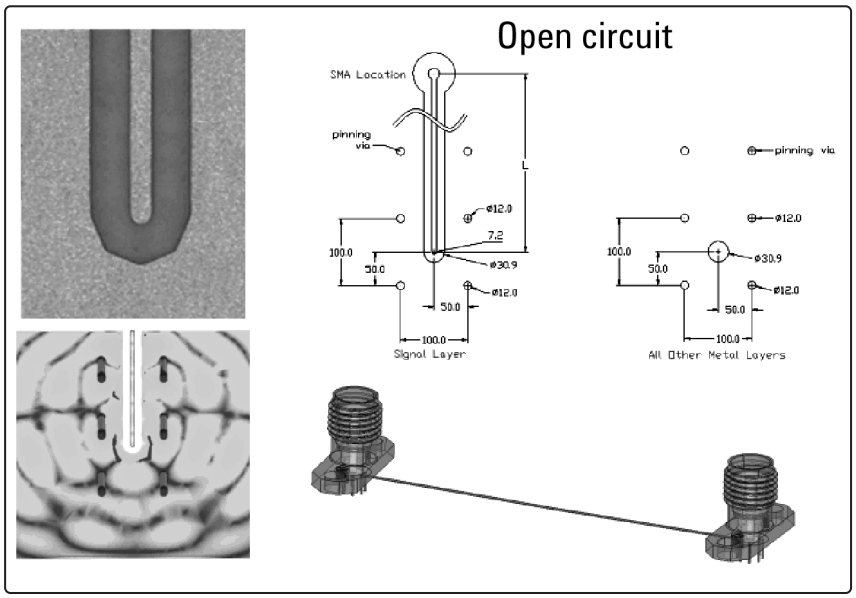

Figure 10. A TRL fixture is designed with the assistance of a three dimensional electromagnetic field solver.

It may be best to consider a TRL design in two parts, macro and micro. In the macro consideration we will look at the design of the PCB, the fixture in general and the TRL portion in particular. In the micro portion we will consider the details that are needed for stripline. Most of the details revolve around how to create a good launch and calibration standards in spite of this feature. First, a little philosophy.

TRL Least Common Denominator, an Open Circuit

We just discussed how calibration removes many types of errors. We can choose to introduce an error and remove it on purpose, as long as the error is systematic and repeatable. One thing we can do with this idea is change the location along the transmission line where the instrument stops and the DUT begins. To do this we simply place our calibration standards at the location where we want to create the instrument-DUT interface. We could, in principle, use SOLT standards, but they are difficult to manufacture in coax with a machine shop. In stripline they will be exceedingly difficult to manufacture to the degree of accuracy needed to allow for a good calibration. Let's use the TRL standards instead, because the electrical characteristics of TRL standards do not need to be precisely known, and they do not need the tight manufacturing controls of a machine shop. We can subject the TRL cal kit to the variation inherent in PCB manufacturing and still achieve a good calibration.

The least common denominator of the fixture and the cal kit is the open circuit. Every element contains at least one of these. For our purposes, the open circuit includes a specific length of stripline, a launch, an SMA, a length of coax and the VNA instrument itself. Because we are going to use the same instrument and length of coax every time, we can forget about these during the fixture design. As long as a torque wrench is used to mate the SMAs, the coax and instrument can be regarded as repeatable. To create the rest of the fixture and cal kit, we are going to keep the electrical characteristics of the stripline, the launch and the SMA the same (as much as possible). To a large degree this translates into keeping the mechanical characteristics of this collection of parts the same each time we create it. This collection of parts can be thought of as a time-domain scope probe. Better still, as a probe station probe. Like a scope probe, this "open-circuit" probe can measure whatever it touches, the cal features, or a DUT. Unlike a scope probe, we don't have the luxury of using the same device every time. A good, high bandwidth, repeatable, design is a must. And unlike a probe, our open circuit probe can't be placed in a random location after the fixture is constructed. It must be placed during the PCB design and layout. Make every open circuit probe the same, as much as possible. This is the part we want to remove from the measurement, either through calibration or through de-embedding. In calibration, we will place the collection of standards at the stripline open circuit probe tip. For de-embedding, this is the collection of parts to model using a 3D-field solver. Another name for the open circuit probe, in the context of measuring the DUT is, "the fixture." See Figure 11.

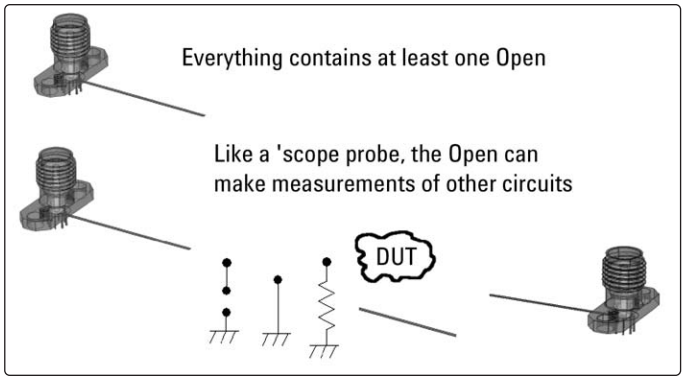

Figure 11. The TRL calibration uses the open circuit standard as a probe.

The Macro Half of a TRL Design

Lets consider the entire PCB for a moment and ask a few questions.

1. What experiments should be conducted? Make sure the fixture allows for the experiments that are required. What non-TRL features need to be included? Make sure that they are included. How many signal layers? How thick should the PCB be? Will a full panel be used or a partial panel? Will the PCB lay flat on the lab bench, or will it be placed in a stand? Fixtures are costly, time consuming to design and manufacture and do not forgive missing features.

2. What material (DK) will be used to construct the fixture? The dielectric constant of the material to be used should be known, because time of flight delays will need to be calculated. A material representative of the finished product is a common choice. Because this division of Molex, Inc. doesn't sell PCBs, we often chose Rogers 4350 to minimize rise times at the DUT. Rogers 4350 is a good material for VNA fixture dielectric use as well. Other dielectrics can be used. If your goal includes system level testing, a dielectric representative of the one used by the system may be a good choice. If the goal is component level testing, a high-performance material is a superior choice because it offers more consistent performance and better repeatability.

3. How far away is the SMA interface from the DUT? Should the board "look" like something else for time domain tests? Are there mechanical considerations that limit SMA location? Generally speaking the closer the SMA-PCB interface is to the intended DUT the better, regardless of which calibration method will be used. Mechanical considerations caused us to place the SMAs about 3.5 inches from a low loss DUT that is only about an inch long. Even so, we believe we obtained good measurement results.

4. What level of performance does the Cal Kit and fixture need to deliver? The expected performance from the cal kit and the bandwidth of the desired data set will drive some compromises into the design. Needless to say, the care and attention to detail needed for a 1-Gb/s design is different than that needed for a 10-Gb/s design. If the measurements will be used for simulations (e.g. scattering parameters used in SPICE) a wider bandwidth measurement than that needed to confirm adherence to a specification may be required.

5. How close to the DUT should the reference plane be? Determine where the reference plane will be placed. The reference plane is a largely arbitrary location along the transmission line from the VNA to the intended DUT. At the reference plane the measurement phase is zero, the gain is zero and the return loss is the same as the noise floor of the measurement. It can be, and often is, placed very close to the intended DUT. The reference plane should be placed along the TEM mode transmission line; don't place it in a discontinuity (E.G. in a via, or a pin, or in an antipad). It may be necessary to leave some of the fixture transmission line in the measurement. As long as the transmission line that is included is understood and recorded, it can be accounted for. Once this location is determined, the actual DUT becomes that thing that is between the reference planes.

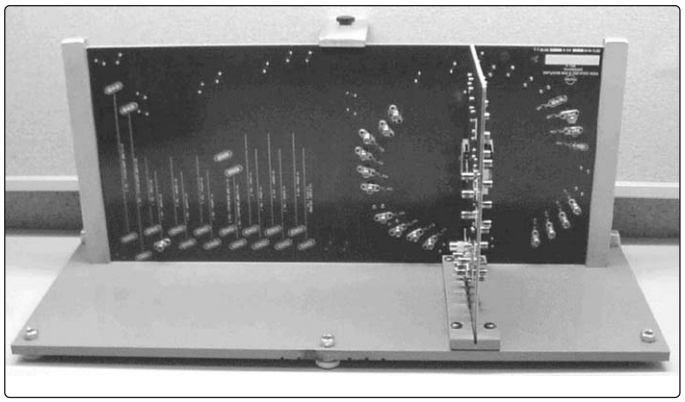

Figure 12. Picture of a test fixture with a TRL calibration kit (left side).

The Macro Element View

We know what experiments and measurements we want to conduct; we know something about the mechanical constraints of the fixture. Now we need a calibration kit to assist with the measurements. Because we just considered the overall fixture constraints we should know where to set the reference plane, and therefore how much transmission line to assign to the open-circuit standard.

A **TRL** calibration kit has four basic elements:

1. **Thru**, this is just a pair of opens, tip of stripline to tip of stripline. A zero length thru is discussed here. This element defines the zero loss, zero phase point. Ultimately, the DUT will be centered in the thru.

2. **Reflect**, an open or a short. This element has to maintain its polarity (sign of the reflection coefficient), but the magnitude of the reflection need not be known. Use the same reflect on each port during calibration.

3. **Line**, it is just like the thru, with an extra piece of transmission line inserted in the center. This extra transmission line needs to 90° long at the center of the frequency band to be covered. The propagation delay of the extra transmission line in each line must be known as well. This element establishes the reference impedance.

4. **Load** (sometimes called match), it serves to cover the bottom most frequency band and relieve the fixture of the need for very long lines. Two are required and each should deliver the same impedance. This element also serves to establish the reference impedance.

The elements listed above are the minimum necessary to construct a broadband, TRL cal kit. A minimal kit, like the one illustrated in Figure 13, might allow calibration from DC to 20 GHz, if the load is carefully designed. Because it is difficult to design a load that works over a broad enough frequency range (DC to 2.5 GHz), it is common practice to employ more than one line in a kit. The lines need to be a quarter wavelength (90°) long, plus or minus a lot, in the dielectric used for the stripline cavity. It may be better to think of them as lengths of transmission line which are NOT integer multiples of a half wavelength (180°) long. It is recommend that we stay 20° or more from the half wavelength point.

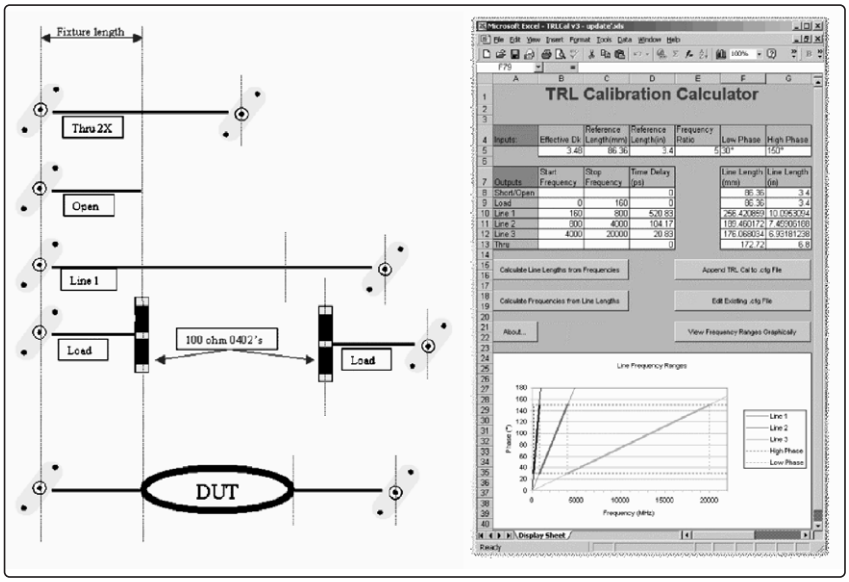

Figure 13. TRL calibration fixture layout with line length calculator. The kit illustrated is the bare minimum needed for a broad band calibration. Often additional lines are required to extend the frequency range.

It turns out that an engineering margin of 20° from a half wavelength is the same as a factor of 8 in frequency range. We might design line-1 to work from 200 MHz to 1600 MHz. The next line, line-2, will need to pick up where the last one left off, 1600 MHz to 12800 MHz. Line-1 would need to be a quarter wavelength longer in the dielectric than the thru at the center frequency (900 MHz), or about 1.639 inches longer if the system is in a DK=4 material. If all this seems complicated don't worry, an example calculation can be found in the "Putting it Together" section on page 16 and there is a calculator available at the web sites referenced in the appendix.

The loads are treated like a very long line by VNA during a TRL calibration. There has to be a pair of them and they are connected instead of a very long line. The first line has to take over where the loads stop working properly. The best way to determine this is to use a full wave field solver and design a high-bandwidth load. It will be apparent where the load starts to show a high return loss, or stops acting like a simple 50-ohm resistor during the design process. My observation has been that a pair of 0402 thin film resistors mounted to a PCB will stop working well between 100 and 200 MHz depending on the system. Turning them on their edge, to reduce capacitance, might allow them to work well to about 1 GHz. Turning 0402 resistors on their side is tedious work, worse, it will yield mixed results. In the *Appendix* at the end of this document, there are URL references which contain a load design to get you started. If a full-wave solver is not in your tool kit, measure the load performance after the board is realized and adjust the design for the next board accordingly. Baring a good load design, do your best and aim low. Even if the load is just a pair of 0402's on a circuit board, it should be possible to reach 20 GHz or more with the three additional lines physical layer test software (N1930A) allows.

Putting it Together

Lets go through an example design.

For this example we will want to test a mated backplane connector pair. The connectors will rest on a PCB constructed with an FR4 core and Rogers 4350 outers. The PCB will be 0.093” thick with the calibrated transmission lines suspended in a Rogers 4350 stripline cavity. Lets place the SMAs 3.500 inches from the intended DUT. Mechanical considerations force this as the minimum distance, if we want to maintain mostly straight transmission lines. This decision results in an arc of SMAs around the intended DUT. Ultimately, we want to test the DUT only, so let’s place the reference plane very close to the connector pins, 100 mil. This means that the open circuit standard will be 3400 mil long. The actual DUT will be a pair of mated connectors with a via and a 100 mil piece of stripline on each side.

The thru is easy to design. Just take two open circuits and connect them, stripline tip to stripline tip. This will define a circuit with two SMA connectors, one at each end of a 6800 mil stripline. The time to propagate a signal through the thru should be exactly the same length of time as it takes to propagate a signal to the end of the reflect and back. In stripline, just flipping the two opens, tip to tip, gets very close. It is likely that no further effort will be required here.

On to the lines and the load. Each line will be incrementally longer that the thru and it will cover some defined frequency band. To avoid the need for a really long line, a load will be substituted. The first line has to take over where the load stops working well. The length of the line is inversely proportional to the band it covers. Lower frequency bands require longer lines that consume more board real estate. Ideally, the load and the lines should be at the same reference impedance, our goal here is 50 ohms. A pair of 100 ohm 0402's placed on the top of a circuit board can stop acting load-like around 100 MHz. This could happen sooner if the via connecting the load has a stub. Some time spent pushing the bandwidth of the loads up will be rewarded with shorter lines and possibly fewer of them. For this example, lets assume we did not optimize the load and that it stops working well at 160 MHz.

Because the load stops at 160 MHz, this first line needs to take over at this point. Lets start our design with a frequency factor of 8. Using this criteria, the first line (line-1) would work from 160 MHz to 1280 MHz. The next one (line-2) would work from 1280 MHz to 10240 MHz. And the third line will work from 10240 MHz to 81920 MHz. This is probably a much higher frequency than needed and higher than most VNAs can cover. Let’s try a factor of 5 instead. The lines now cover the following bands line-1 covers 160 MHz to 800 MHz, line-2 covers 800 MHz to 4000 MHz and line-3 covers 4000 MHz to 20000 MHz. This will give us more engineering margin, without increasing the number of calibration structures that we need to measure. The system set up with a factor of 8 will probably work, but there is less margin for error. If a DK comes out wrong, or a transmission line doesn't come in at exactly the length we wanted etc. the factor of 8 kit may run into trouble.

The lines need to be a quarter wavelength long in the material in which they are constructed. Lets assume DK=4, because it is a common value. Recall, light travels at 299792458m/s in a vacuum. The center frequency of line-1 would be ((160E6+800E6)/2)=480E6. A quarter wavelength in DK=4 dielectric at 480 MHz is, c/f * _ * 1/SQRT(DK) * 39.37 inches/meter = 3.074 inches. Thus, the length of line-1 is 3.074 inches longer than the thru, or 9.874 inches. The VNA will need to know the delay for each line. For our line-1 example this works out to be, (length/c)*SQRT(DK) = 3.074 inch* 84.7 ps/inch* SQRT(4) = 520.7 ps. Make a similar calculation for each of the lines and layout the lines accordingly. See Figure 14 for a complete order, including some extra features for non-TRL calibrations.

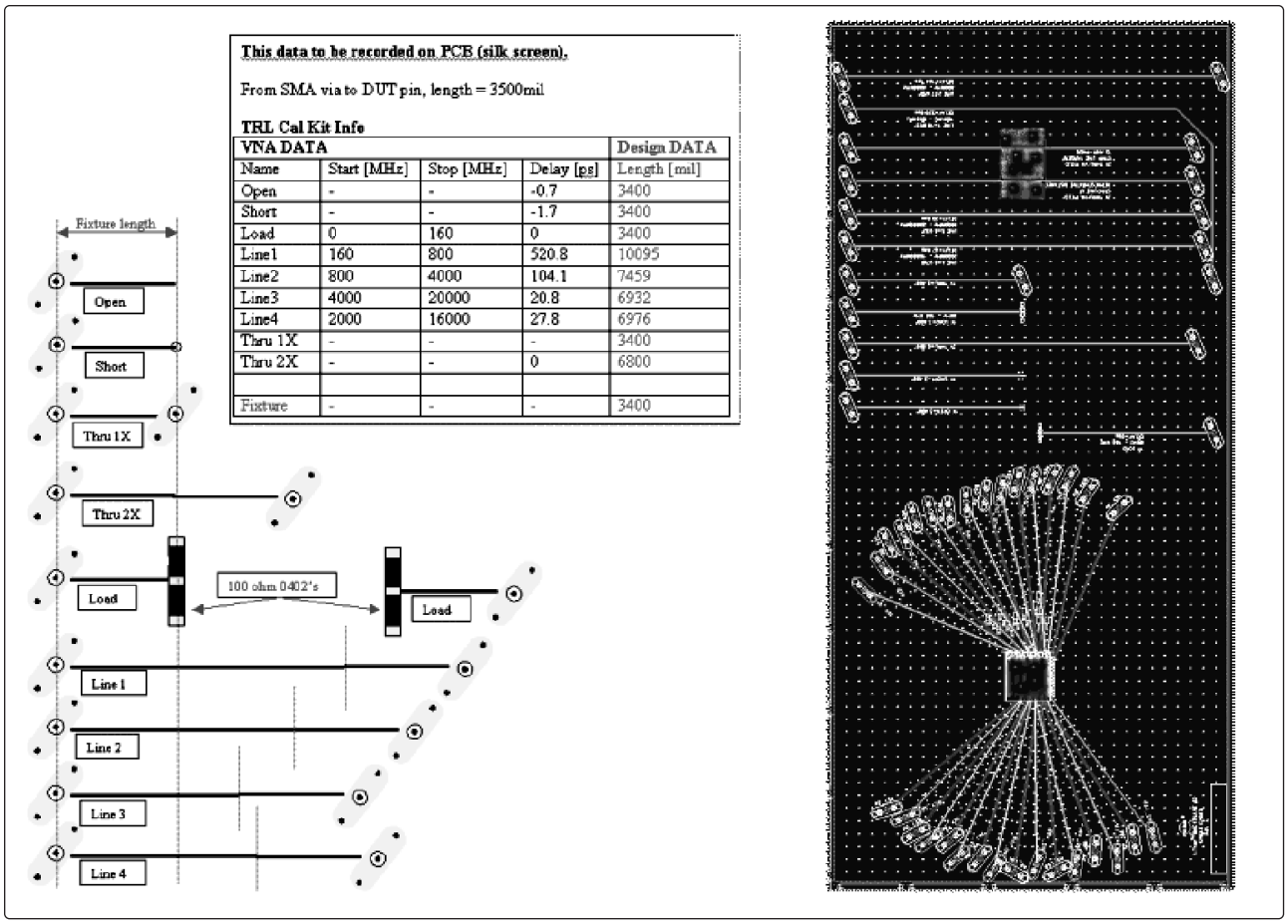

Figure 14. TRL calibration fixture layout order with line lengths (left). CAD illustration of PCB (right). Note that the 1X thru is not needed for the TRL method, it was included for time domain work. Line-4 is part of an experiment to calibrate the VNA using the load up to 2 GHz. To calculate lengths and delays in the table above, DK=3.48 was used.

The Micro half of a TRL Design

From a macro point of view, we're done. The length of all the necessary parts has been calculated and we can move on to layout. If this were coax, we really would be done. But this isn't coax and we are only about half done. It is time to consider the micro half of the problem. This was alluded to in the discussion above about the load and how its performance changes the length, and possibly the number of lines needed to complete a calibration. Stripline is a pretty good transmission line, but it has a significant problem in that it is usually accessed by the use of a drilled, plated through hole; known as a PTH or via. If you're designing for high speed, you're already familiar with the problem. Via stubs create resonances and the location and depth of the resonance changes with the length of the via, the length of the stub, the barrel diameter, the number of pads on the via, the diameter of the pads, the size of the antipads and probably some things we don't keep very good track of, such as the wear on the drill and the amount of etch. Vias are a mess and they are almost always necessary. What to do? The same things we do for any high speed circuit, only more so if we can. If possible, use a full-wave simulator to assist with this (e.g. HFSS or CST). Consider blind, or back drilled, launches and loads. If you want to measure a component placed on the PCB, consider high performance materials and optimized stackups. Yes, it adds cost, but it improves the performance of a PCB that is likely to see a very short run. Remember, one of our goals is to be able to subtract the fixture from the measurement. Removing sources of variability from the fixture will be rewarded by more accurate and repeatable measurements, regardless of the calibration technique used.

PCB launch characteristics

The SMA to PCB interface, the launch, should be as electrically transparent as can be managed and easily reproduced. If the signal is sufficiently attenuated or altered by the launch, no useful measurement will result. If the launch doesn't provide consistent performance, it can't be subtracted through either TRL calibration or de-embedding. There are several papers available on good PCB launch design. Ask your SMA vendor for help, if you need more detail about launch design. If you have time to optimize the performance of only one feature, make it this one. See Figure 15.

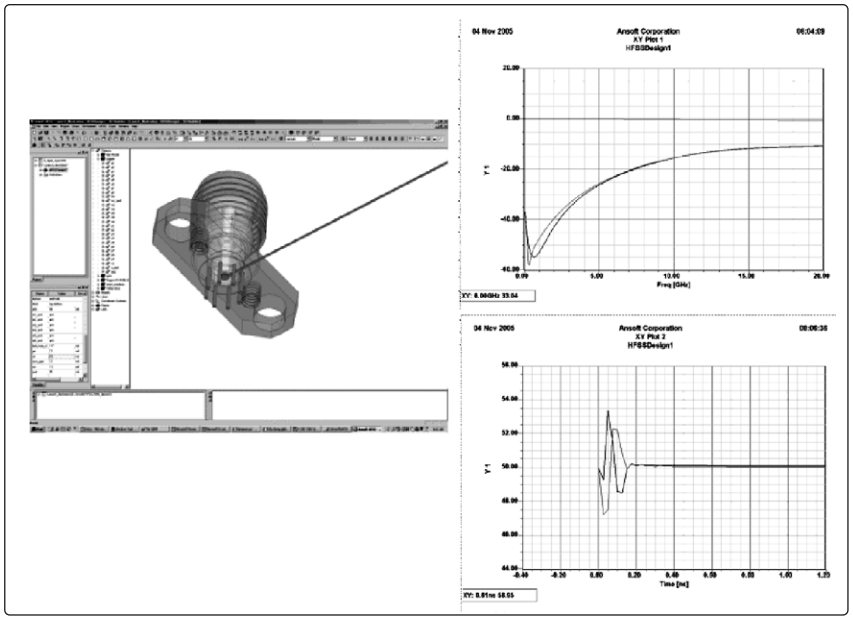

Figure 15. Optimizing the PCB launch is a critical step to successful stripline VNA measurements.

If broadband measurements are desired, an economical way to achieve them is to include a broadband load design. Consider a system with no load. The first line will need to cover 10 MHz – 80 MHz, thus it will need to be about 42 inches long in a DK=3.5 material. The kit will need three additional lines, all of which take up space and all of which need to be measured to perform the calibration. This is a lot of transmission line to place on an 18x24 inch panel. Worse, the top most frequency that can be achieved with a TRL cal kit based on a no-load design is 5 GHz. Not adequate for many of today's designs. An extreme example, yes. Lets consider another extreme example, a load design that works up to 3 GHz. Now the first, and only, line needs to be only about 7 inches long in the same DK=3.5 material. The kit becomes very compact, it is easier to calibrate because fewer connections are needed and the top bandwidth of such a kit is 24 GHz. Ample for many of today's designs and near the limit of APC 3.5-mm connectors. There is a load design on-line, see the "Appendix" at the end of this document for URL information.

Consider the open or short. Is the discontinuity well defined? This is relatively easy to do, but it is worth considering anyway. The location of the reflection from the reflect standard should be well defined, for ease of design and layout. The mechanical length of the reflect should be one half the length of the thru. The reflect must maintain its polarity (sign of the reflection coefficient) throughout the desired bandwidth of the measurement. There is an open and a short design on-line, see the "Appendix" for URL information.

Check (CAD), **Check** (Gerbers), **Check** (Finished Product)! Most CAD packages for PCB layout do not do well with some of the TRL stripline features. The short seems to cause the most grief. It is common for the short to lose its length and become shorted right at the SMA interface. The CAD software apparently believes that there is no difference between a short at the end of a transmission line several inches long and one that has zero length. For this reason, and because the open seems to perform better in simulation, I usually use opens as the reflect standard for stripline. The short isn't the only place where CAD problems arise. Check the Gerbers and the finished product as well. Remember, the goal is to use identical open circuit probes to measure the DUT and the cal kit. If this happens, the open circuit probe can be reliably subtracted from the measurement and the actual DUT can be measured. See Figure 17.

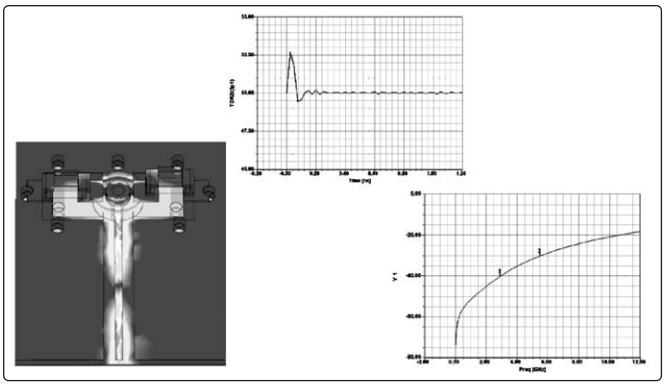

Figure 16. High frequency structure simulator (HFSS) is a powerful tool for load analysis.

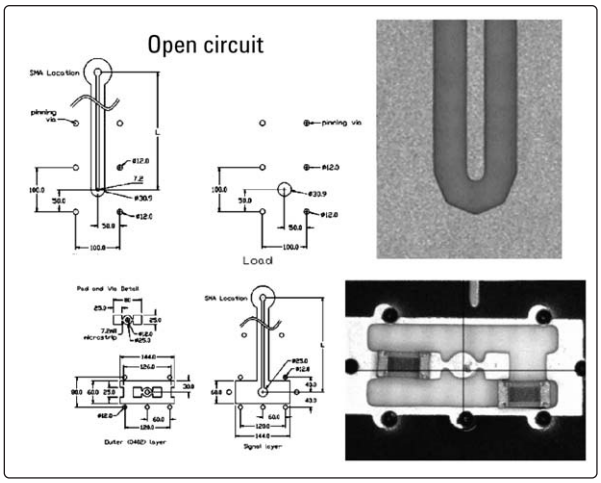

Figure 17. Comparing design intent to realized prototype TRL fixture.

Validation of a TRL Fixture

Lets compare some measurements using a stripline TRL calibration to similar measurements made using the gold standard, an SOLT calibration plus de-embedding. For this comparison a fixture, like the one described in the example above, was employed and both a TRL calibration and an SOLT calibration was applied and measurements taken. In this case, the connector is differential and the TRL calibration reference plane is placed near the point where the transmission lines get close enough together to create a differential mode. This is about an inch from the desired DUT, a mated pair of connectors. For the SOLT calibration, the reference plane was placed at the end of the coaxial cable and then moved to the same place using de-embedding. To de-embed, a scattering parameter set of the item to be de-embedded must be created. To do this an HFSS simulation of the open circuit probe was created and a scattering parameter set extracted. Now we should have two data sets which are comparable.

The first pass doesn't look good. See Figure 18. At 1 GHz the delta between a TRL calibration and an SOLT plus de-embedding is 0.29 dB, at 7 GHz it is 1.17 dB. Where did we go wrong? The piece to be de-embedded, our open circuit probe, was carefully modeled using HFSS. Dimensions were double checked and confirmed correct. Upon measuring the dielectric properties of the material used, we realized that the DK and DF varied from the advertised values by a fairly large margin. DK was off by 10% and DF was off by more than 100%. To obtain the actual DK and DF values, two lines of different length (the thru and line-1) were measured using an SOLT calibration. The group delay and loss values were subtracted to obtain time of flight and loss per unit length. Using these values, new DK and DF parameters were found. Applying a TRL calibration and measuring the delay and loss in line-1 directly confirmed this. Lesson learned, don't count on the vendor for actual DK and DF values. Measure them yourself.

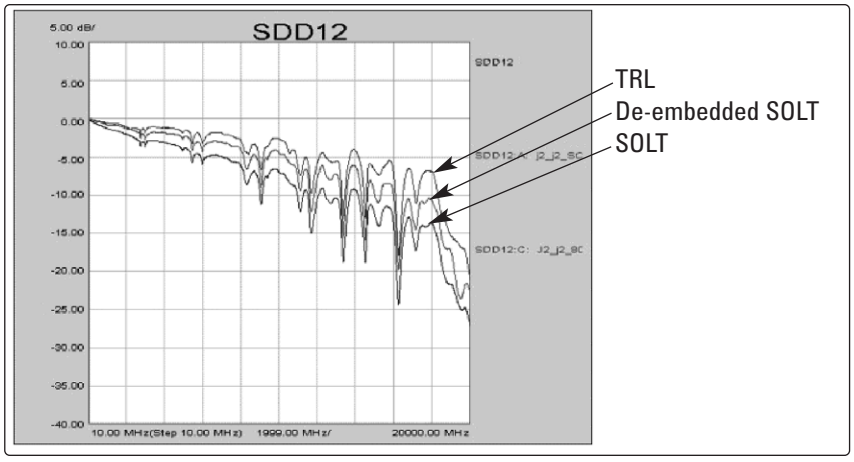

Figure 18. First pass doesn't compare TRL and SOLT plus de-embedding well.

Using the Corrected Material Properties

The new material properties entered into the HFSS simulation for our open circuit probe and scattering parameters were extracted for entry into PLTS. This resulted in curves that correlated very well in the forward direction and pretty well in the reflected direction. The insertion measurement shows the de-embedded curve resting just below the TRL derived curve. A closer examination of material properties might help to bring these even closer together. We used a single value for DK and DF, even though the measurements made it clear that they are frequency dependent. Copper parameters were assumed to be textbook. See Figure 19.

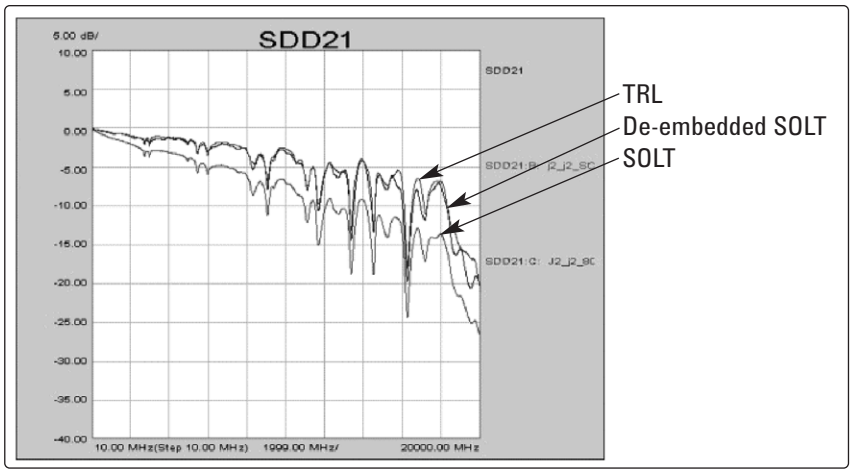

Figure 19. Applying correct dielectric constant of PCB material shows correlation between de-embedded SOLT and TRL.

Near-end crosstalk characterization

What about near-end crosstalk (NEXT)? This is a more difficult measurement to make than insertion loss. An adjacent pair of pins was selected and a NEXT measurement was obtained. These curves match up very well, in insertion loss, in group delay and in the time domain. See Figure 20.

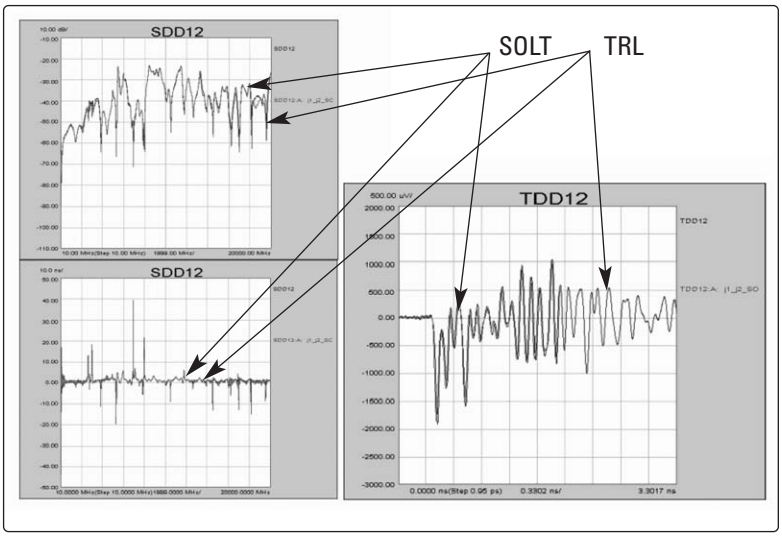

Figure 20. Near end crosstalk analysis shows good correlation.

Far-End Crosstalk Characterization

How far can we push the forward direction? A pair of pins on the diagonal was selected and forward-end crosstalk (FEXT) was measured. We see correlation in the scattering parameters all the way down to the noise floor. Insertion loss, group delay and time domain all correlate. See Figure 21.

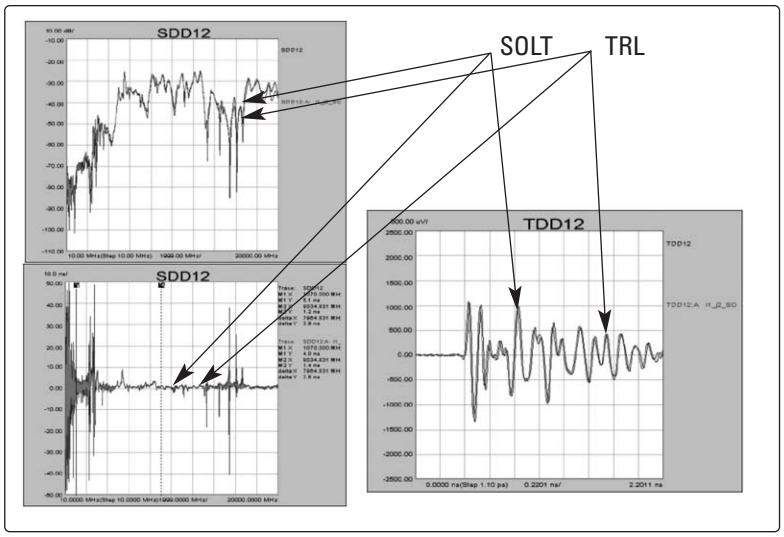

Figure 21. Far-end crosstalk analysis shows good correlation.

Finally, lets compare the reflections. A pair of pins was selected and the reflect direction was examined. Correlation is good, but not as good as in the forward direction (Figure 22). Impedance measurements of the actual DUT varied by 2-3 ohms and the return loss curves to do not show the near perfect overlap that the forward direction curves do. The cause of this variation is not fully understood, but it could be due to inaccuracies in the open circuit probe model that was de-embedded. Or it could be due to imperfections in the TRL cal kit or fixture. Another source of variation is the impedance standard. For the SOLT calibration it was a broadband coaxial standard. For the TRL calibration it was a resistive load and the characteristic impedance of the lines. In any case, the correlation between these two methods is quite good.

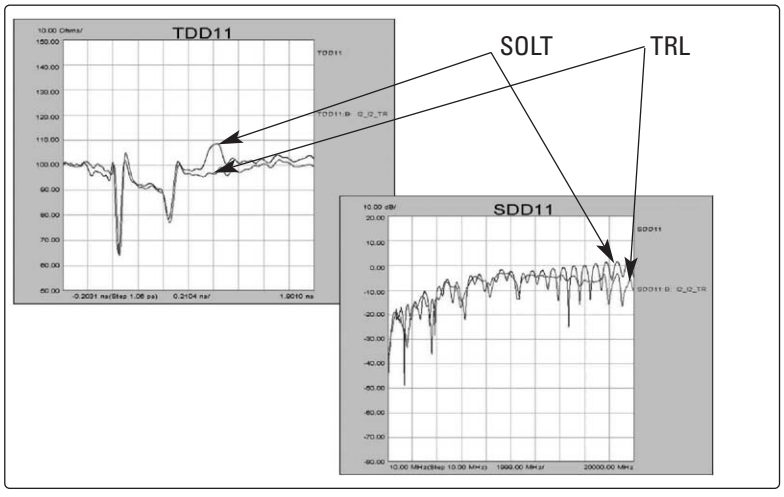

Figure 22. Anomalies in the reflect direction.

Conclusion

Both techniques showed very good correlation in the forward direction, from 0 dB down into the noise floor of our techniques (~-50 dB to -80 dB). The reflect direction was not as satisfactory, but correlation was still good. To design the TRL cal kit, it was necessary to spend some time with a full-wave solver and design a launch and a load. Because this was done, scattering parameters for the open circuit probe could be obtained and de-embedding done. To obtain correct material properties for the SOLT de-embedding it was necessary to include and measure some of the TRL cal kit features (the thru and line-1 were measured). A well designed and implemented TRL cal kit will allow both de-embedding and TRL to be easily used. Ideally, TRL and SOLT de-embedding reinforce each other. Either measurement would result in a very good set of data for compliance testing or SPICE simulations.

It is worth noting that the TRL cal kit was designed using the same erroneous DK value that caused de-embedding to fail. We didn't need to know much about DF to design the kit, only that it is low. The extra margin we gave ourselves by using a factor of 5 instead of a factor of 8 was sufficient to ensure that the lines portion kit still worked in a different dielectric than was planned for. By measuring the TRL standards, the loss and phase of the fixture (the open circuit probe) was taken into account with no further effort on our part. Conversely, if we didn't see the disparity between the SOLT plus de-embedding measurement and the TRL measurement, the dielectric properties might not have been measured and an erroneous measurement could have been reported. It is easier to obtain a good measurement with TRL than by de-embedding an SOLT measurement. The flexibility of reference plane placement is a very welcome feature as well.

Appendix

Additional material, including detailed drawings of various components, a TRL calculator and HFSS simulations, can be found at:

www.agilent.com/find/plts

www.sun60.com/TRL2006

www.molex.com/vnatrl.html

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Dave Dunham, Electrical Engineering Manager, Molex, Inc
Dave Dunham is responsible for high-speed development of backplanes, board-to-board and I/O interconnect solutions.

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