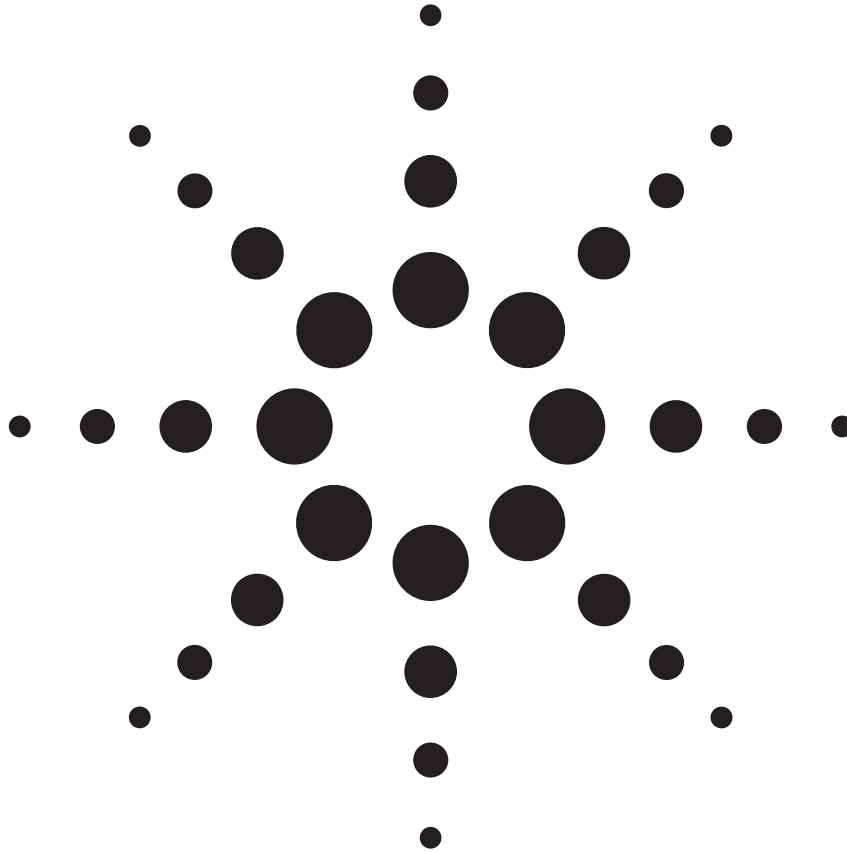


# Agilent Triggering the N6030A Arbitrary Waveform Generator

Application Note



## **Overview**

The N6030A has four hardware trigger inputs that can be used to alter the behavior of the internal sequencer based on externally generated events. In this application note, we discuss the behavior of synchronous and asynchronous trigger inputs in terms of the latency and repeatability of triggered waveform events.

For an overview of trigger operation including selecting between trigger inputs and setting the trigger threshold, polarity and delay, please refer to the N6030A User's Guide, Section 3, page 43.

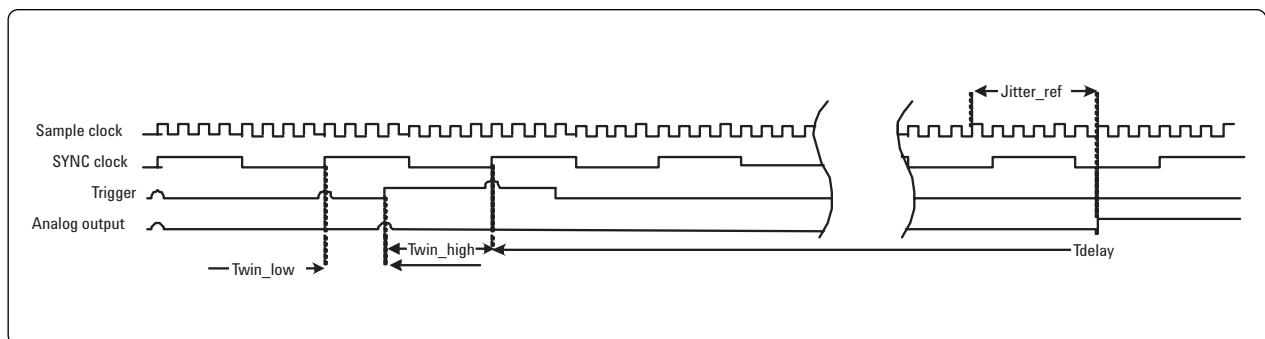
## Synchronous Triggers

Triggers are registered into the N6030A using the SYNC clock. The SYNC clock is nominally at the sample clock frequency divided by 8. However at lower sample rates an internal variable modulus prescaler selects other binary divide ratios: 4, 2, and 1. In general the SYNC clock frequency is always in the range of 78.13 MHz to 156.25 MHz. So the input clock frequency ranges and prescaler divide ratios are as specified in Table 1.

**Table 1. SYNC Clock frequency ranges**

Frequency Range	SYNC Clock Prescaler Divide Ratio
625 MHz - 1.25 GHz	8
312.5 MHz – 625 MHz	4
156.25 MHz – 312.5MHz	2
100 MHz – 156.25 MHz	1

It is necessary to ensure that the correct timing relationships are achieved to guarantee consistent synchronous trigger operation. The trigger input must occur within a valid window with respect to the SYNC clock. The window is specified by two times:  $T_{\text{win\_low}}$  - the minimum trigger delay after the prior SYNC clock edge; and  $T_{\text{win\_high}}$  - the minimum trigger setup before the next SYNC clock edge. These are specified for the trigger Input relative to the SYNC clock Output. The trigger must be a minimum of one SYNC clock cycle long. The trigger timing is specified relative to the rising edge of the SYNC clock. The analog output from the N6030A is then produced a fixed number of sample clock cycles (plus a small fixed propagation delay) after the first rising edge of the SYNC clock after the trigger goes active. Since the analog output is retimed by the sample clock, the reference for jitter measurements is the sample clock. This timing is shown in Figure 1.



**Figure 1. Synchronous trigger timing diagram**

## Synchronous Trigger Jitter

The input trigger is retimed first by the SYNC clock and then finally by the sample clock. It is important to consider carefully how the timing of the ultimate analog output is related to these three signals. As long as the trigger input meets the valid timing window of the input register clocked by the SYNC clock, the exact position of the trigger input in time (within that one SYNC clock period) will have no impact on when the analog output is produced. This synchronous trigger will then effect the desired change in the sequencer operation, such as starting or stopping the output waveform. The sequencer points to particular sample values in the waveform memory that are then fed to the high performance Digital to Analog Converter (DAC). The DAC produces the desired analog output current. The DAC output is retimed in a very low jitter (low phase noise) analog retimer, clocked by the sample clock. Any jitter in the analog output is specified relative to the sample clock. This can be either specified in terms of phase noise or jitter.

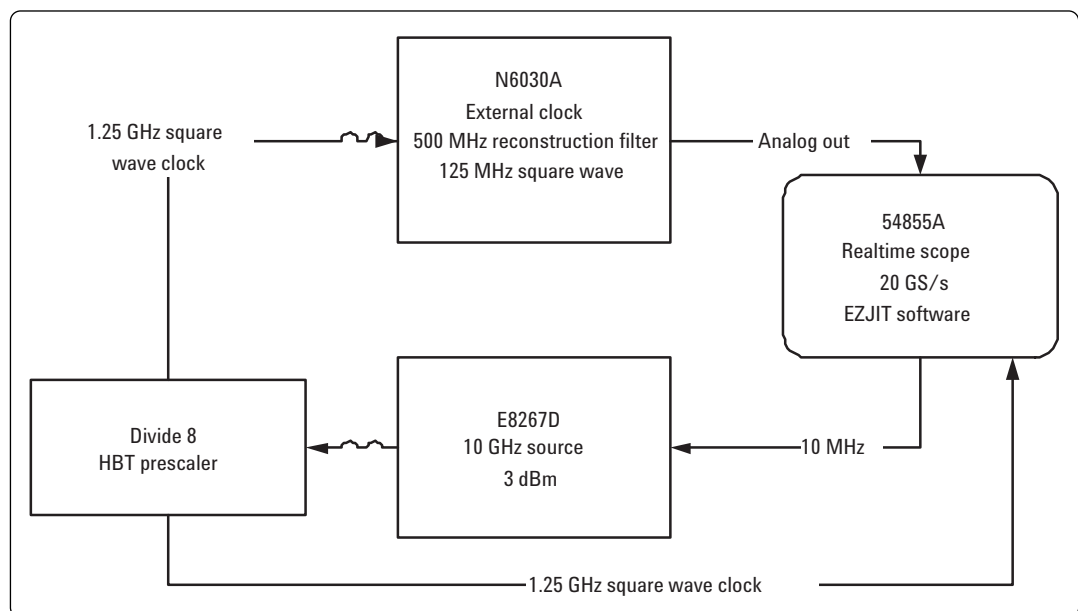
Both the internal clock source and the DAC output have exceptional phase noise performance. With the internal clock, the N6030A has a specified phase noise floor of  $-150$  dBc/Hz. Typical performance is  $-155$  dBc. If an external clock source is used, similar performance can be achieved provided the external clock source has comparable noise performance. The jitter can be estimated by integrating the phase noise over the bandwidth of the reconstruction filter being used. Since little energy is located close to the carrier (relative to the total 500 MHz modulation bandwidth of the N6030A, the close in noise has a very small bandwidth of  $\sim 1$  MHz), the noise floor of the N6030A dominates the jitter calculation. The precise scaling of the phase noise integral to derive time domain jitter is well known. For the case of the N6030A with 500 MHz bandwidth and  $-150$  dBc noise floor, the calculated jitter of a sine wave at, for example, 400MHz is 400 fs (0.4 ps).

In general, low level discrete spurious signals in the output will not significantly change a time domain measurement of jitter. Harmonic spurious causes slight waveform distortion, not jitter. Nonharmonic spurious causes bounded periodic jitter, for example, sinusoidal jitter. Since unbounded Gaussian random jitter continues to grow the longer a measurement is made on an oscilloscope, it dominates. A typical rule of thumb for an oscilloscope measurement is that the peak-to-peak random jitter is approximately ten times the RMS random jitter. In the case of the N6030A this is at least 4 ps pk-pk. The nonharmonic spurious is less than  $-65$  dBc or about 1 part in 2000 in voltage. Since the risetime of the N6030A is on the order of 1 ns, the bounded periodic jitter caused by the nonharmonic spurious will be less than 1 ps. It will typically not be possible to discern this without looking at the jitter spectrum either by using an FFT or a spectrum analyzer.

Measuring the phase noise is relatively straightforward. One method is the recently introduced E5052A Signal Source Analyzer. It is possible to demonstrate the synchronous trigger performance by triggering between two waveforms. Each consists of alternate cycles of a sine wave with zeros in between. If only one of these waveforms is played, large spurious signals are observed in the spectrum, due to the chopped output. If properly triggered with an external synchronous trigger, the resulting waveform will be a complete sine wave with no gaps. This sine wave can be measured with the E5052A and the phase noise shown to be unchanged. This demonstrates low jitter, but not in a way that most users are accustomed.

Most users are interested in a direct measurement of the jitter performance in the time domain. In this case, oscilloscope measurements will limit the jitter performance that can be demonstrated. Still the measured performance is more than adequate for most practical applications. For a time domain measurement, a square wave output is used to measure the edge jitter. Variations in the N6030A output are basically amplitude errors that are interpreted as time errors based on the risetime of the signal being measured. A faster risetime gives a better jitter measurement. Fortunately the N6030A has both wide bandwidth and very low noise so that the overall jitter performance is excellent. For best results, the oscilloscope is triggered on the sample clock. Since the 54855A real-time oscilloscope can trigger with lower jitter on a clock signal with a faster risetime, an external clock (with faster risetime) is used. This clock is produced from a high performance divide by 8 prescaler driven by a 10 GHz microwave signal from an E8267D source. A prescaler evaluation board that can be used for this purpose is the HMMC-3128 which can be purchased through the Agilent web site at <http://www.agilent.com>. This produces sharper edges than the internal source in the N6030A, which makes it easier to trigger the 54855A, with lower jitter.

An N6030A waveform of a square wave at 125 MHz is produced using the internal 500 MHz reconstruction filter and the external 1.25 GHz sample clock. The 54855A is also triggered on the 1.25 GHz sample clock. The EZJIT software in the 54855A analyzes the square wave as a series of data transitions (looking only at rising edge transitions). The two-source Setup Time Analysis of the EZJIT then gives a measure of the jitter performance of the square wave relative to the sample clock. Applying a low-pass filter to the square wave data will smooth it, since the 54855A is over-sampled (at 20 GSa/s) for the N6030A output bandwidth (500 MHz). Phase locking the 54855A to the E8267D using the 10 MHz reference, slightly reduces the 54855A jitter and was done in these measurements. The measurement setup is shown below in Figure 2.



**Figure 2. Jitter measurement setup**

In Figure 3 the 125 MHz square wave is shown. The uncorrected edge response of the 7-pole elliptic reconstruction filter is evident. Trace #1 shows the reduction in trace noise produced by a digital Thompson Bessel low-pass filter function with 1 GHz bandwidth in the oscilloscope. Since high frequency trace noise will produce jitter inversely proportional to the rise time of the analog waveform, reducing the trace noise with a digital filter should also reduce the measured jitter. Unfortunately, to use the EZJIT software the digital low-pass filter function had to be turned off. Hence, the digital low-pass filter was not employed in the final measurements shown below (even though it would reduce the overall jitter noise floor – so the jitter measurements described below are conservative). The 1.25 GHz input clock is shown as noted.

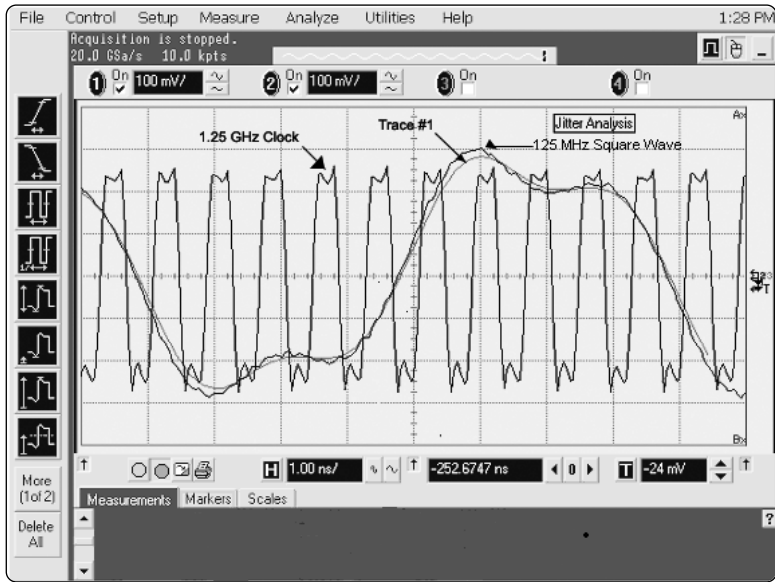


Figure 3. Full scale analog 125 MHz square wave and 1.25 GHz clock from the prescaler

In Figure 4 the vertical sensitivity is increased to lower the jitter noise floor. The two input setup time measurement of the 125 MHz square wave relative to the 1.25 GHz clock is performed with the EZJIT software (without the digital low-pass filter). The RMS jitter of  $\sim 4$  ps is shown. This jitter is dominated by the vertical sensitivity (noise) of the 54855A in the full 8 GHz bandwidth, and scope trigger jitter. Jitter on the clock trigger of 1.5 ps (much faster risetime) is also shown. While clearly oscilloscope limited, this time domain measurement shows the N6030A trigger jitter is less than 4 ps RMS.

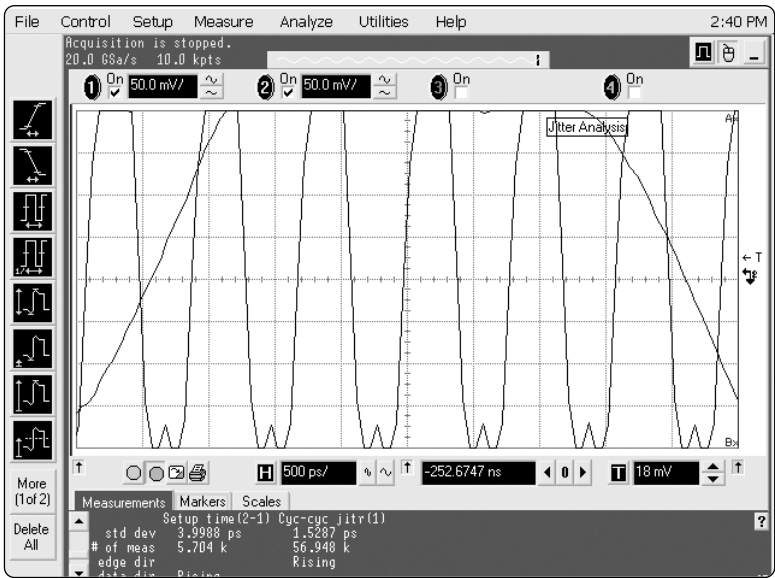
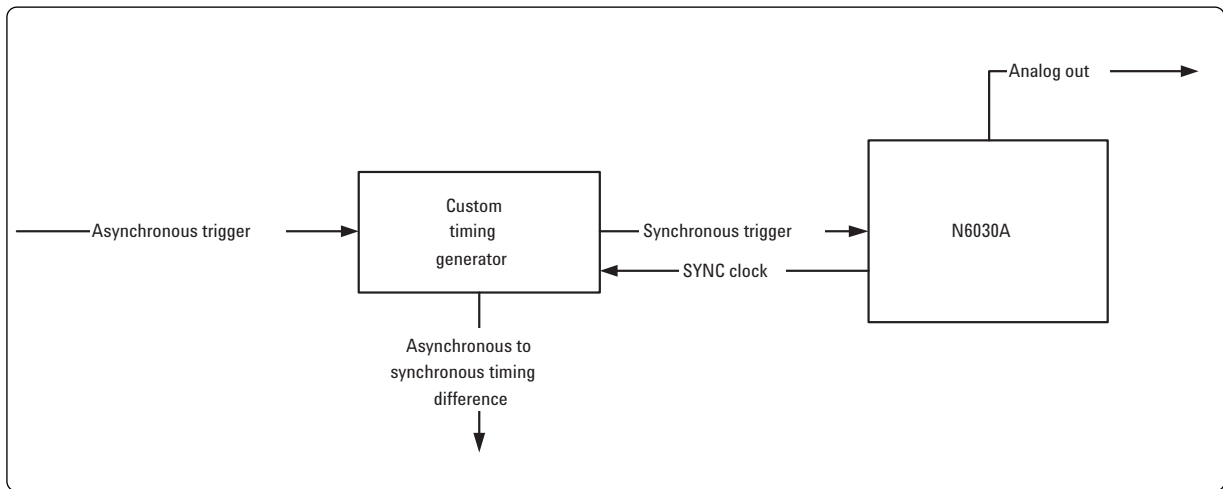


Figure 4. EZJIT jitter measurement showing  $\sim 4$  ps RMS triggered jitter

## Asynchronous Triggers

If the input trigger is not synchronized to the SYNC clock, the trigger uncertainty will generally be one SYNC clock cycle. This is due to having no knowledge of where in the SYNC clock period the trigger arrives (as shown in Figure 1). Worst-case, due to meta-stability in the input register, an additional SYNC clock cycle of timing error could be observed.

For certain applications, the following circuit can be employed to force an N6030A trigger event at a known time near that requested by an asynchronous trigger. The circuit shown in Figure 5 generates a synchronous trigger from the asynchronous trigger event and also logs the time difference between the two triggers. Then by knowing the deterministic synchronous trigger latency of the N6030A, the waveform trigger time can be known precisely.



**Figure 5. Custom timing generator to work with asynchronous triggers**

## Conclusions

The N6030A is capable of deterministic waveform sequencer operation while responding to externally supplied hardware triggers. The most reproducible, low jitter, operation is produced using synchronous triggers. Jitter below 1 ps RMS can be produced with a low noise sample clock source and a synchronous trigger. However at present, time domain measurement issues limit the demonstration of the jitter to 4 ps RMS. Due to these jitter measurement difficulties, the jitter specification is set at 50 RMS, even though typical operation is almost 2 orders of magnitude better. In practice, the typical N6030A synchronous jitter performance exceeds that required by even the most demanding time domain applications.

Asynchronous trigger jitter is more challenging. Users can supply a Custom Timing Generator circuit that makes it possible to generate a triggered waveform at nearly the time requested by an external asynchronous trigger. A correction signal from the Timing Generator makes it possible for the user to adjust for the known deterministic timing errors in the system.

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