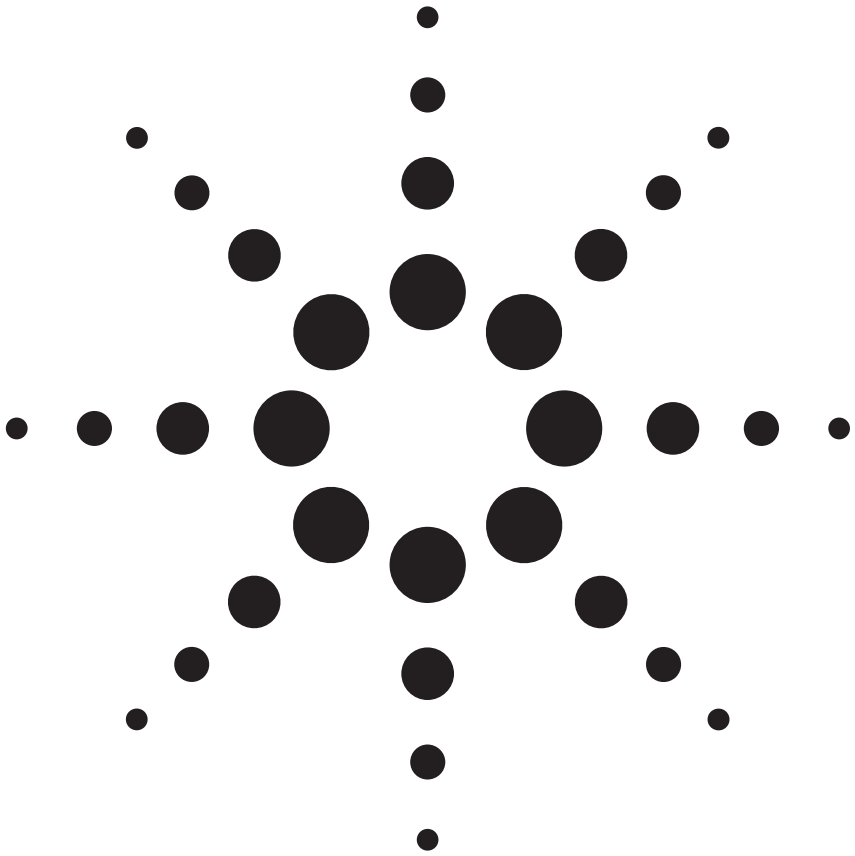
Agilent
Trigger and Marker Interfacing on the N6030A

Application Note



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Overview

The N6030A has four hardware trigger inputs that can be used to alter the behavior of the internal sequencer based on externally generated events. In addition there are four Marker outputs that can be used to control external hardware. The trigger inputs and marker outputs are all clocked synchronously with respect to the SYNC clock.

In this application note we describe how to configure the triggers including the driving source termination and N6030A input trigger threshold values for several different logic families. In addition, the timing of the trigger inputs and marker outputs relative to the SYNC clock is specified.

Synchronous Trigger Timing

Triggers are registered into the N6030A using the SYNC clock. The SYNC clock is nominally at the sample clock frequency divided by 8. However, at lower sample rates, an internal variable modulus prescaler selects other binary divide ratios: 4, 2, and 1. In general, the SYNC clock frequency is always in the range of 78.13 MHz to 156.25 MHz. The input clock frequency ranges and prescaler divide ratios are as specified in Table 1.

Table 1. SYNC Clock frequency ranges

Frequency Range	SYNC Clock Prescaler Divide Ratio
625 MHz - 1.25 GHz	8
312.5 MHz – 625 MHz	4
156.25 MHz – 312.5MHz	2
100 MHz – 156.25 MHz	1

It is necessary to ensure that the correct timing relationships are achieved to guarantee consistent synchronous trigger operation. The trigger input must occur within a valid window with respect to the SYNC clock. The window is specified by two times: Twin_low - the minimum trigger delay after the prior SYNC clock edge; and Twin_high - the minimum trigger setup before the next SYNC clock edge. These are specified for the trigger *Input* relative to the SYNC clock *Output*. The trigger must be a minimum of two SYNC clock cycles long. The trigger timing is specified relative to the *rising* edge of the SYNC clock by default, as shown in Figure 1. To guarantee proper synchronous trigger operation with arbitrary length cables, it is possible to configure the trigger inputs to register the trigger event with respect to the *falling* edge of the SYNC clock, under software control. In this way there is always a setting for the trigger input timing which will operate reliably for any chosen cable. The typical specifications for the trigger window using the internal clock at 1.25 GS/s is (these values will vary at other clock frequencies):

- Twin_high > 3.4 ns
- Twin_low > –2.8 ns (the trigger can occur slightly *before* the prior SYNC clock edge)

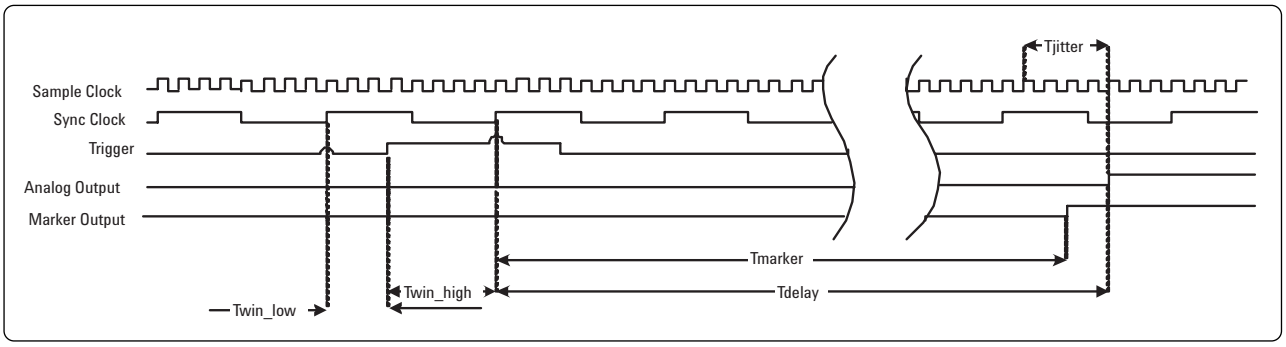

Figure 1. Synchronous trigger timing diagram

These values are measured at the front panel of the N6030A. One method of measuring this is to use a splitter on the output of the pulse generator driving the trigger input and to also run this into an oscilloscope. A third cable connects the SYNC clock output of the N6030A to a second oscilloscope channel. These three cables are of matched length, as shown in Figure 2. A 50 Ω oscilloscope input should be used for the SYNC clock. The trigger input of the N6030A is high impedance, so the input impedance of the oscilloscope should be chosen depending on the driving impedance of the pulse generator that is employed.

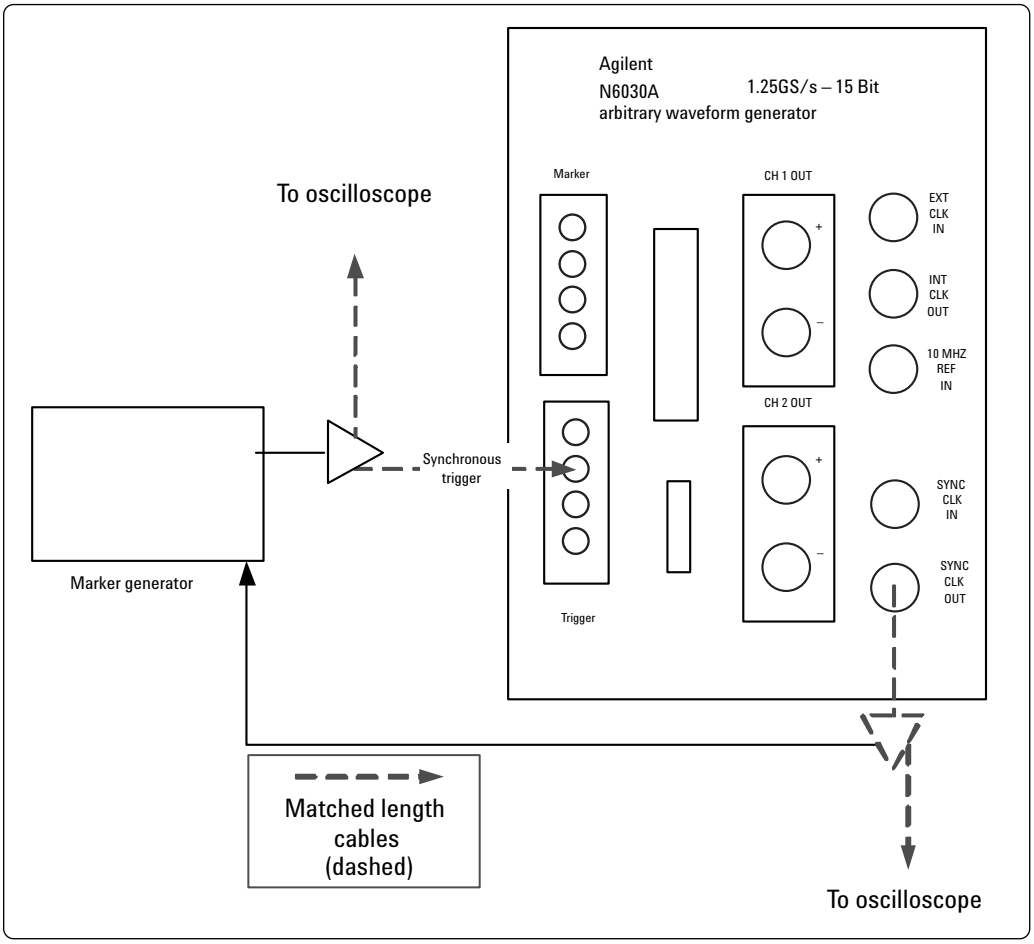

Figure 2. Trigger input timing measurement

Triggered Waveform Latency

The N6030A trigger latency is a combination of a number of sample clock cycles plus an additional fixed propagation delay to the output. As a consequence the latency, Tdelay, in Figure 1 varies with sample clock frequency and also output filter setting. A variable trigger delay can be added in integer number of SYNC clock cycles, although this capability is only supported in the IVI-C driver and not the GUI. In addition, the IVI-C driver supports clocking on either the rising or falling edge of the SYNC clock, while the GUI sets the rising edge. A nominal trigger delay of 0 is assumed in the specifications described below. Using the internal clock at 1.25 GHz and the differential through path, the waveform latency from the rising edge of the first SYNC clock after the trigger to the analog output:

Tdelay (diff_through) = 144.7 ns

This nominal delay will vary as a function of the analog path chosen, as given in Table 2.

Table 2. Output latency variation with output path

Path	Delay (ns)
Differential Through	0
Differential 500 MHz	2
Differential 250 MHz	3.5
Single-ended, no amplifier, Through	0.5
Single-ended, no amplifier, 500 MHz	2.3
Single-ended, no amplifier, 250 MHz	3.8
Single-ended, with amplifier, Through	0.8
Single-ended, with amplifier, 500 MHz	2.8
Single-ended, with amplifier, 250 MHz	4.2

Marker Output Latency

The N6030A marker latency is a combination of a number of sample clock cycles plus an additional fixed propagation delay to the output. As a consequence the latency, Tmarker, in Figure 1 varies with sample clock frequency. In addition, a marker delay can be added in integer number of SYNC clock cycles, although this capability is only supported in the IVI-C driver and not the GUI. The default delay in the GUI is 14 SYNC clock cycles. A nominal trigger delay of 0 is assumed in the specifications described below. Using the internal clock at 1.25 GHz, the marker latency from the rising edge of the first SYNC clock after the trigger to the marker output:

Tmarker = 62 ns

Since the marker delay is less than the analog output delay, the marker output will in general precede the analog output unless marker delay is added. The marker has ~ 100 ps RMS jitter and hence may not be the best choice for triggering for very low output jitter measurements.

Trigger Input Levels

The N6030A trigger inputs are high impedance with a user settable input threshold. With proper trigger source termination, this versatile trigger input makes it possible to interface to a wide range of logic families including: PECL, LVPECL, TTL, and LVTTL. In addition, other non-standard logic types can be accommodated in many cases. Note that because the trigger input has ~2 kΩ impedance, the voltage received will be twice that programmed into a 50 Ω source (such as a pulse or function generator). So, for example, to set an output high voltage of 3 V into the trigger input, the pulse generator should be set to 1.5 V.

Source termination

The N6030A trigger input is high impedance. Hence, to avoid multiple reflections when cabled in a 50 Ω system, a 50 Ω source impedance is required. In most cases this is accomplished with a 50 Ω series termination in the driver. The N6030A Marker outputs use a 30 Ω series termination as a compromise that can drive both high impedance and 50 Ω loads. A generic output driver circuit is shown in Figure 3.

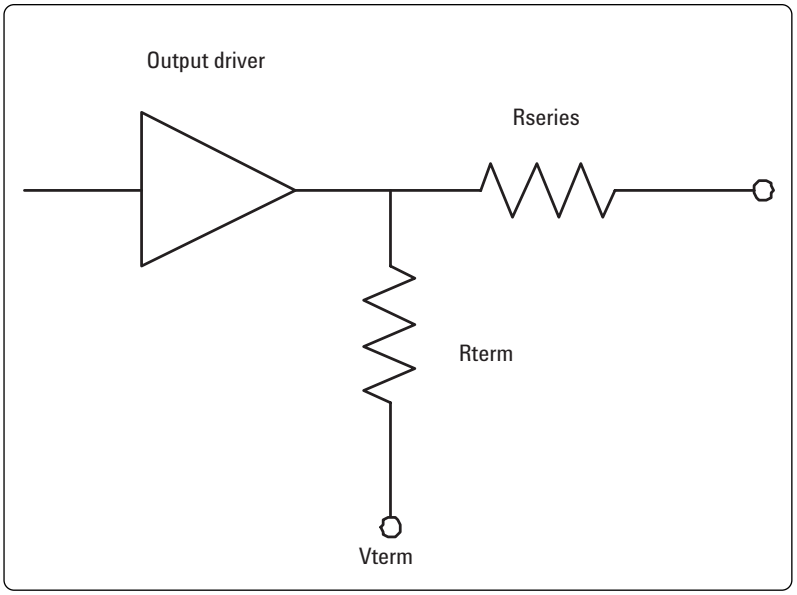

Figure 3. Generic output driver diagram

The suggested values for the user's driving circuit, as well as the trigger threshold voltage to be programmed into the N6030A, are given in Table 3 for a variety of standard logic types.

Table 3. Trigger input threshold and output driver component values

Logic Family	Vlow	Vhigh	Rseries	Rterm	Vterm	Trigger Threshold
LVTTL	0.8 V	2.4 V	46.4 Ω	Open	None	1.2 V
TTL	0.8 V	4.6 V	46.4 Ω	Open	None	2.4 V
LVPECL	1.6 V	2.3 V	46.4 Ω	121 Ω	0 V	2.0 V
PECL	3.2 V	4.0 V	46.4 Ω	273 Ω	0 V	3.7 V
ECL	–1.8 V	–0.9 V	46.4 Ω	273 Ω	–5 V	–1.3 V

Marker Output Levels

The N6030A marker outputs use a 30 Ω series termination as a compromise that can drive both high impedance and 50 Ω loads. They have a low level of 0 V and a high level of 3.3 V, when driving a high impedance load. There are a total of four marker outputs that can be programmed independently. The marker output is clocked with the SYNC clock. The marker polarity, width and delay can all be set in multiples of the SYNC clock, although this capability is only supported in the IVI-C driver and not the GUI (with the exception of setting the polarity). The default marker width is two SYNC clock periods and the minimum is one period.

Synchronous Trigger Example

Figure 4 shows an example of how a synchronous trigger can be generated in the user's system. In this example, the user's master sample clock can be at any frequency in the range of 100 MHz – 1.25 GHz by using the external clock input of the N6030A. In the user's trigger generator circuitry, trigger events to control the N6030A sequencer are generated synchronous with a sub-multiple of the sample clock presented from the N6030A as the SYNC clock output. The timing of this trigger input must be correctly aligned with the SYNC clock output as described in earlier sections of this document. In this way, very repeatable triggering of the waveform output with extremely low jitter is achieved.

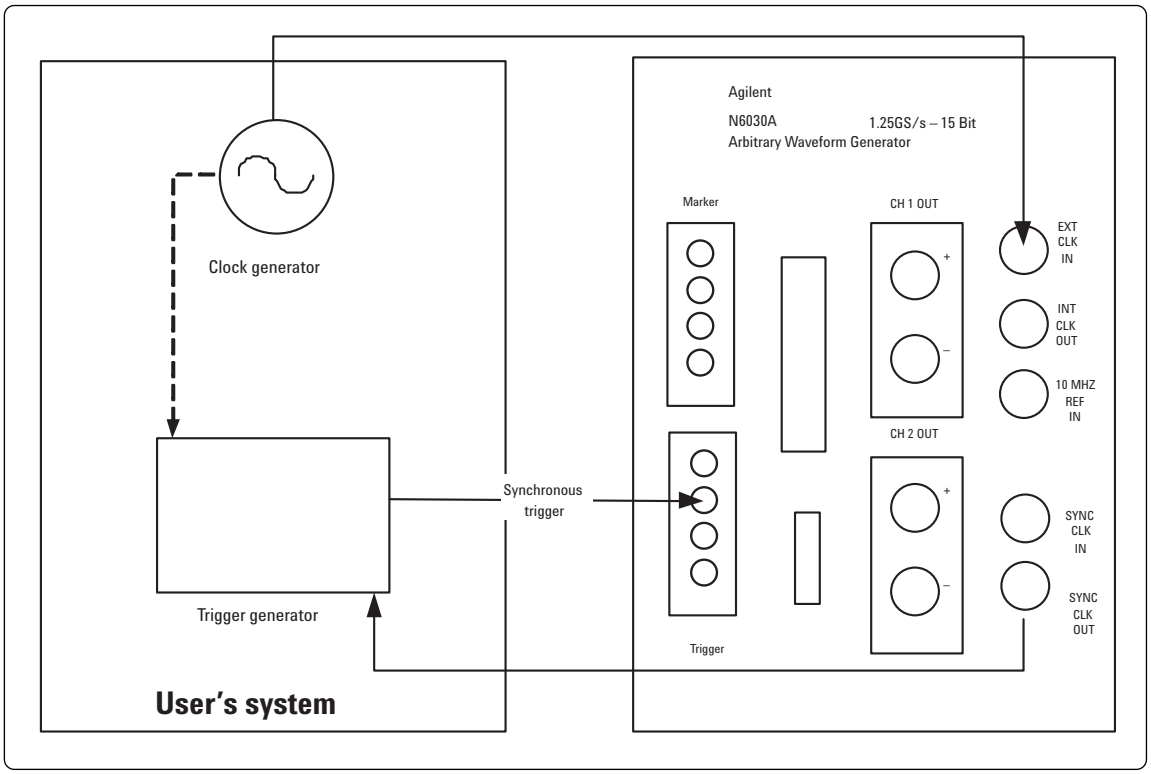

Figure 4 Synchronous trigger usage example

Conclusions

The N6030A is capable of deterministic waveform sequencer operation while responding to externally supplied hardware triggers. To guarantee proper trigger operation, care must be taken with the driving source termination and the setting of the threshold of the trigger input. In addition, the timing of the trigger pulse relative to the internal SYNC clock must be controlled to insure proper synchronous operation. When these requirements are taken into consideration, extremely reproducible, triggered, operation is obtained with a wide range of logic inputs.

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