Next Generation I/O Bus PCI-Express BER Test Solution

Product Note

Introduction & PCI-Express Background

As computer products have matured, the data speed on motherboard busses has been getting faster and faster. In 1980 the ISA bus (Industry Standard Architecture) was the first parallel interface to support a variety of I/O cards for graphic, sound and other human interfaces. In 1992 due to the huge demand for faster graphic interfaces, EISA (extended ISA) was migrated to the first version of PCI (Peripheral Component Interconnect) for color image displays. At this time, PCI was a synchronous multi-drop bus with up to 32 data lines running at a clock speed of 33 MHz.

PCI developed over several generations. The latest version of the parallel bus structure is called PCI-X running 64 bits wide with double-data rate up to 266 Mb/s. Within the latest standard there is also a quad-rate version with 532 Mb/s, but at the time of writing it has neither been implemented nor does it seem likely to be.

Synchronous parallel buses with separate clock signal lines suffer from skew problems as data rates become faster. This creates problems for PC Board designers who have to carefully route the traces to keep signals within the tolerances for setup and hold times. Crosstalk and ground bounce create further problems with regard to EMI (Electromagnetic Interference). In order to enhance North and South bridge transport capability, engineers at Intel Corporation came up with the idea of changing to serial communication.

If the clock signal is embedded in the data signal, it can be recovered by the receiver, eliminating skew problems. This concept turned out to be very successful: not only was PCI replaced by PCI-Express (PCIe), but other standards developed serial alternatives too (see Figure 1), IDE/ATA (AT Attachment) produced S-ATA, for example. The latest developments in these serialized interfaces, now in their second or third generations, have data lane speeds in the 5 Gb/s to 6.5 Gb/s range.
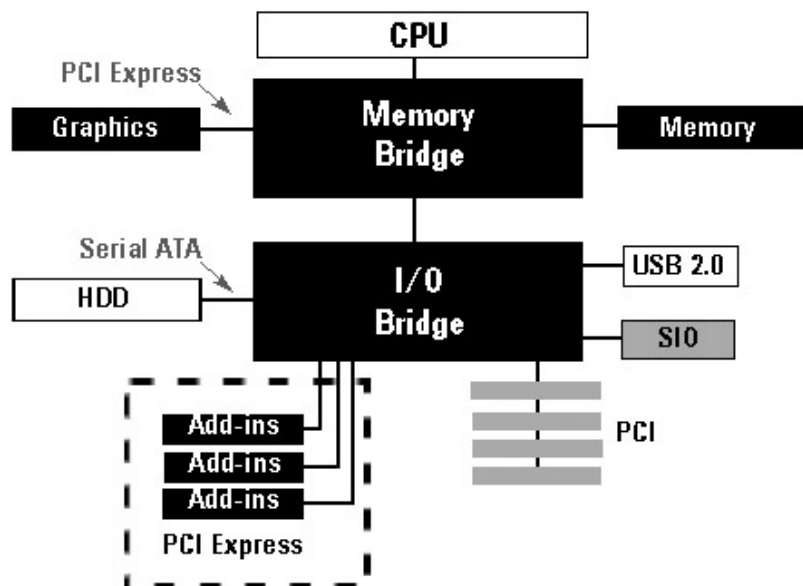

Figure 1: Motherboard Structure

PCIe Test Basics

PCIe increases data transport efficiency and data quality. It uses an 8/10b encoding methodology to embed the clock signal in the data signal. Each PCIe transport lane uses a differential pair and there can be up to 16 lanes. The data rate is 2.5 Gb/s in the current implementation, but at the time of writing, the standard is being upgraded for a second generation with twice this data rate. PCIe is designed for a Spread Spectrum Clock (SSC) to reduce EMI issues.

PCIe is structured into three layers: at the bottom there is the physical layer, then there is the data link layer and finally the transaction layer. Each layer needs proper instrumentation for validation and verification. The physical layer is normally tested using a pattern generator/error detector and an oscilloscope to check signal integrity and verify the Bit Error Ratio (BER). A logic analyzer can help validate the data link layer, as well as being useful for code debugging. A protocol analyzer and exerciser can do transaction layer validation.

The focus of this document is on physical layer testing on the transmitter (TX) and receiver (RX) terminal. BER testing not only provides system or chipset function checks, when properly set up it can also provide important information on TX and RX parametric capabilities. We focus here on the chipset designer and demonstrate how to implement a total BER test solution for a PCIe chipset. We detail how to use the Agilent 81250A ParBERT for BER measurements. We provide information on how to edit patterns on this equipment, and explain its capabilities for jitter injection and tolerance testing.

PCIe Environment and Setup for Test

PCIe testing can be performed in two ways: motherboard testing or add-in card testing (see Figure 2).

Motherboard testing concentrates on North Bridge or South Bridge chipsets placed on a motherboard. This needs a solution such as the Compliance Load Board (CLB) to interface to the TX and RX signals. Testing add-in cards, such as Ethernet or Graphic cards, should use the Compliance Base Board (CBB) to interface to the TX and RX signals. In such cases, the CBB needs to be powered, which can be done using a regular PC power supply. The motherboard normally provides the 100 MHz reference clock for motherboard testing, while for add-in card testing we need to provide this clock as part of the test setup.
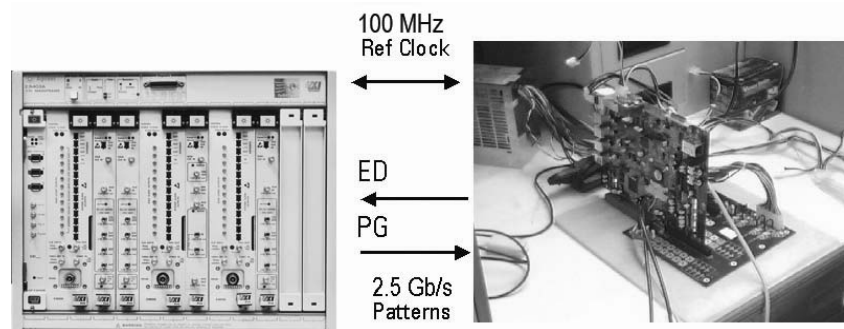

Figure 2: PCIe Graphics Card on Compliance Base Board

PCIe Physical Layer Specifications

Before testing we need to clarify the test margins by examining the specifications. The PCIe chipset includes both a transmitter (TX) and a receiver (RX), each with different physical parameters defined by the standard for the current generation. For the TX, the data stream is at 2.5 Gb/s, which corresponds to a Unit Interval (UI) of 400 ps. The data rate may vary by ± 300 ppm. This does not yet include SSC (Spread Spectrum Clocking), which will add a modulation of -0.5% at a rate of 30 kHz. The TX output provides differential amplitude between 800 mV (min.) and 1.2 V (max.), including de-emphasis. Figure 3 shows this de-emphasis on the single-ended normal and complement signals of the TX output. The first bit after a bit change is called the transition bit, which has a boosted power level. This boost compensates for losses in the transmitting medium, to raise the transmission efficiency. If a bit stays constant for more than 1 UI, this is called a de-emphasized bit. The amplitude of the de-emphasized bit may decrease by –3.5 dB nominal, which is called the de-emphasized output voltage. So when we check the PCIe TX eye quality, we must make sure to check both the transitional and the de-emphasized eye. Over time, the eye opening should reach a minimum value of 0.7 UI. In other words, a jitter of up to 0.3 UI is acceptable. The other part of the physical PCIe system is the RX. Again, the data rate is 2.5 Gb/s, or a UI of 400 ps, with ±300 ps timing variation. The differential amplitude of the input signal can be as low as 175 mV, and closed to 0.4 UI in time. The difference between RX and TX amplitude and timing specification is the budget for jitter allowed in the transmitting media between two chipsets. Apart from the minimum eye opening for the signal input to the RX, the jitter must not exceed 0.3 UI from the edge position of the ideal TX signal. Additionally the RX input must tolerate an AC peak common mode input voltage up to 150 mV.

All of these specifications can be addressed with a solution based on BER test, with some additional instrumentation.

But there is one further specification: the return loss, specified at a minimum of 15 dB. This needs different test equipment. We recommend the Agilent Vector Network Analyzer (E507X Series 4-port ENA) for this purpose.
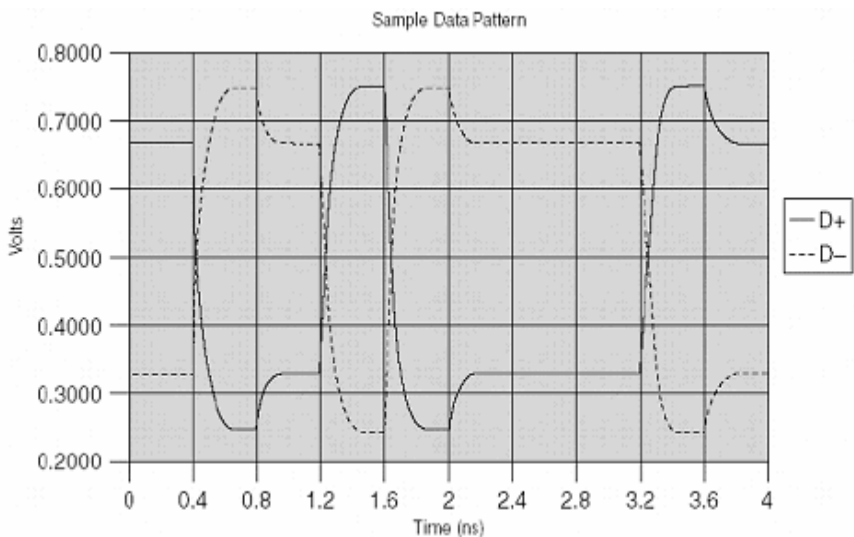

Figure 3: TX De-Emphasis

PCIe BER Test Principle

The basic theory for Bit Error Ratio (BER) testing can be applied to different digital data stream situations, such as optical transceiver test, digital IC chip test, or digital communication system test. The general approach is as follows: first we use a pattern generator to generate a bit stream which we send to the DUT (Device Under Test). Then we feed the bit stream from the DUT output back to the error detector. Based on the bit stream generated by the pattern generator, the error detector internally generates another bit stream, called the expected data. After digitizing and sampling the bit stream coming from the DUT, the error detector uses a decision circuit to compare this bit stream with the expected data, bit-by-bit in real-time. If the bits are different, this error count is incremented. The Bit Error Ratio is the number of errors divided by the total number of bits compared.

For BER testing of a PCIe chipset we need a known, deterministic and periodic bit stream which runs through the DUT. To do this we use the "loop back" mode defined in the PCIe standard. The PCIe standard defines a specific symbol (symbol 5) to be set within the link training sequences TS1 and TS2 that force the DUT to loop back. In general, the training sequences are part of the configuration when a PCIe link starts operating from a valid hot-plug-in (see Figure 4). In this setup the PCIe device runs through "detect state" into

"polling state", then moves to "configuration state" and finally into "L_0" mode by exchanging specific link information in TS1 and TS2 . The basic concept for forcing the loop back mode is to send a stream of TS1 and TS2 with the loop back bits enabled. Once in loop back mode, any bits we send, are returned back from TX terminal. This allows functional and parametric verification or compliance testing based on the BER measurement.

How to Create the Proper Training Sequence Flow

As described earlier, BER testing is a matter of comparing individual bits. The training ordered sets required here are based on symbols, which are bit streams based on the rules of:
- The running disparity of the 8b/10b coding
- The skip ordered set
- Proper repetition of the training ordered sets

On the BER test equipment, this is set up using the sequence and segment editing.

Test Equipment

In this document, we focus on a solution for a complete PCIe test using the 81250A ParBERT system. (Other Agilent solutions include the N4900 series SerialBERT; and for stimulus only, the Agilent 81133A/34A Pulse Pattern Generator). The 81250A ParBERT system offers the highest flexibility in configuring multiple channels for testing multiple lanes or for setting up multiple de-emphasized signals. We recommend two different configurations:
The first is for testing at the current PCIe speed of 2.5 Gb/s, and is based on 3.35 Gb/s ParBERT hardware. The second is intended for the next generation of PCIe or SATA and uses either the 7 Gb/s or 13.5 Gb/s hardware. Initially, the 7 Gb/s may be sufficient, and this can be upgraded to 13.5 Gb/s later, making this a good choice to begin with.

For add-in card testing we always need to provide the 100 MHz reference clock. For motherboard testing we can get the clock from the setup. The configurations listed below
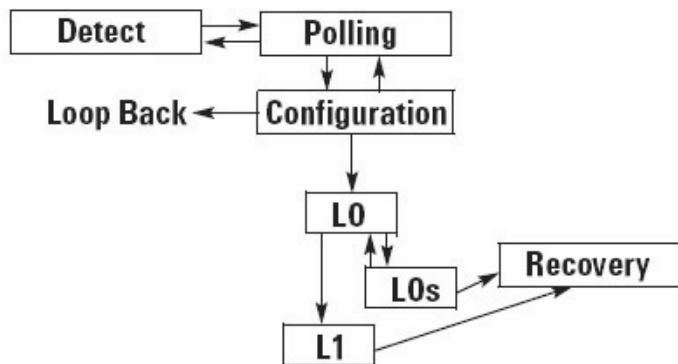

Figure 4: Loop Back mode within PCI-Express Status

show what needs to be added to provide a reference clock:

3.35 Gb/s ParBERT System
- 1×81250A ParBERT with #013 Firewire & #149 Frame
- 1×E4875A User Software
- 1×E4808A Clock Module
- 2×E4861B Data Module
- 2×E4862B Generator FE
- 1×E4863B Analyzer FE

For a reference clock from the test system:
+ 1×E4805B Clock
+ 1×E4832A Data module
+ 1×E4838A Generator FE

7/13.5 Gb/s ParBERT System
- 1×81250A ParBERT with #013 Firewire and #149 Frame
- 1×E4875A User Software
- 2×E4809A 13.5 GHz Clock
- 3×N4872A/74A 13.5 G / 7G Pattern Generator Module
- 1×N4873A/75A 13.5 G / 7 G Analyzer Module

For a reference clock from the test system:
+ 1×E4809A Clock
+ 1×N4872A/74A 13.5 G / 7 G Pattern Generator Module

Table 1 compares the functionality of the two recommended configurations. This also shows that the faster system also has additional capabilities:
- Full jitter tolerance
- Full differential eye opening
- Analyzer with Clock Data Recovery (CDR)
- Spread Spectrum Clocking

The 7/13.5 Gb/s configuration has three clock groups:
The first clock group uses two 7/13.5 Gb/s pattern generators. We demonstrate how this combination can be used to set up the de-emphasized signal.

The second clock group uses the N4873A/75A analyzer module, and is necessary if we plan to use the CDR. Finally, the third clock group can provide the 100 MHz reference clock. The full configuration is shown in Figure 5.

The results presented later in this document are from the 13.5 Gb/s configuration testing a PCIe 2.5 Gb/s add-in card.

Configuration Matrix	ParBERT 3.35 Gb/s	ParBERT 7/13.5 Gb/s
Parametric Test PCI 2.5 G	•	•
Parametric Test Next Generation PCI		•
De-emphasized Signals	•	•
Delay Control	•	•[1]
Jitter Tolerance		•
Differential Output Timing	•	•
Differential Eye Opening		•
CDR		•
SSC Clock		•

Table 1: Selection of ParBERT configuration
Note (1): Delay Control covers 0.5UI max for PCIe 2.5 G

Additional Equipment and Accessories

1. Agilent 54855A real time oscilloscope, equipped with E2688A high speed serial data analysis software
2. Agilent E4422B Signal Generator with FM modulation capability
3. Agilent 33250A Arbitrary Waveform Generator
4. 2×11636B Power Divider for SSC clock dividing
5. 3×11667B Power Splitter for de-emphasis generation
6. 5×15442A 4×SMA cable kit
7. 8×N4911A opt 002 3.5 mm (f) to 2.4 mm (m) adapter

Testing for the PCIe Standard

To test whether a DUT meets the requirements of the PCIe standard, as outlined above, we perform the following tests:

For the RX:

1. Functional test at 2.5 Gb/s by running a BER measurement and checking the BER value
2. Creating a de-emphasized signal, and reducing it to minimum amplitude
3. Adding jitter to reduce the eye opening in time
4. Adding common mode voltage as noise

For the TX:

1. Functional test at 2.5 Gb/s by running a BER measurement and checking the BER value
2. Checking the voltages either on an oscilloscope or using the ParBERT measurement suite (eye opening /output level measurement)
3. Checking the eye on the oscilloscope or with help of the ParBERT measurement suite (eye opening/output timing measurement)
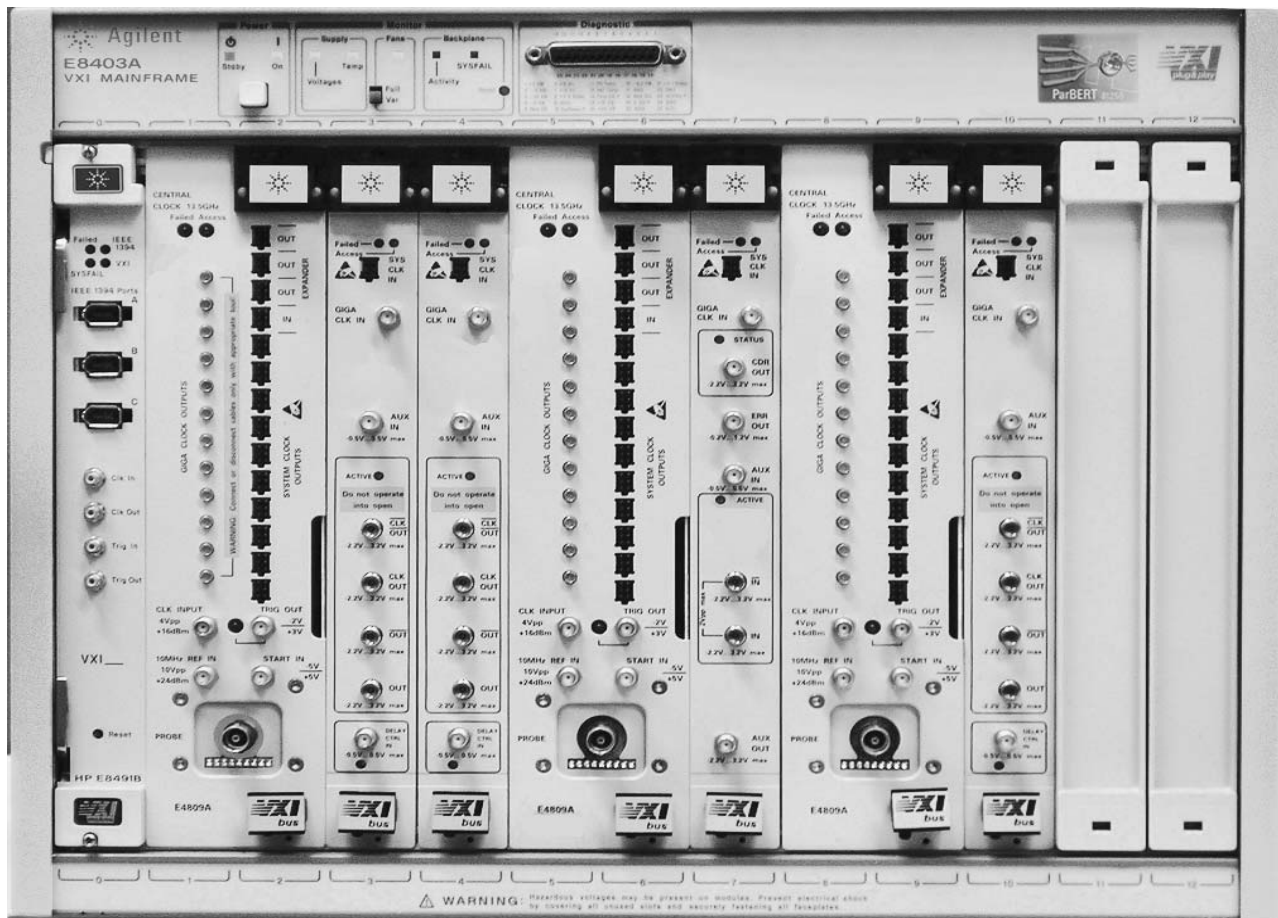4. Debugging jitter with help of ParBERT measurement suite (spectral jitter decomposition)

Figure 5: 81250A ParBERT Configuration 7 G/13.5 G including three clock groups

## How to Generate De-Emphasis Patterns

Verifying the compliance of the signal waveform is best done using an oscilloscope. The characterization of the RX should also check for the sensitivity to any kind of de-emphasis. This means we need to construct a de-emphasized signal with variable magnitude and duration of the pre-emphasis. We can achieve this by combining two pattern generator channels as indicated in Figure 6.

According to the PCIe specification, the pattern voltage swing shall not exceed 1.2 V_{pp}, so we can set ParBERT channel 1 to 1 V_{pp} and channel 2 to 200 mV_{pp}. We then subtract the signal from channel 2 from the signal of channel 1, and apply this to two electrical combiners (11636B power divider) to produce the de-emphasized signal as a differential pair. (Using the combiners, we actually lose half of the amplitude of the single-ended signals, but as the differential amplitude doubles again, we end up meeting the specifications.) We have two choices for delaying the de-emphasized signal:

- either we edit the pattern to shift the bits by one bit; this creates a de-emphasized voltage starting at the second bit.
- or we duplicate the pattern and set the generator delay to 1 UI.

Using the generator delay we can fine-tune the position of the de-emphasis to more or less than 1 UI.
Figure 7 shows a de-emphasized signal on an
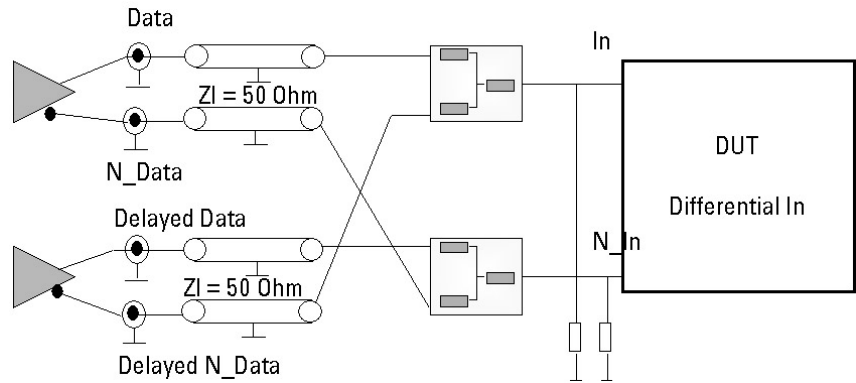
Figure 6: Generator setup for the de-emphasized signal

Agilent 54855A real time oscilloscope equipped with E2688A high speed serial data analysis software. This also has an 8b/10b decoding function, which can be used to check whether the chipset was properly forced into loop back mode. This makes it a good complimentary tool to the ParBERT system.
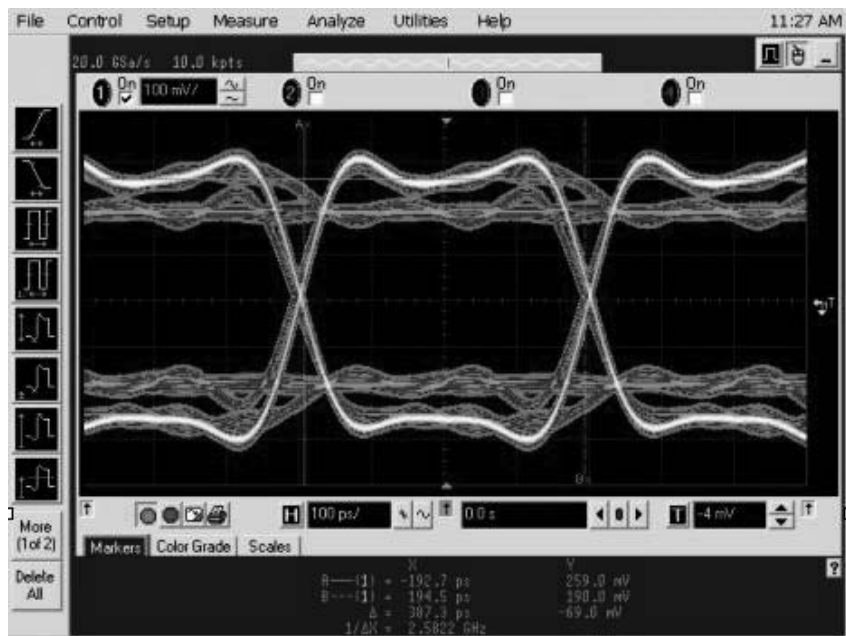
Figure 7: De-emphasized signal by combining two generators

81250A ParBERT Setup

For the test we need to set up:
1. Frequency
We use a signal generator with FM capability, run at 2.5 GHz, to drive an external clock to all clock inputs set for direct external clock. We need to split the signal generator's output three times using two power splitters.
This setup may sound over-engineered, but it does mean that we are already prepared for using a Spread Spectrum Clock.

2. Signal into RX:
We combine the two generators to drive the RX with the de-emphasized signals, as described before. For a functional test we use 1 V_{diff_pp}. The differential amplitude is twice the single ended amplitude, but we lose half of the single ended amplitude due to the power dividers, so we use the dc levels of HIL= +0.5 V and LOL= -0.5 V on generator 1 and HIL = +0.1 V and LOL =-0.1V on generator 2. Due to AC coupling, we use the levels symmetrically around ground and set the termination voltage V_t = 0 V.

3. For the analysis we can either use the external clock from the signal generator or the CDR capability of the 81250A ParBERT. If we decide for CDR mode, we need to reconnect the external clock input to the CDR output. Using the CDR mode may have advantages when testing for jitter, because low frequency effects will be tracked by the CDR and omitted from the jitter values. For SSC testing, we recommend running the analyzers on the external clock to keep the test system in sync with the SSC clock.

4. Figure 8 shows the sequence-editing environment. It combines nested loops and customized user patterns. It indicates the setup of the necessary TS1 and TS2 flow with embedded SKIP symbol generation. The provision of SKIP symbols is required on a regular basis, here it is provided by the segments TS1SKP and TS2SKP. With the loop back bits in place, TS1 and TS2 force the PCIe device into loop back mode. Once in loop back mode, we use a pattern with a length of 2560 bits. This length fulfills the analyzer's requirements for proper synchronization.

5. Each segment within the sequence can be individually edited for the desired bits. For a segment of expected data on the analyzer, it is sometimes useful to use the masking capability. This means ignoring specific bits in the BER measurement. By masking either the de-emphasized or transition bits, we can measure the eye opening on the transition bit and on the de-emphasized bit respectively.

Figure 8: Nested Loop pattern for BER Measurement in Loop back

Test Results

The following test results were obtained for a graphic card connected with the compliance base board (CBB). The ParBERT provided a de-emphasized data signal and the 100 MHz reference clock. The output was first checked with a real-time oscilloscope, then with the error detector of the BERT.

RX/TX Functional Test:
Figure 9 shows the results of an extended BER test; there are no errors within the test time of roughly 18 hours.

TX output:
In Figure 10 we check the waveform by connecting the TX outputs to the inputs of the real-time oscilloscope. 1m of coaxial cabling, together with the wiring on the CBB board, creates enough loss to mostly eat-up the pre-emphasis, so we have a hard times to measure this.
In Figure 11, we check the TX output with the eye opening measurement provided by the 81250 ParBERT. This is a view of the true differential signal. The left eye is from the transition bit; the right eye is from the de-emphasized bit (obtained by masking the expected data). Please notice that the voltage reading is at the BER threshold of 1e-6, which is different from an oscilloscope reading.

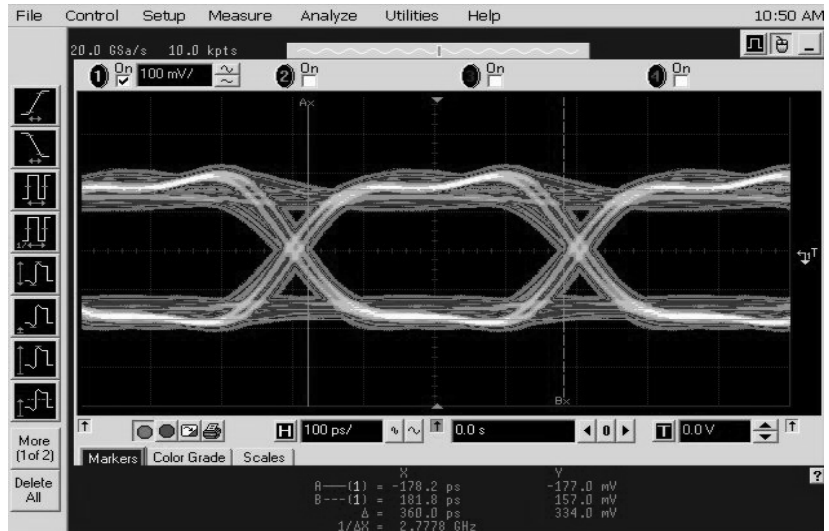**Figure 9: BER Test result after roughly 18 hours**

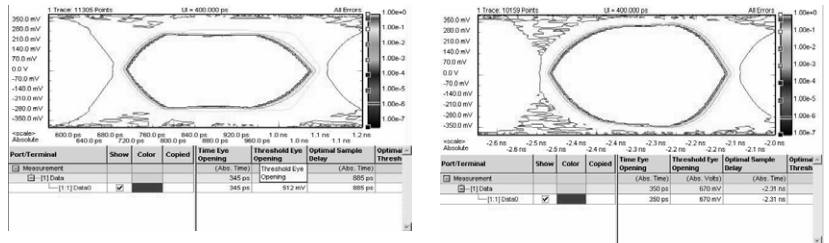**Figure 10: Single ended Waveform from TX output on the Real-Time Scope**

Figure 11: Eye Opening measurement on differential signal of TX on Transition Bit (left) and de-emphasized bit (right)

Alternatively, we can measure the levels with the output level measurement of the ParBERT (see Figure 12). This uses the same connection as in Figure 9, so again we lose some of the de-emphasis, but we can measure the differential amplitude directly. The measured value for the amplitude matches double the value obtained from the oscilloscope reading very well.

Another way of looking at the TX output performance uses the output timing measurement. This provides jitter measurement, including Rj and Dj separation, as shown in Figure 13. This goes beyond the specification, but provides valuable information for debugging.

Apart from the phase margin reading, which is taken at the actual BER threshold, there is an extrapolation for Total Jitter (Tj) for the BER threshold 10^{-12}.

Finally, another meaningful debug tool is the spectral jitter decomposition. This provides an insight into the spectral content of the jitter and can be helpful in isolating sources of jitter (see Figure 14).
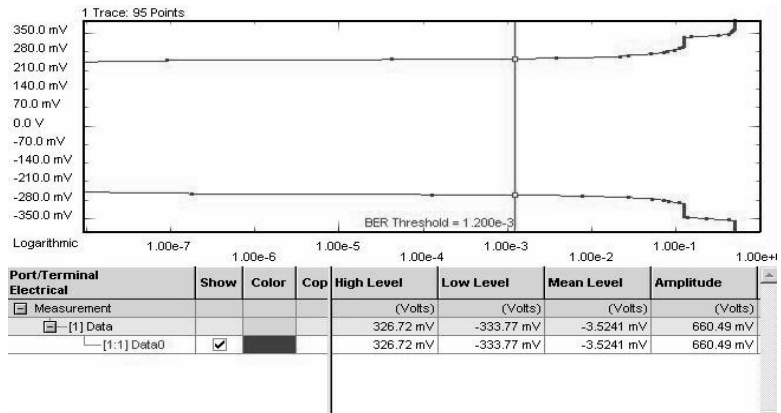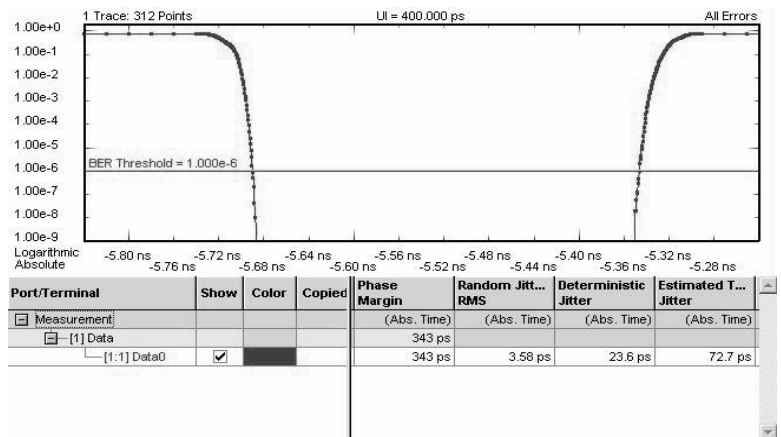

Port/Terminal Electrical	Show	Color	Cop	High Level (Volts)	Low Level (Volts)	Mean Level (Volts)	Amplitude (Volts)
⊟ Measurement							
⊟ [1] Data				326.72 mV	-333.77 mV	-3.5241 mV	660.49 mV
[1:1] Data0	✔			326.72 mV	-333.77 mV	-3.5241 mV	660.49 mV

Figure 12: Output Level Measurement

Port/Terminal	Show	Color	Copied	Phase Margin (Abs. Time)	Random Jitt... RMS (Abs. Time)	Deterministic Jitter (Abs. Time)	Estimated T... Jitter (Abs. Time)
⊟ Measurement							
⊟ [1] Data				343 ps			
[1:1] Data0	✔			343 ps	3.58 ps	23.6 ps	72.7 ps

Figure 13: Output Timing Measurement

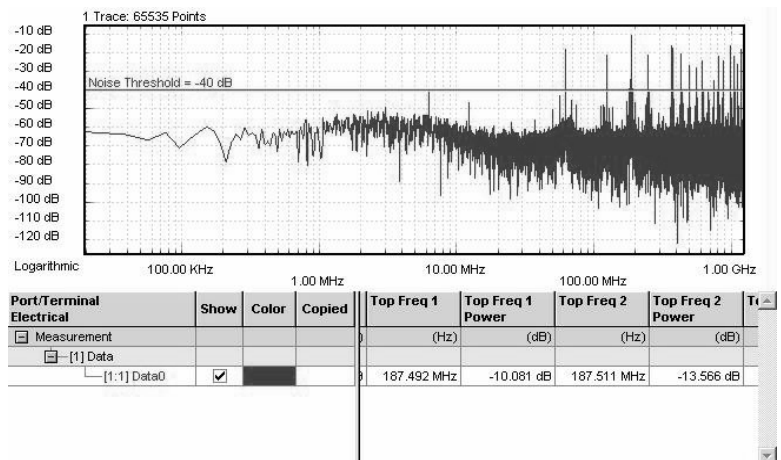| Port/Terminal Electrical	Show	Color	Copied	Top Freq 1 (Hz)	Top Freq 1 Power (dB)	Top Freq 2 (Hz)	Top Freq 2 Power (dB)	T(
⊟ Measurement								
⊟ [1] Data								
[1:1] Data0	✔			187.492 MHz	-10.081 dB	187.511 MHz	-13.566 dB	

Figure 14: Spectral Decomposition Measurement

RX input:

To check the parametric behavior of the RX input, we need to use the de-emphasized signal, set up as described earlier, for a minimum amplitude of 175 mV$_{pp}$ diff. Then we add jitter to the signal to create a minimum eye. This is called jitter tolerance testing. With the help of an arbitrary waveform generator (Agilent 33250A), we feed a sinusoidal signal into the delay control input of the generator. With the help of an additional noise source we can create a jitter mix consisting of Rj and Dj. This jitter tolerance setup is shown in Figure 15. This setup is able to provide jitter up to 1 UI at a data rate of 5 Gb/s (0.5 UI at 2.5 Gb/s). For multiple UI we need to add a signal generator with FM modulation capability.
The delay control is limited to 200ps, so for the 2.5 Gb/s PCIe device we cannot close the eye to the point of failure. This will be possible for any implementation running at 5 Gb/s or higher, as a 100% closure is possible there.

To create the minimum swing and the eye closure in time, we monitor the single ended stimulus signal on the oscilloscope as shown in Figure 16.

The current standard for PCIe does not say much about jitter tolerance requirements, but we expect that the next, faster implementation will require operation according to a jitter tolerance curve. This needs to be tested by sweeping the jitter frequency and magnitude from multiple UIs at low
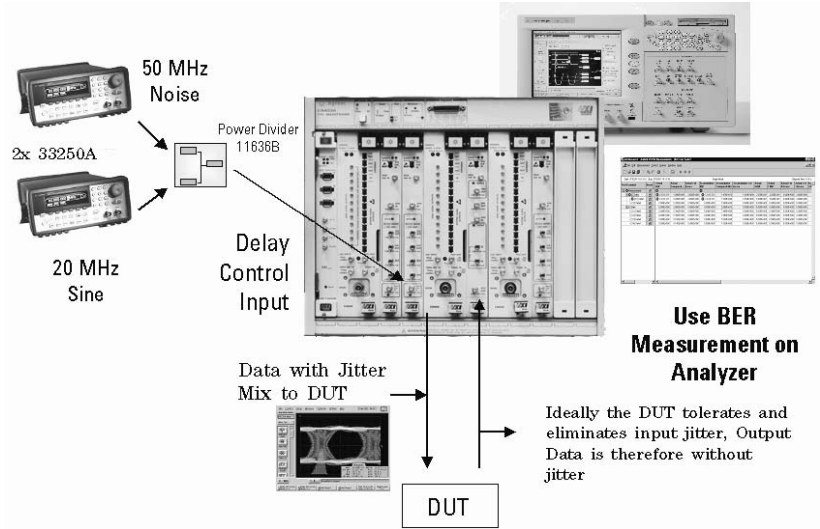

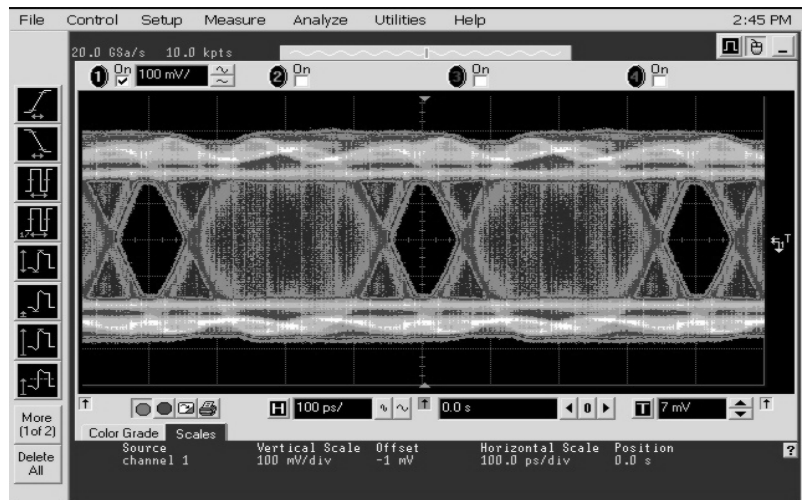**Figure 15: Jitter Tolerance Setup w/o Signal Generator**

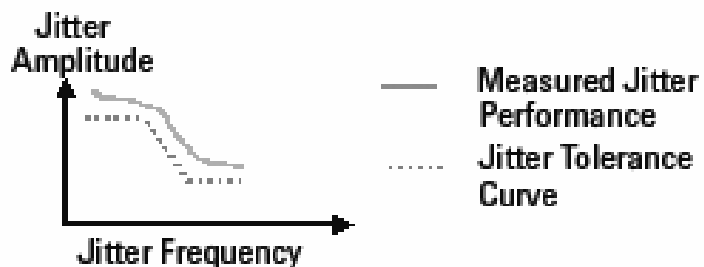**Figure 16: de-emphasized signal with jitter modulation**

Figure 17: Jitter Tolerance Curve Example

frequency to fractions of a UI at higher frequency (see Figure 17). The setup including the signal generator for clock modulation and the function generator for delay control provides full capabilities for this.

Spread Spectrum Clocking

The PCIe standard says that the data rate can be modulated from +0% to - 0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30 kHz – 33 kHz. The ± 300 ppm requirement still holds, which requires the two communicating ports to be modulated such that they never exceed a total of 600 ppm difference. For most implementations, this places the requirement that both ports require the same bit rate clock source when the data is modulated with an SSC.

FM modulation is symmetrical. The practical setting on the signal generator is therefore 2.49375 GHz with a modulation deviation of ±.2.5%, which is 6.25 MHz
With a modulator sensitivity of 10 MHz/V, we need to apply amplitude of 625 mV from the modulating source. Some signal generators provide internal modulating capabilities.

The results are interesting: when modulating the ParBert with an SSC clock, system performance is already slightly affected – the eye opening in loop back mode reduces from 95% to 82%, the PCIe device
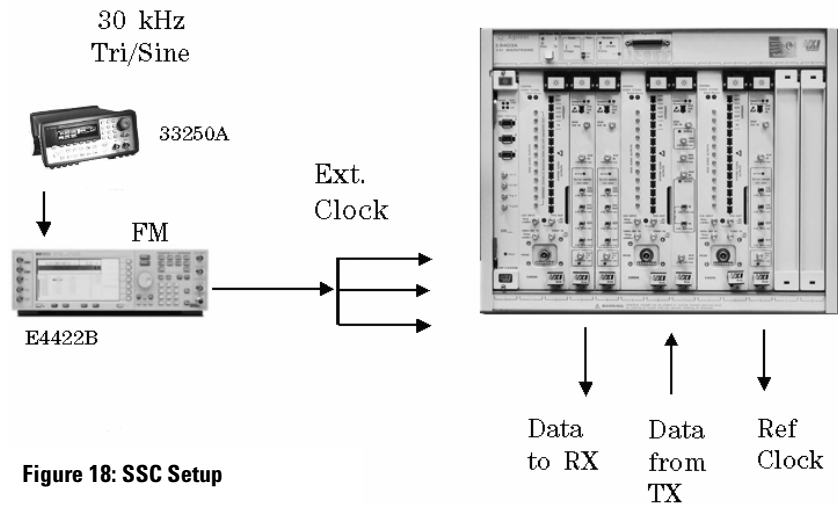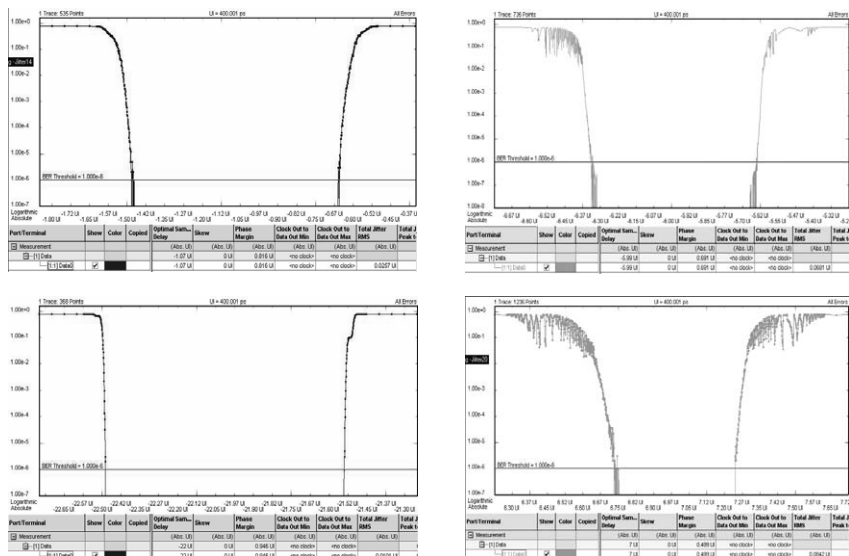
Figure 18: SSC Setup

Figure 19: SSC Results

is closing from 70% without SSC, to 50% with SSC. The eye closure is taken at a BER threshold of 1e- 6. As the standard does not specify a BER threshold for the eye opening, we cannot compare this directly to the specifications.

Conclusions:

A robust PCIe physical layer test solution is very important for companies designing chipsets. BER test is getting more and more important as the data rate increases. This is especially true for next generation PCIe and SATA II/III and high speed Fully Buffer Dimm (AMB chip) test in the future. With its ParBERT, Agilent offers a powerful solution for the measurement needs of the physical layer.

References:

[1] PCI Express™ Base Specification Revision 1.0a, April 15, 2003

[2] Compliance Base Board (CCB), Compliance Load Board (CLB), see the link: http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library

Ordering instructions:

To minimize startup time please order Special Application Start-up kit E4875PCI:
- Setting, Segments
- Setup Guide
- Detailed App.-Note including measurement results
- CBB
- PCIe Graphic Card
- Powersupply

Related literature	Publication number
Agilent ParBERT 81250 13.5 Gb/s Parallel Bit Error Rate Test Platform Photocard	5988-9201EN
Jitter Tolerance Testing Agilent ParBERT 81250 Platform Application Note	5989-0223EN
Testing High Speed IO Interfaces Based on Spectral Jitter Decomposition Datasheet	5989-0611EN

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