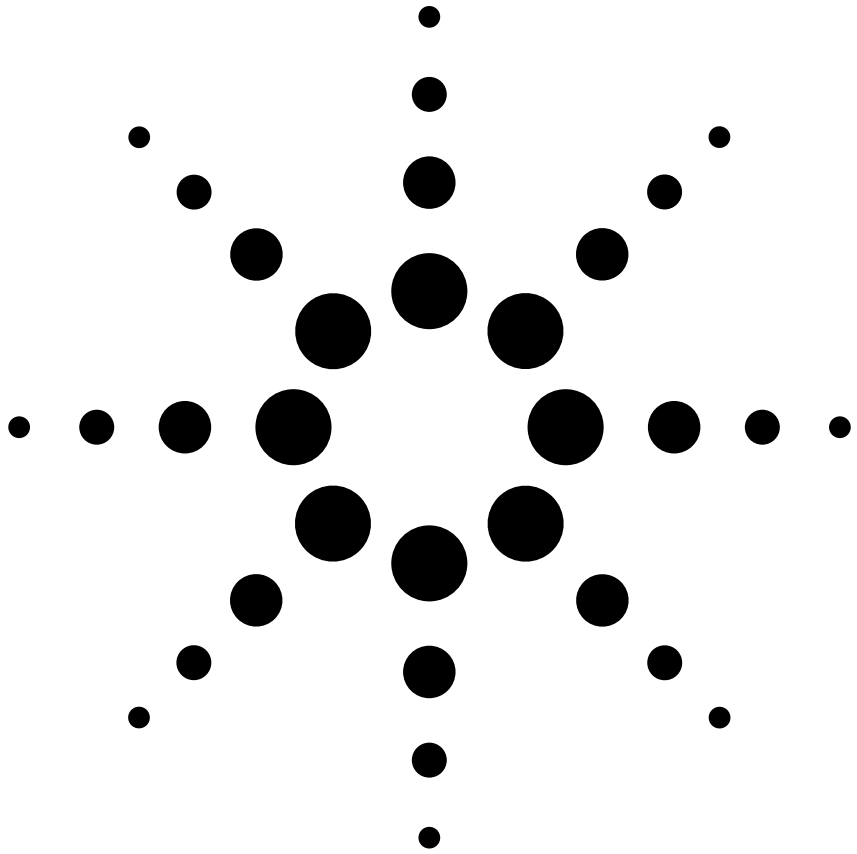
Agilent
Utilizing TDR and VNA Data to Develop 4-port Frequency Dependent Models for Simulation

White Paper



Agilent Technologies

Abstract

Frequency dependent effects are becoming more prominent with the increasing data rates of digital systems. Differential circuit topology is proliferating throughout design laboratories with the goal of enhancing the data carrying capable of the physical layer. Simple impedance and delay measurements of copper transmission lines on backplanes are not sufficient to ensure accurate analysis of gigabit interconnects. The challenge to push design rules to the limit now requires the use of concurrent time and frequency domain measurements. This paper will discuss methods to achieve proper measurement techniques using a time domain reflectometer (TDR) oscilloscope and vector network analyzer (VNA) to assure accurate models are produced for simulation. Error correction techniques will be discussed for both time domain and frequency domain instrumentation. It will be demonstrated that accurate 4-port frequency dependent models can closely simulate performance of a differential channel.

Signal Integrity Challenges

With the increase in speed of digital system design into the gigahertz region, frequency dependent effects become a more prominent challenge than in the past. Yesterday's interconnects could be easily characterized by measuring the self-impedance and propagation delay of the single-ended transmission line. This was true for printed circuit board stripline, microstrip, backplanes, cables and connectors. However, the proliferation of high-speed serial data formats in today's digital standards demand differential circuit topology. A paradigm shift in measurement technology is required to achieve the design goals of the advanced differential physical layer. It is now necessary to consider both time and frequency domain analysis to obtain proper characterization. Tracking the technology adoption curve in Figure 1 below, shows that several new implementations of PCI Express and Infiniband reach data rates into the 4 Gb/sec range. New standards, such as XAUI, OC-192, 10 G Ethernet, and OC-768 aim even higher–up to and past 40 Gb/sec. This upward trend creates signal integrity challenges for physical layer device designers and the inevitable struggle to keep up with data processing and storage capabilities.

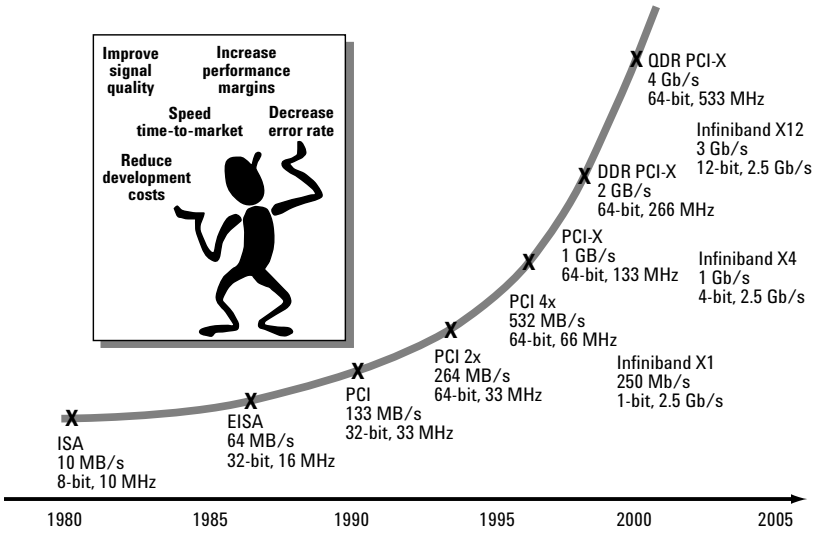


Figure 1. Partial list of many new high-speed serial link formats.

Trend to Differential Topologies

In the discussion of these new signal integrity challenges, it becomes clear why we need to understand the implications of differential topologies and how mode-conversion analysis is an important concept for designing digital interconnects.

Ideal differential linear passive interconnects respond to and/or generate only differential signals (two signals of equal amplitude and opposite polarity). These perfectly designed devices exhibit beneficial characteristics noted in Figure 2 and do not generate in-phase signals (also known as common signals). Any radiated external signal incident upon this ideal differential transmission line is considered a common signal and is rejected by the device. This is called common mode rejection ratio (CMRR) and is the main benefit of differential topology. The radiated common signals are usually generated from adjacent RF circuitry or from the harmonics of digital clocks. Properly designed differential devices can also reject noise on the electrical ground, since the noise appears common to both input terminals.

Non-ideal differential transmission lines, however, do not exhibit these benefits. A differential transmission line with even a small amount of asymmetry will produce a common signal that propagates through the device. This asymmetry can be caused by any physical feature that is on one line of the differential pair and not the other line, including solder pads, jags, bends and digs. This mode conversion is a source of EMI radiation. Most new product development must include EMI testing near the end of the design cycle. Very often the test results show that the design exhibits EMI radiation or susceptibility. However, there is usually very little insight as to what physical characteristic is causing the EMI problem. Mode conversion analysis provides the designer with that insight so that EMI problems can be resolved earlier in the design stage.

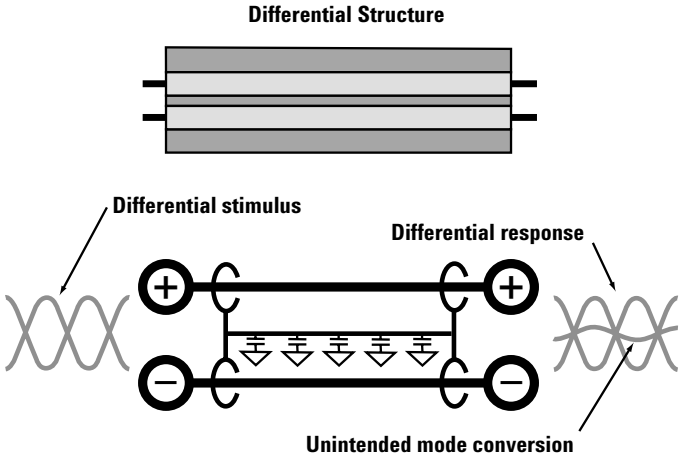


Figure 2. Ideal differential structures exhibit no mode conversion if they are perfectly symmetric.

Model Extraction Methodologies

In order to describe the test system laboratory configuration used in this design case study, the authors will refer to the flowchart in Figure 3 for clarification purposes. Measurement based model extraction can be accomplished using a variety of methods. The ultimate goal is to achieve an accurate model that can be simulated in either the time domain or frequency domain. Most digital designers will focus on time domain models and that will be our focus in this paper. Either a topological model or behavioral model may be developed. The topological model is based on the physical structure of the device and can be very complex for a lengthy device exhibiting multiple impedance discontinuities. This requires multiple iterations and is easily done using today's standard PC computational power. The behavioral model is a "black box" approach and describes how the device behaves toward a particular stimulus. One type of behavioral model is scattering parameters or S-parameters.

This flowchart shows that both time domain test equipment (time domain reflectometer or TDR) and frequency domain test equipment (vector network analyzer or VNA) were used to measure prototype devices. Both test instrument types have strengths and weaknesses and the specific user application will normally dictate the use of one or the other. In general, the TDR is easier to use and the VNA is more accurate. Most signal integrity laboratories have one of each.

In this experiment, measurements were made with a VNA using the Agilent N1930A physical layer test system software to control the VNA via GPIB. This allowed for use of the automated calibration wizard and simplified this typically rigorous and error prone process. The resultant 4-port S-parameter data was exported to the TDA Systems IConnect MeasureXtractor model extraction tool that in turn created an accurate time domain Hspice model.

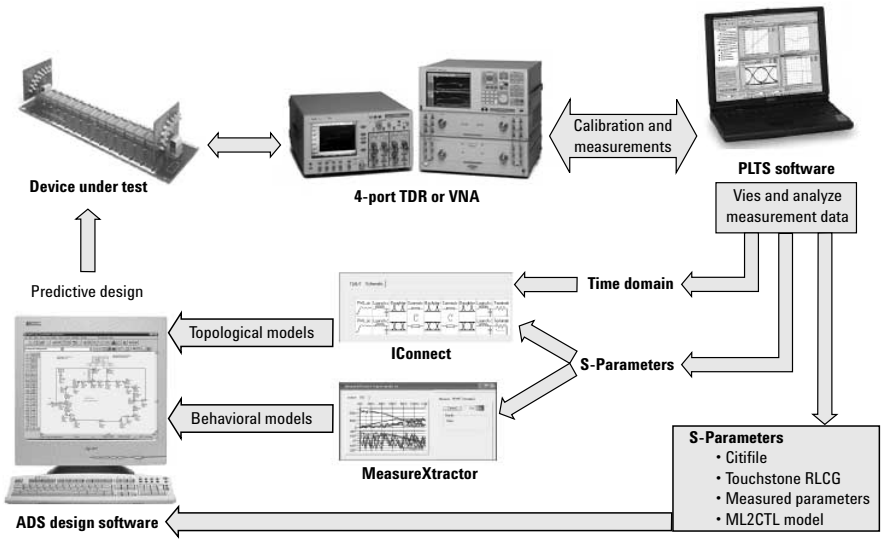


Figure 3. Many different methods exist today for model extraction, but measurement-based model extraction is a relatively new process yielding insight into high frequency effects.

The model extraction tool used in this design case study was the TDA Systems IConnect MeasureXtractor. It was chosen because it was simple and easy to use. This extraction tool imports the impedance profile or 4-port S-parameters after the user performs the measurement with either a time domain reflectometer (TDR) or vector network analyzer (VNA). The resultant model can be directly linked to a simulator subsequent to using a laptop to perform multiple iterations of model refinement. The convenience of comparing measured results to simulated results very quickly is an efficient way to check accuracy of models.

Typical Four Port Measurement Systems

Measurement based models for differential devices require a 4-port measurement system. A well-calibrated and controlled stimulus will be input to the device under test and the response will be measured with receivers co-located within the same measurement system. With a full 4-port measurement system, this stimulus/response test is performed on the reflected response and transmitted response in both single-ended mode and differential mode. The TDR instrument accomplishes this task with a fast step with little overshoot in concert with a wideband receiver to measure step response. The VNA uses a precise sine wave and sweeps frequency as a narrow band receiver tracks the swept input response. This narrow band receiver is what enables low noise and high dynamic range of the VNA.

Whether the data acquisition hardware is time domain based or frequency domain based, mixed mode data is also compiled in a 4-port measurement system. The mixed mode data refers to two specific test conditions: one being differential stimulus and common response and the other being common stimulus and differential response. This analysis leads to the discovery of interesting effects due to asymmetry within a differential transmission line.

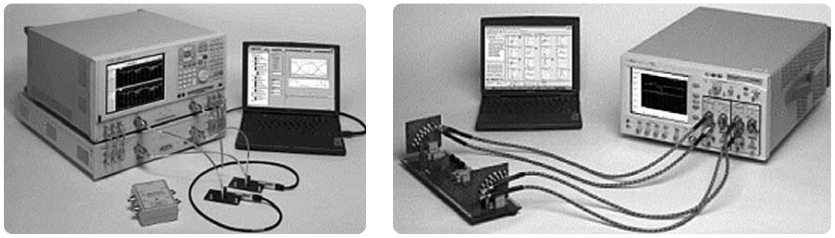


Figure 4. High-speed differential interconnects need to be characterized with a 4-port measurement system, whether it be a 4-port VNA (left) or 4-channel TDR (right).

Understanding 4-port Mixed Mode Analysis

In order to interpret the large amount of data in the differential parameter matrix, it is helpful to analyze one quadrant at a time. The first quadrant in Figure 5 is defined as the upper left 4 parameters describing the differential stimulus and differential response characteristics of the device under test. This is the actual mode of operation for most high-speed differential interconnects, so it is typically the most useful quadrant that is analyzed first. It includes input differential return loss (S_{DD11}), input differential insertion loss (S_{DD21}), output differential return loss (S_{DD22}) and output differential insertion loss (S_{DD12}). Note the format of the parameter notation SXYab, where S stands for Scattering Parameter or S-parameter, X is the response mode (differential or common), Y is the stimulus mode (differential or common), a is the output port and b is the input port. This is typical nomenclature for frequency domain scattering parameters. All sixteen differential S-parameters can be transformed into the time domain by performing an inverse fast fourier transform (IFFT). The matrix representing the time domain will have similar notation, except the "S" is replaced by a "T" (i.e. T_{DD11}).

The second and third quadrants are the upper right and lower left 4 parameters, respectively. These are also referred to as the mixed mode quadrants. This is because they fully characterize any mode conversion occurring in the device under test, whether it is common-to-differential conversion (EMI susceptibility) or differential-to-common conversion (EMI radiation). Understanding the magnitude and location of mode conversion is very helpful when trying to optimize the design of interconnects for gigabit data throughput.

The fourth quadrant is the lower right 4 parameters and describes the performance characteristics of the common signal propagating through the device under test. If the device is design properly, there should be minimal mode conversion and the fourth quadrant data is of little concern. However, if any mode conversion is present due to design flaws, then the fourth quadrant will describe how this common signal behaves.

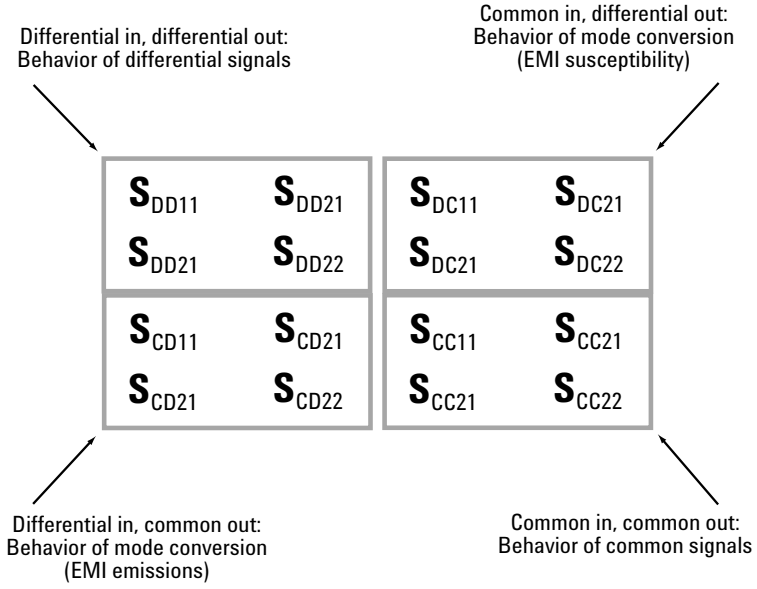


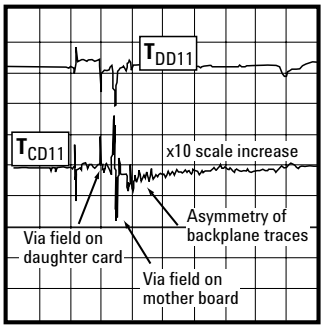
Figure 5. The sixteen S-parameters that are obtained by fully characterizing a differential interconnect can be categorized into 4 stimulus/response quadrants: differential in/differential out, common in/common out, common in/differential out and differential in/common out.

Differential Interconnect Analysis

The first step in the process of analyzing differential interconnects is to understand the 16 S-parameters and what information can be extracted from the large amounts of data. Next, the actual measurement is made to obtain these 16 S-parameters. This can be done with a variety of frequency domain instrumentation (vector network analyzers) or time domain instrumentation (time domain reflectometers). Figure 6 describes the important 4-port S-parameters that lead to successful differential interconnect analysis. Differential impedance is the most ubiquitous figure of merit for describing the quality of the transmission line under test. Designing a controlled impedance environment for the differential signal is crucial for propagating high-speed data. Then, the next most important parameter is finding lossy transmission lines by observing the input differential insertion loss (S_{DD21}). This will give a very accurate indication of the bandwidth of the device under test. Lastly, carefully analyzing mode conversion (T_{CD11} and S_{DC21}) is crucial to high-speed design. Optimization of the design can be accomplished by determining the magnitude of mode conversion as a percentage of input signal and then locating the physical structure that is causing the mode conversion.

Measure important parameters

T_{DD11}	Differential impedance profile
S_{DD21}	Signal quality of differential signal, time delay of differential signal
T_{CD11}	Conversion of differential signal to common signal in reflection (emissions)
S_{DC21}	Conversion of common signal to differential signal in transmission (susceptibility)
T_{CC11}	Common impedance profile
S_{CC21}	Signal quality of common signal, time delay of common signal



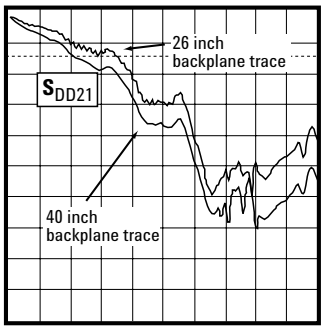


Figure 6. Example of typical 4-port analysis using both time and frequency domain data. Note: this is just an example from a 3 Gb/s backplane, not from the design case study device.

Measurement Accuracy and Error Correction

Ideally, all test equipment would not require any correction. However, in the real world imperfections exist in even the highest quality test equipment. Some of the factors that contribute to measurement error are predictable over time and can be removed, while others are random and cannot be removed. The basis of error correction is to measure a known electrical standard and use this device as a reference.

All measurement systems can exhibit three types of measurement error:

- Systematic errors
- Random errors
- Drift errors

Systematic errors are caused by imperfections in the test equipment and test setup. If these errors do not vary over time, they can be characterized through calibration and mathematically removed during the measurement process. Random errors vary randomly as a function of time. Since they are not predictable, they cannot be removed by calibration. The main contributors to random errors are instrument noise. Drift errors occur when a test system's performance changes after a calibration has been performed. They are primarily caused by temperature variation and can be removed by additional calibration.

The error correction techniques shown in Figure 7 are described as follows: time-domain gating is easiest to implement. The user defines a start and stop point, and software mathematically replaces the measured data in that section with an ideal transmission line. With the enhanced dynamic range of the network analyzer, multiple gates are possible, but accuracy diminishes in proportion to the number of gates. Port extension will mathematically extend the measurement plane to the input of the device under test. However, it assumes the fixture looks like a perfect transmission line with a flat magnitude response, a linear phase response, and constant impedance. Port extensions are usually done after a coaxial calibration has been performed at the end of the test cables. De-embedding removes a fixture or unwanted structure from the measurement by using the S-parameters or an accurate linear model of the structure. This S-parameter or model representation is mathematically removed from the DUT measurement data in post-processing. Calibration at the DUT reference plane has the advantage that the precise characteristics of the fixture don't need to be known beforehand, as they are measured during the calibration process.

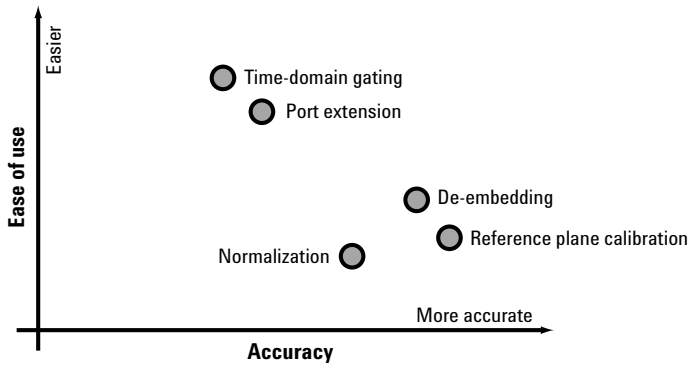


Figure 7. Various mathematical computations and error correction techniques can be made to enhance measurement accuracy. Usually, ease of use and degree of accuracy are inversely proportional to each other.

Unique Time Domain Error Correction Technique

There are three primary sources of error in TDR/TDT measurements: the step generator and connectors, the oscilloscope, and the cables. The shape of the step stimulus is critical for accurate TDR/TDT measurements. The most commonly discussed aspect of the TDR step is the risetime. This is with good reason because a faster TDR step risetime will produce better spatial resolution for resolving adjacent impedance discontinuities. However, an equally important figure-of-merit for a TDR step generator is the level of the aberrations on the step. Aberrations are defined as overshoot and non-flatness. If the overshoot is substantial, the device response error can be dramatic. A good step flatness is anything under 10% of step amplitude.

The oscilloscope can also introduce small errors that are due to the trigger coupling into the channels and channel crosstalk. These errors appear as ringing and other non-flatness in the display of the measurement channel baseline and are superimposed on the measurement waveform. They are generally small and so are only significant when measuring small signals.

Cables between the step source and the DUT can significantly affect measurement results. Impedance mismatches and imperfect connectors add reflections to the actual signal being measured. These can distort the signal and make it difficult to determine which reflections are from the DUT and which are from other sources. In addition, cables are imperfect conductors that become more imperfect as frequency increases. Cable losses, which increase at higher frequencies, increase the risetime of edges and cause the edges to droop as they approach their final value.

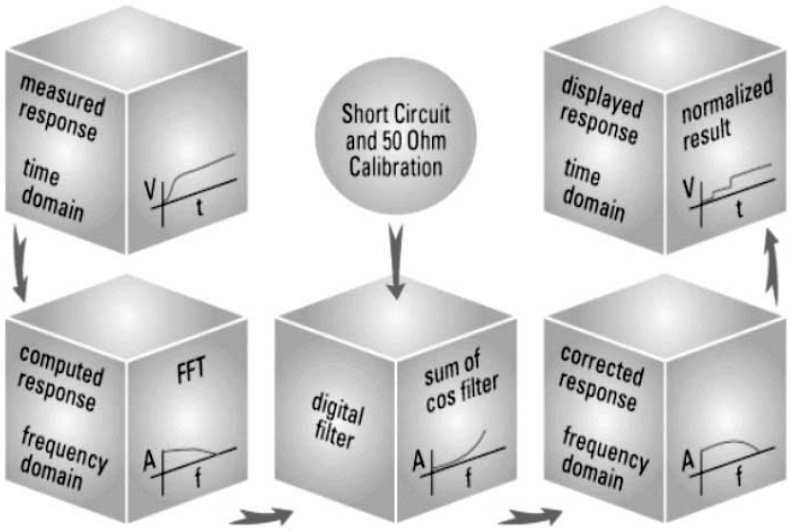


Figure 8. Time domain normalization is an error correction technique that resides in firmware inside the TDR oscilloscope. This technique utilizes the Bracewell Transform developed at Stanford University and removes test fixture error by performing frequency domain math functions.

Design Case Study: Silicon Pipe ChannelPlane

The design case study described in the forthcoming analysis employed the use of a prototype provided by Silicon Pipe of San Jose. The ChannelPlane technology developed by Silicon Pipe creates a well-controlled impedance environment in the area surrounding the backplane/connector interface. Using a process conceptually analogous to optical fiber splicing where the two ends of a fiber are highly polished to achieve a closely matched index of refraction to minimize optical reflections, the ChannelPlane cross sectional copper conductors are polished to minimize electrical reflections. This results in a flush mount cable assembly compatible with the popular 2 millimeter Winchester SIP-1000 backplane connector. The prototype ChannelPlane cable was constructed from high bandwidth Gore G4 material that was cut three inches from the SMA end and terminated with a patented coax/twinax flush mount termination. A coaxial interposer was then used to mate to the Silicon Pipe coax cable. A functional block diagram in Figure 9 shows the construction. A picture of the ChannelPlane assembly with flush mount termination is shown in Figure 10.

Figure 9. The Silicon Pipe ChannelPlane functional block diagram shows construction details.

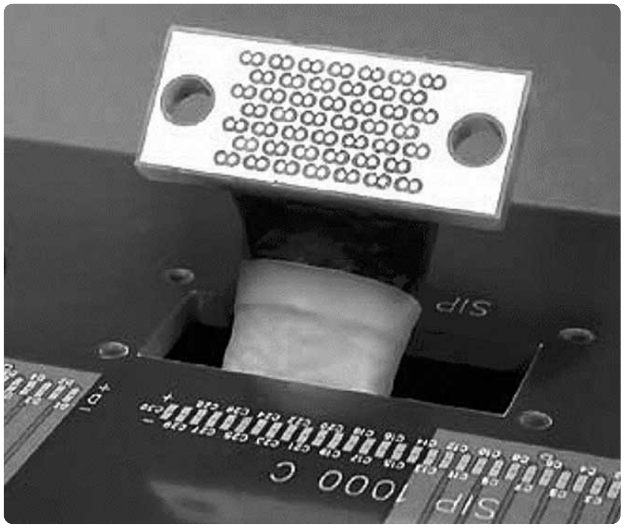


Figure 10. The Silicon Pipe ChannelPlane shown above is a backplane cable assembly that consists of a flush mount connector compatible with the Winchester SIP-1000 backplane connector.

Corrrelation of Two Methodologies

There are many ways to develop models for digital interconnects. An overview of the many possible modeling methods is shown in Figure 11. The method used in this particular design case study is show in the chart in Figure 12. Measurement based models constructed in this design case study combine precision 40 GHz VNA-PLTS testing with TDR-IConnect model partitioning, optimization and test correlation. This method is capable of resolving femtoFarads over 1/10 mm distances even on long cables because of the nature of the VNA instrument. This takes the form of an expanded "time gating" using the model extraction tool to transform the S-parameter data into time domain voltage waveforms. Time domain reflectometry testing is preferred for device model partitioning of paths and can be combined with VNA measurements to resolve small backplane connectors over long distances.

Frequency and time base correlation was required because of the large bandwidth and dynamic range required for this test. It was important to isolate and test coaxial lines with an 80 dB accuracy in order to optimize impedance, insertion and return loss models. The model discovery process requires the ability to detect changes in impedance, risetime and frequency in small connectors embedded in long cables. It will be shown that eye diagram patterns, the ultimate measure of a digital path performance, will correlate well between PLTS and MeasureXtractor. For short electrical length devices, it is desired to have a test bandwidth of 80 GHz using a 7 ps Gaussian input pulse. Where system geometric dynamic range is large, it becomes easier to detect and optimize measurement based models within the model extraction tool fitting measurements to Hspice simulations right in the laboratory. This is a more efficient way to discover, study and optimize the interaction between model attributes.

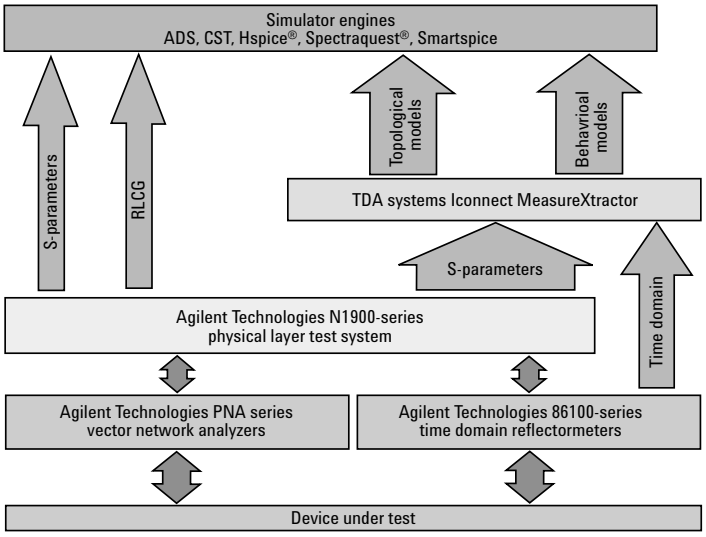


Figure 11. An overview of the many ways to develop models for digital interconnects.

Partitioning the Impedance Profile

Optimized Hspice models must be created by compiling measurement based model schematics in the model extraction tool to make Hspice TDR/T simulations and iterations to refine the match of the measurements as extracted from the S4P files. Both single-ended, differential, even and odd mode simulations can be conducted at the discretion of the engineer. Most importantly, the engineer must check the integrity of all DUT components before diving into model extraction and optimization. For this case, two separate coaxial cables were presumed to match physically and electrically. Both differential leg TDR voltage waveforms were checked for faults before being superimposed as differential or odd/even impedance profiles. In other words, investigating the single-ended impedance of each line of a differential pair separately can yield interesting insight to differential impedance discontinuities.

Behavioral S-parameter measurements were exported into the model extraction tool to construct Hspice topological models. Effectively, S-parameters are "time gated" and "re-time gated" in IConnect until Hspice topological simulations match the measurements. Fortunately this iterative optimization sequence requires only PC work and is easily automated. Both impedance and lossy models were constructed using this methodology. Hspice fitted simulations to the TDR, TDT and S-parameter data enabling the authors to divide and conquer complex modeling applications.

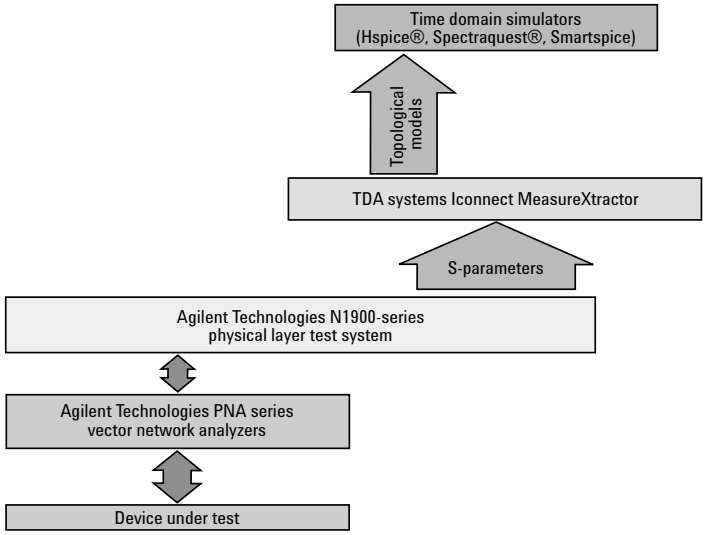


Figure 12. The first model extraction method used in this experiment used measurements from a VNA, then exported the 4-port S-parameters from PLTS directly into MeasureXtractor. A topological model was then exported from MeasureXtractor into Hspice.

Correlating Measurements and Models

As seen on the upper left hand side of Figure 13, the VNA measurement of input differential insertion loss (S_{DD21}) correlates well with the upper right hand side modeled input differential insertion loss (S_{DD21}) of the model extraction tool that imported the 4-port S-parameter file from PLTS. Furthermore, the lower left hand side eye diagram simulation using the virtual pattern generator of PLTS and the lower right hand side of the MeasureXtractor eye diagram simulation matches quite well with each other. In both eye diagram simulations, a similar algorithm was used in each case. The 4-port S-parameter data was used to create an impulse response of the ChannelPlane device. The impulse response was then convolved with an arbitrary binary sequence to achieve a simulated eye diagram. The resultant eye diagram shows the extremely high performance of the ChannelPlane exceeding 40 Gb/s. Future experiments will attempt correlation to eye diagrams measured from a digital communications analyzer and 40 Gb/s PRBS pattern generator.

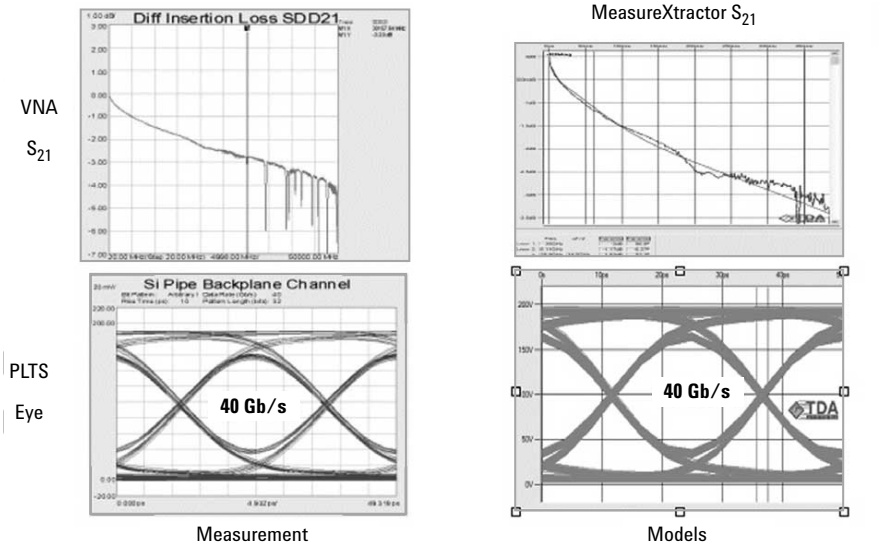


Figure 13. Correlation of input differential insertion loss (S_{DD21}) and 40 Gb/s eye diagram was very good between measurement and simulation.

Hspice Subcircuit Model for Backplane Only

The backplane cable Hspice model was a lossy W-element model of Port 12 and exhibited good signal integrity. Two 50 ohm coaxial backplane cables can be used as 50 ohm single ended or a 100 ohm differential pair. The lossy Hspice W model shown is in RLGC format and includes a skin effect resistance Rac=133 microOhms per root Hertz. It includes a dielectric loss Gac=213 femtoSiemens per Hertz. Both measured and modeled S-parameters are very well behaved beyond 40 GHz. Therefore, the model predicts 40 Gb/s eye pattern as taken directly from the VNA/PLTS test. No extrapolation or correlation was required as shown in eye pattern figures.

Flush mount connectors were then sliced into the ends of the backplane and re-tested on the VNA out to 30 GHz. The four port test data was then exported into MeasureXtractor and partitioned as separate lossy cable and connector capacitance models.

```
.subckt Lossy_Line_34_wire_30in port1 port2 gnd_

W1 N=1  port1 gnd_  port2 gnd_
RLGCMODEL=Lossy_Line_34_wire_30in_Model L=1.0

* RLGC values for W element
.MODEL Lossy_Line_34_wire_30in_Model W MODELTYPE=RLGC N=1
+ Lo=1.66268e-007
+ Co=6.86542e-011
+ Ro=0.102
+ Go=1.14e-006
+ Rs=0.000133
+ Gd=2.13333e-013

.ends
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Figure 14. Hspice subcircuit model of backplane cable without flush mount connector.

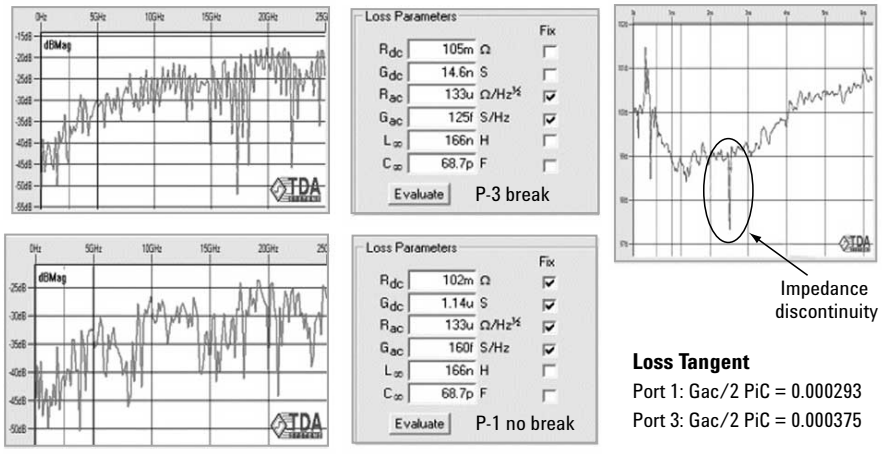

Figure 15. Backplane cable assembly lossy models shows loss tangent with impedance discontinuity due to cable defect on one side of differential pair.

Comparing Discontinuities: Flush Mount Connector verses Cable Break

A physical break in the cable assembly under test can be seen in Figure 16 in green as a capacitive discontinuity that loads down the impedance 2 ohms at a distance of 3 inches from the ends of the cable SMA termination. The objective was to maintain constant impedance before and after minimizing the connector length. A controlled impedance environment can be achieved with a novel fabrication process. Similar to the design goal of optical fiber splicing where the index of refraction is well matched between two fiber cross sectional surfaces, the copper conductor in the ChannelPlane cable assembly has well impedance matched cross sections.

The impedance profile of the damaged single cable was compared to the new backplane cable with connectors. Again, the impedance change and length of the breaks appears very similar. Note the capacitance discontinuity between the two is in the same order about 1/4 to 1/2 pf. The only major difference is the fact that there are two connectors, twice the insertion loss and a slightly elevated return loss.

Impedance profile accuracy could be an issue because the connector slice was only approximately 5 mils wide. The equivalent launched VNA test step risetime was 10 ps with a propagation velocity in the cable being 120 ps/in. The model extraction tool can resolve an impedance profile to approximately 1/10 of the risetime or no less than 1 ps. This translates to 1/120 of an inch or approximately 10 mils. That means cursor placements used to measure connector capacitance on the impedance profile could be off significantly due to resolution issues. Hspice simulations were iterated until a simulated return loss matched the measurement.

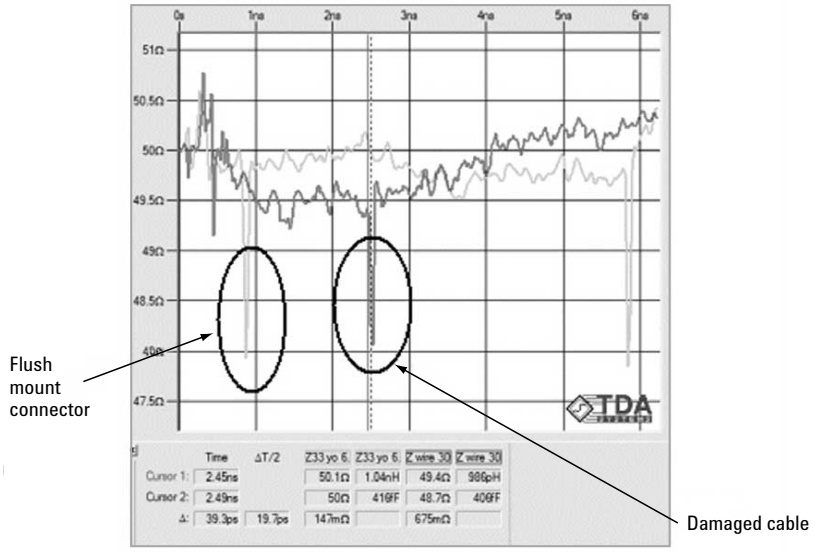

Figure 16. Impedance discontinuities from two different physical structures can look very similar. However, the intuitive nature of TDR's helps discriminate between and break in the cable and the flush mount connector.

Hspice Subcircuit Model for Backplane with Flush Connector

Connectorized cable modeling yielded a similar Hspice model with the same skin effect resistance Rs of 111 u ohms per root Hertz. This was extracted on the 2nd VNA test with the connector sliced into the previously tested cables. However, Gac increased significantly due to the losses in both flush mount connectors. Again, the model extraction tool S-parameters agreed with VNA measurements. However, the eye pattern was degraded over the previous measurements on the cable only. Was it the 10 GHz difference in the bandwidth of the measurements? Or was the degradation solely related to the sliced in flush mount connectors? Since both the eye height and jitter changed less than 20%, it was presumed to be the connectors. Hspice model simulations were fitted out to 30 GHz including connector models with elevated return loss. A valid 40 Gb/s eye verifies that degradations came from connectors.

```
.subckt Lossy_Line_butt_30in port1 port2 gnd_

W1 N=1  port1 gnd_  port2 gnd_
RLGCMODEL=Lossy_Line_butt_30in_Model L=1.0

* RLGC values for W element
.MODEL Lossy_Line_butt_30in_Model W MODELTYPE=RLGC N=1
+ Lo=1.62028e-007
+ Co=6.66083e-011
+ Ro=0.106434
+ Go=0
+ Rs=0.000111
+ Gd=2.86667e-013

.ends
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Figure 17. Hspice subcircuit model of backplane cable with flush mount connector.

Hspice TDR Optimization Schematic Combines Cable and Connector Loss

The second VNA test simulation schematic in Figure 18 includes both backplane cable and connectors. The test objective was to simulate both transmittance and reflectance TDR/T waveforms, convert them to S-parameters and compare them to VNA measurements. Hspice was used to overcome the lost bandwidth between 30 GHz and 40 GHz measurements on the same cable. Simulations replicated insertion loss measurements by adjusting the connector capacitance until a match was achieved. Therefore, the simulated TDR/T waveforms predict valid 40 Gb/s eye integrity using flush mount connectors quite well.

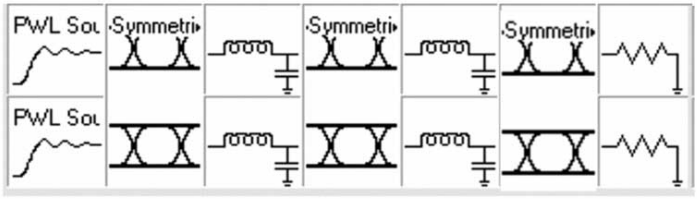


Figure 18. Differential Hspice schematic shows piecewise linear source, lossy transmission line segments, lumped LC flush connector and termination.

Analyzing Connector Shunt Loss

Scaled W-models were interpolated by length from the VNA measurements as a three-inch coaxial launch and termination cables, as well as a 24-inch backplane cable. The partitioned schematic in Figure 19 shows a TDR source, a 3 in cable launch, a flush connector, the backplane cable, another flush mount connector, and a 3-inch termination to 50 ohms. Several Hspice runs simulated the TDR voltage waveform with the objective to match the 10-mv discontinuity in the connector measured by the VNA. Once an optimum fit was achieved, the TDR voltage waveform was converted to S-parameters and re-checked against the VNA S-parameter return loss measurement. Different connector capacitance discontinuity values were iterated starting 400 fF measured in the impedance profile at the capacitive dip. Iterative simulations were used to overcome the impedance profile accuracy issue created by the 30 GHz measurement bandwidth. The simulation matched the -15 dB return loss with a 112 fF connector capacitor.

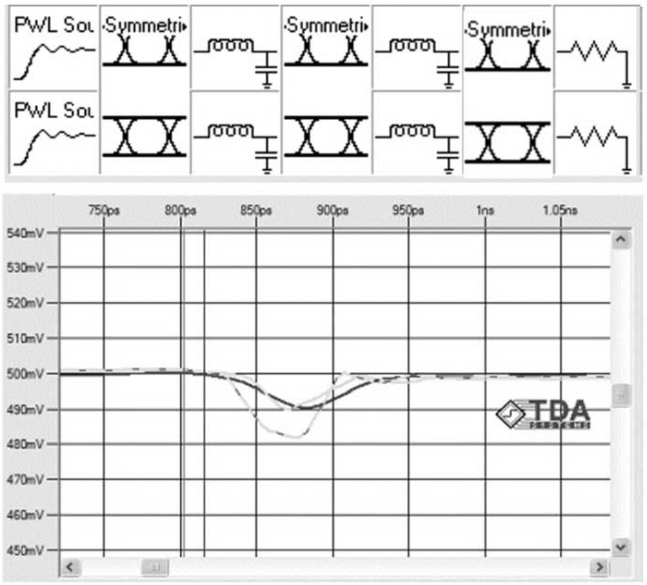


Figure 19. Superimposing the differential schematic of the cable assembly with the impedance profile indicates a connector shunt loss that causes a 5 ps degradation.

Analyzing Fringe Capacitance

The 3D fringe capacitance value of 112fF was extracted from modeling the TDR voltage waveforms (including the connectors) reaching a maximum of -12 dB at 36 GHz. This fit the return loss VNA measurements out to 30 GHz. The modeled backplane insertion loss shown in Figure 20 in Red (S_{21}) fit the -3 dB attenuation at 25 GHz measurement made on the VNA. The Blue (S_{21}) backplane cable attenuation without connectors was -3 dB at 35 GHz. With reflection peaking at only -12 dB, the extrapolated S-parameters appear valid out to 40 GHz. Given the small 5 ps risetime degradation, this model accurately predicts a 40 Gb/s eye with a 90 mv height and a 2.4 ps peak-to-peak jitter. If the backplane flush mount connectors are extremely well matched in impedance, then these losses should decrease to -15 to -20 dB.

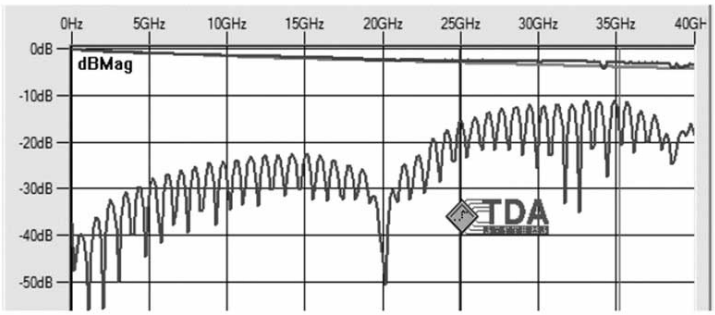
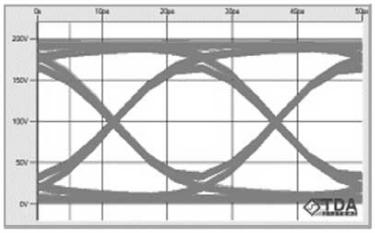


Figure 20. Simulated insertion loss (top) and return loss (bottom) for 30" backplane cable assembly with 112femtoFarad connector.

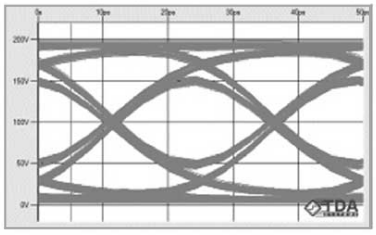
Modeled Eye Diagram With and Without Connectors

The shunt losses in the connectors degraded the input risetime by 5 ps and lowered the eye height to less than 100 mv. The 30 ps measured output risetime can be seen in the eye diagram across the 2 unit interval risetime; starting at the left side (approximately 10%) and reaching 30 ps at the center top (approximately 90%). Note that a 20 ps by 75 mv valid eye mask can be constructed inside this eye.

PLTS 32 bit eye pattern jitter doesn't appear significantly larger than the IConnect 10 bit PRBS data patterns shown here. A key point is the connector TDR discontinuity is short enough to minimize reflections sufficiently to not deteriorate eye opening. For this to occur, the return loss needs to exceed -10 dB. So both a lossy component and a capacitive component are required to model precision flush mount connector insertion and return loss.



Left shows eye without conectors
Jitter PP: 2 ps
Eye height: 130 mv



Right shows eye with connectors
Jitter PP: 2.4 ps
Eye height: 90 mv

Figure 21. Modeled eye diagrams with and without connectors.

- Cable backplane flush connector Break model
- Only 20% jitter increase
- 5 ps I/O Tr degradation
- 8 dB more return loss
- Insertion loss unchanged
- Dual flush mount connectors 10 mv discontinuity is a 112 ff 3D connector fringe capacitor on ends of 30" backplane

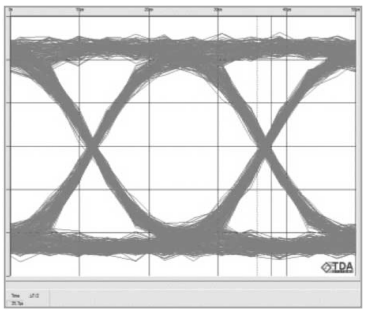


Figure 22. Modeled eye diagrams with and without connectors.

Conclusions

A comparison of two measurement-based modeling techniques have been presented that utilize 4-port S-parameters. These modeling techniques were applied to a novel high-speed differential interconnect that employed the SiliconPipe ChannelPlane technology. This flush mount connector was fabricated by a precision slicing of a copper conductor cross-section as if it were a fiber optic cable. The polished copper cable interface has been shown to minimize impedance discontinuities and return loss at the connector interface. If this type of copper interface were polished to a higher degree of surface quality, it is estimated that the connector could achieve a return loss as low as -20 dB. The correlation of measurements to models was very good. Also, the risetime, eye Diagram patterns and S-parameters correlated quite well.

The commonly used Touchstone format of 4-port S-parameters (.s4p) resulting from the 40 GHz VNA measurements was directly exported from Agilent's physical layer test system software and imported into the TDA Systems IConnect model extraction tool. After refining and optimizing the model with multiple iterations within IConnect, a simulated 40 Gb/s eye diagram was obtained. This 40 Gb/s eye diagram was then compared to the 40 Gbps eye diagram derived from the internal PLTS eye diagram generating algorithms. The qualitative correlation of these two simulated eye diagrams was very good.

The advent of high-speed serial channels has driven today's circuit topology to differential architecture. While this enables the inherent benefits of coupled transmission lines, this adds new challenges for the signal integrity engineer. Measurement, model extraction and simulation are critical to an efficient design cycle and meeting time-to-market demands. It sometimes seems as if there are as many design tools as there are design engineers, but the message is clear. New techniques that utilize measurement-based modeling are necessary for fully characterizing differential interconnects. It is now possible to use one measurement system for both time and frequency domain information that will quickly identify design flaws that ultimately degrade performance.

References

Content herein presented at the International Engineering Consortium - DesignCon 2004, Santa Clara, California.

Jim Mayrand, Mike Resso, Dima Smolyansky, “Utilizing TDR and VNA Data to Develop 4-port Frequency Dependent Models”, International Engineering Consortium DesignCon 2004 Proceedings (High Speed Interconnect Track), Santa Clara, California, Feb 2-5, 2004.

Web Resources

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