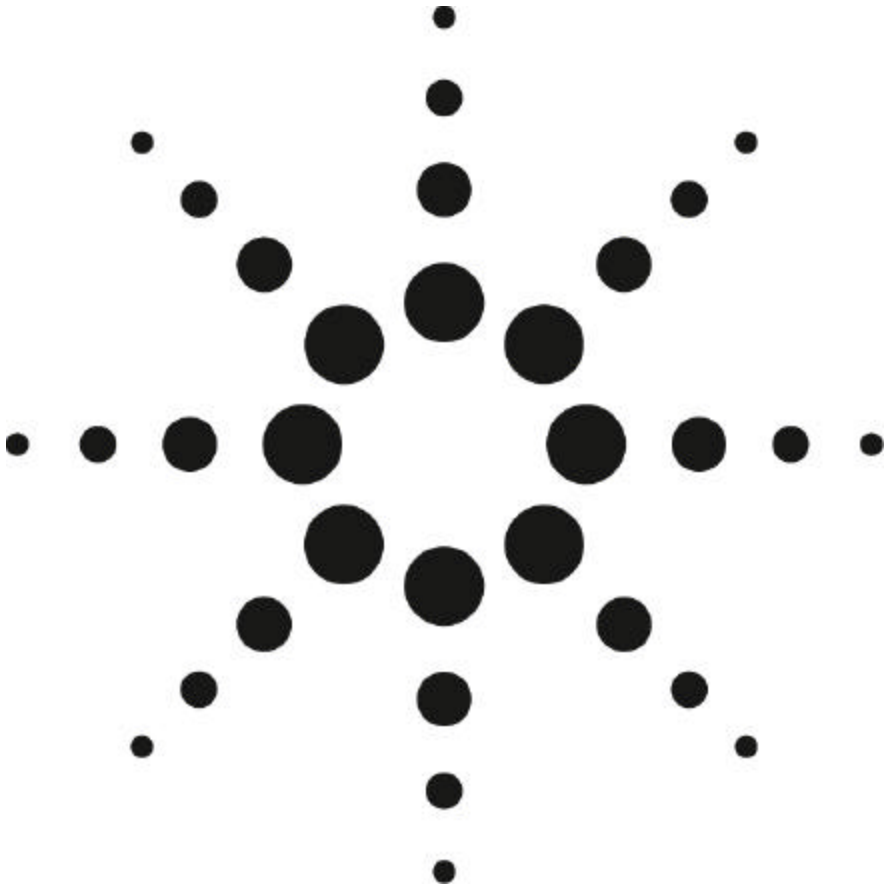
The Path to 10 Gb/s:

Connector and Backplane Capabilities for High-Speed Applications

White Paper



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Connector and Backplane Capabilities for High-Speed Applications

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Abstract

As backplane data rates migrate toward 10 Gb/s and beyond, there is an ever-increasing expectation for level of performance of every component in the data stream, including the optical transceivers, physical layer ICs and connectors. This paper looks at modeling the performance of three different backplane connectors and their usability for various data rates such as 2.5, 3.125, and 5Gb/s. The modeling tool is Agilent Advanced Design System (ADS™), which is used to model a backplane system given raw S-parameters of each particular connector. If you have raw S-parameters for a connector, ADS allows you to simulate the backplane environment for any configuration of line length, width, adjacent channel spacing or board stackup, producing results in the time or frequency domain. We show that this method is viable enough to potentially eliminate the need to build a backplane to prove suitability of a particular connector or other component for a specific application.

The Problem: How to Simulate Backplane Performance Without Committing to Hardware

In order to have a successful high-speed data link a signal must successfully pass from transmitter (say a physical layer SerDes operating at serial rate of 2.5 Gb/s) to receiver. In some cases the signal medium is optical fiber. In others (say XAUI at 3.125Gb/s operating from line-card to backplane) the medium is a PCB with a connector attaching the line-card to backplane. Since the transmission medium is such an important factor determining signal quality and success of link, it is helpful for chip and system designers to have models that predict whether a particular data rate or electrical line length will work within a system. For this study we focused on three different backplane connectors in an attempt to see whether basic connector models could be used to accurately predict transmission quality within a larger system. The connecters we focused on were: (1) VHDM™ (Teradyne), (2) Speedpac + ™ (Tyco Electronics), (3) HB™ (FCI-Electronics), and (4) Micro GigaCM™ (Fujitsu). The VHDM™ connector is a thru-hole modular connector. The connector used in this study was an 8-row version based on a 2mm x 2.25 mm grid. A thin ground plane separates each 8-signal column. At the time the backplane was built this was the latest connector from Teradyne. However Teradyne now offers a differential connector (called the HSD connector) that is form-factor compatible with the module that we tested and is a true differential connector.

The Speedpac+™ is a connector that is surface-mounted to a backplane board. It uses a zero-insertion-force mechanism to clamp onto both sides of a daughtercard to make surface connection with pads on the daughtercard. The differential Speedpac+™ model (what was used here) utilizes a 2.5mm pitch per signal pair.

The HB™ connector is a thru-hole connector that is based on a 2.5mm x 2.0 mm matrix. Each differential pair is in a twin-ax configuration and is surrounded by a ground plane. All of the connectors are controlled-impedance connectors.

We also measured a Fujitsu connector that was an early version of the MicroGigaCM ™ connector. The model that we measured was a surface-mount connector with 24 differential pairs lined up in two rows. Each pair is separated by a ground plane and has a 1.5mm channel-to-channel pitch. However the design of the connector changed just prior to our completing this experiment and we didn't have time to incorporate the connector system simulations results into this paper. We do show an eye measurement through the isolated connector.

Figure 1 shows photos of the backplane board and daughtercard with the four connector types. The backplane board measures 22" x 16" and the daughtercard measures 15 ½" x 14".

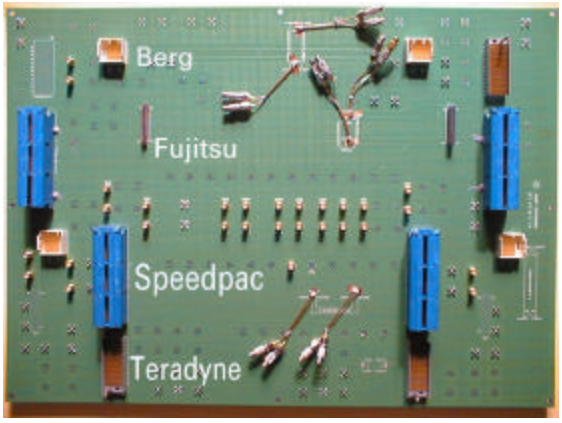

Figure 1a: Backplane and connectors

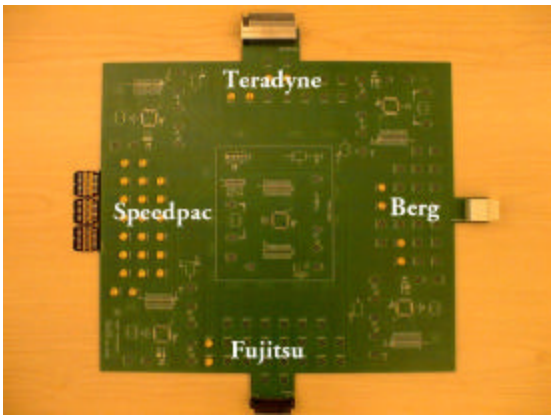

Figure 1b: Daughtercard and connectors

Introduction to ADS

Agilent Advanced Design System (ADS) is a comprehensive software simulation environment that performs circuit and electromagnetic simulations among other things. The circuit simulation tool within ADS has various built-in models of PCB structures, such as strip-line and micro-strip lines for arbitrary material constants (such as relative permittivity and dielectric loss tangent) and planar geometry constants (line length, line width, line separation, inter-dielectric heights, etc.) We were attempting to show that if someone is armed with a measured "model" of the connector and a simulation tool such as ADS they can arrive at system-level models that accurately predict transmission characteristics. The value of this approach is that it is no longer necessary to build hardware in order to gauge the signal-worthiness of the overall inter-chip copper transmission system. Circuits are built up within the ADS schematic tool. The blocks within an ADS circuit (analogous to ".models" within SPICE) can either be empirical measured models of connectors or built-in models of board traces or vias. These models are frequency-based. The measured "model" for each connector is a citifile containing S-parameter measurements done on a network analyzer, (in our case an Agilent 8510B.) ADS has a circuit simulator tool to predict time-domain results (e.g. eye waveforms or time-domain reflectometry plots) or frequency-based results (overall Sparameters) for the overall system "circuit".

The empirical model for each connector is a set of frequency-based S-parameters. Figure 2a gives a brief review of S-parameters for a two-port system.[1] Figure 2b defines the 4-port S-parameter system that is applicable for our study (since we measured differential paths through each connector and across the backplane and daughtercards.)

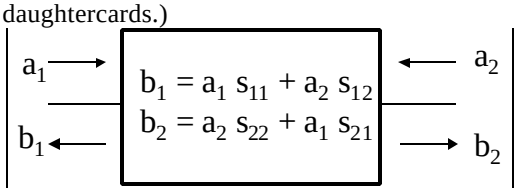

Figure 2a: Review of 2-port S-parameter Definitions

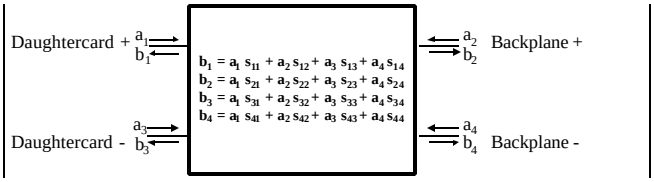

Figure 2b: 4-port S-parameters for differential ports

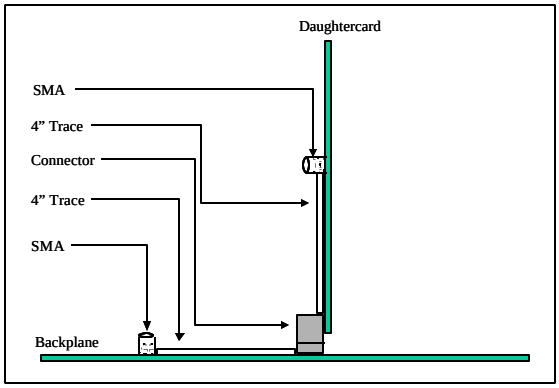

Figure 3: "empirical connector model" elements

First, Baby Steps

The first step in this approach was to verify that the conversion between time and frequency domain of our models was accurate. We started with the S-parameter model of the connector "by itself". (Figure 3 shows the board topology of the basic connector "block".) The connector model is composed of: Daughtercard (SMA to 4" trace to connector half) to Backplane (other connector half to 4" trace to SMA). This S-parameter set therefore becomes the "library model" for the particular connector measured.

This library model was used within an ADS circuit to generate a time-domain eye. (Figure 4). The block in the middle of the circuit is the S-parameter "model" for a Speedpac™ connector (in this case). The pulse generators amplitudes were each set to 0.866 V each to correspond to the BERT output pk-pk output of 0.866 V when the BERT differential amplitude was programmed to 1.0 V (pk-pk).

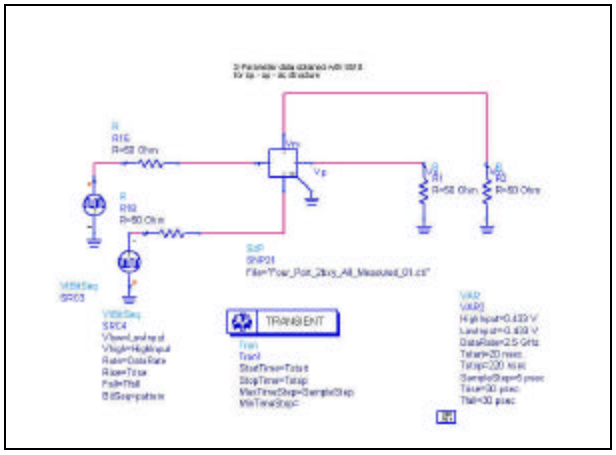

Figure 4: Circuit for Time Verification of Connector Model (Speedpac shown)

The eye from the transient simulation was compared with the time-domain eye measured on each connector. The input source for the eye measurement was a differential source from an Agilent 71612B (12Gb/s Bit Error Rate Tester-BERT.) The comparison for each connector (Figure 5) shows a similarity of shape and a close approximation of amplitude. The resemblance of shapes and close matching of amplitudes between simulation and measurement suggests that our frequency to time conversion is sound and that the connector "models" are good.

The True Test

The obvious question at this point is whether the empirical connector models can be used within an ADS circuit to predict results for various backplane topologies. It's easy enough to move from frequency to time domain for a simple connector block but when the block is combined with other models within ADS (such as a second block or a length of backplane stripline), is the result accurate?

To answer this question, we ran simulations using our empirical models for the FCI Electronics, Teradyne, and AMP connector types using 12" and 18" built-in ADS models at bit rates from 2.5Gb/s to 5 Gb/s. We also did measurements on our board confirming that the ADS simulations were accurate. Figure 6 shows the list of simulations that were carried out.

At this point in the project, there were some challenges. One challenge was that our board topology differed slightly from the topology represented by the "connector model". Namely, there are two extra SMAs that are not physically present on the system backplane traces between the two connectors. (Refer to figure 7.) Because SMAs have noticeable return loss at these rates, their inclusion in the simulation signal path

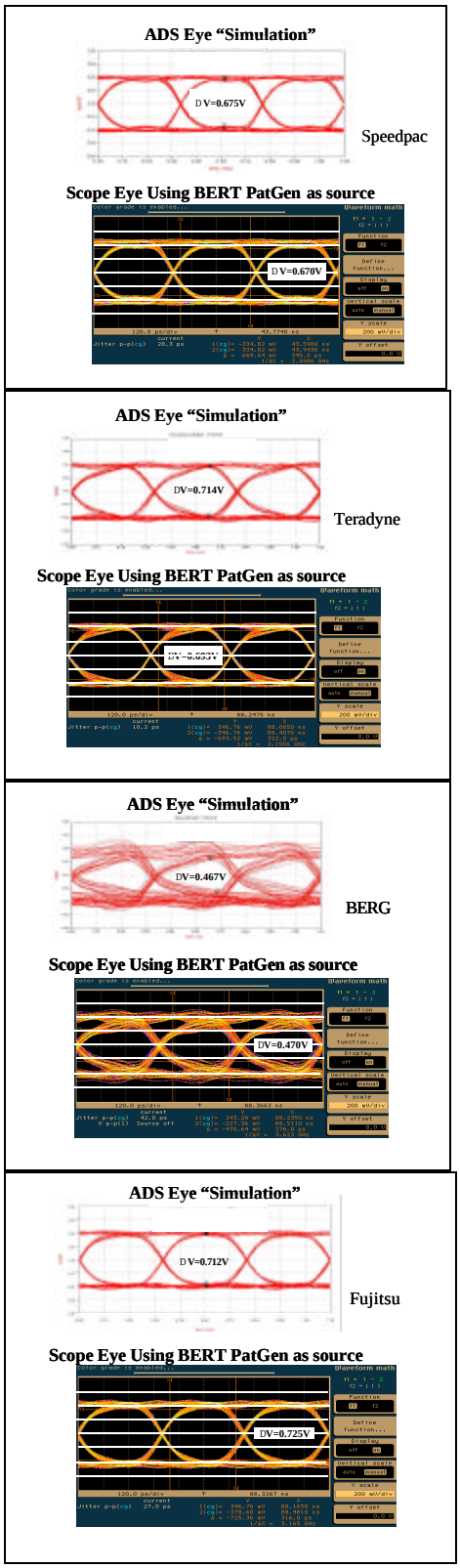

Figure 5 - Comparison of Scope eye to ADS f-to-time conversion for four connectors

Connector	Length of inter-connector trace	Rate (Gb/s)
Berg	12" 18"	2.5 3.125
Teradyne	18"	3.125
Speedpac	18" 18" 18"	2.5 3.125 5

Figure 6 - Multi-Component Simulations

expectedly caused some degradation of simulations versus what was measured (and this is what we observed.) To help solve this problem, we employed a built-in feature of ADS known as a "de-embedding block." This block is itself an S-parameter network. What the block does is remove the effect of the network that is within the de-embedding block from the circuit. In other words, it "de-embeds" the effect of its own network from the rest of the circuit. In our case, the de-embedding block was a 1.5" trace with an SMA connector on either end of the trace. By employing this de-embedding block (figure 8) the effect of the SMAs from the backplane end of each "connector block" was removed. (In reality there is a slight concern in that the RHS SMA of the de-embedding block is adjacent to a stripline and immediately adjacent to the RHS connector block. However, this ended up not being a large effect in most cases, perhaps because the 2nd backplane SMA is further into the signal launch and plays a smaller effect on the signal quality than the initial one. (Consider that signal rise-time is filtered by the time the signal hits this SMA; therefore it should play a smaller role than the upstream SMA on the right-hand side of the LHS block.) Further refinements will involve using two de-embedding stripline structures, each which has an SMA on one end and a "transparent" high-speed probe launch as the port on the other end.)

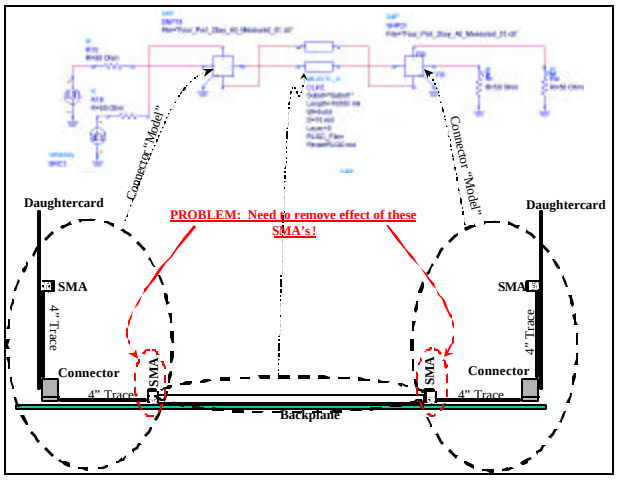

Figure 7 Simple ADS Circuit shows Extra SMA's that aren't in actual backplane

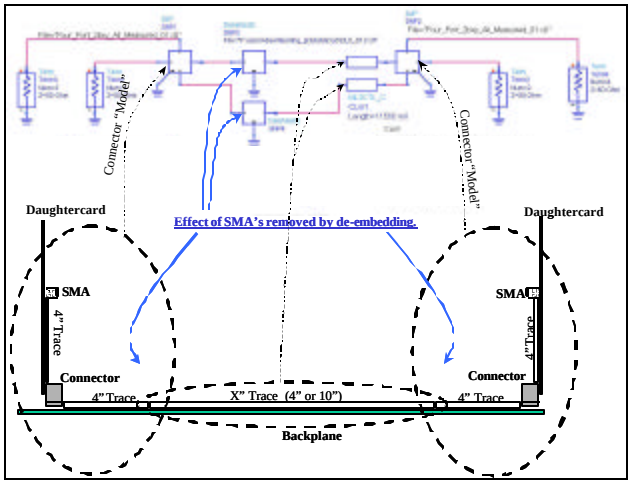

Figure 8: De-embedding circuit for removing effect of extra SMAs

Test Results

Eye measurements were taken with each of the combinations of length, data rate, and connectors listed in Figure 6. These combinations were chosen because they stressed each connector to the limit of its respective performance. The measure of "agreement" was taken as the internal opening at the time of maximum eye opening. (This didn't necessarily occur in the middle of the eye for non-symmetric eyes.) In most cases, the agreement between simulation and measurement is quite good, as can be seen in Figure 9. Discrepancies ranged from 5% to 17%, but the average difference was 7%. The largest discrepancy was seen for the HB Metral™ connector at 2.5Gb/s for a 12" trace. Considering that this plot is the only result given for the shorter trace length (12") it is not surprising. The effects of the

"negative SMA" discontinuity (due to the de-embedding block) and the positive SMA discontinuity (due to the dangling SMA on the RHS connector "block") will be attenuated more by the longer trace length (and hence will be less of an effect) than for the shorter trace length. Future measurements and simulations will confirm whether this is true.

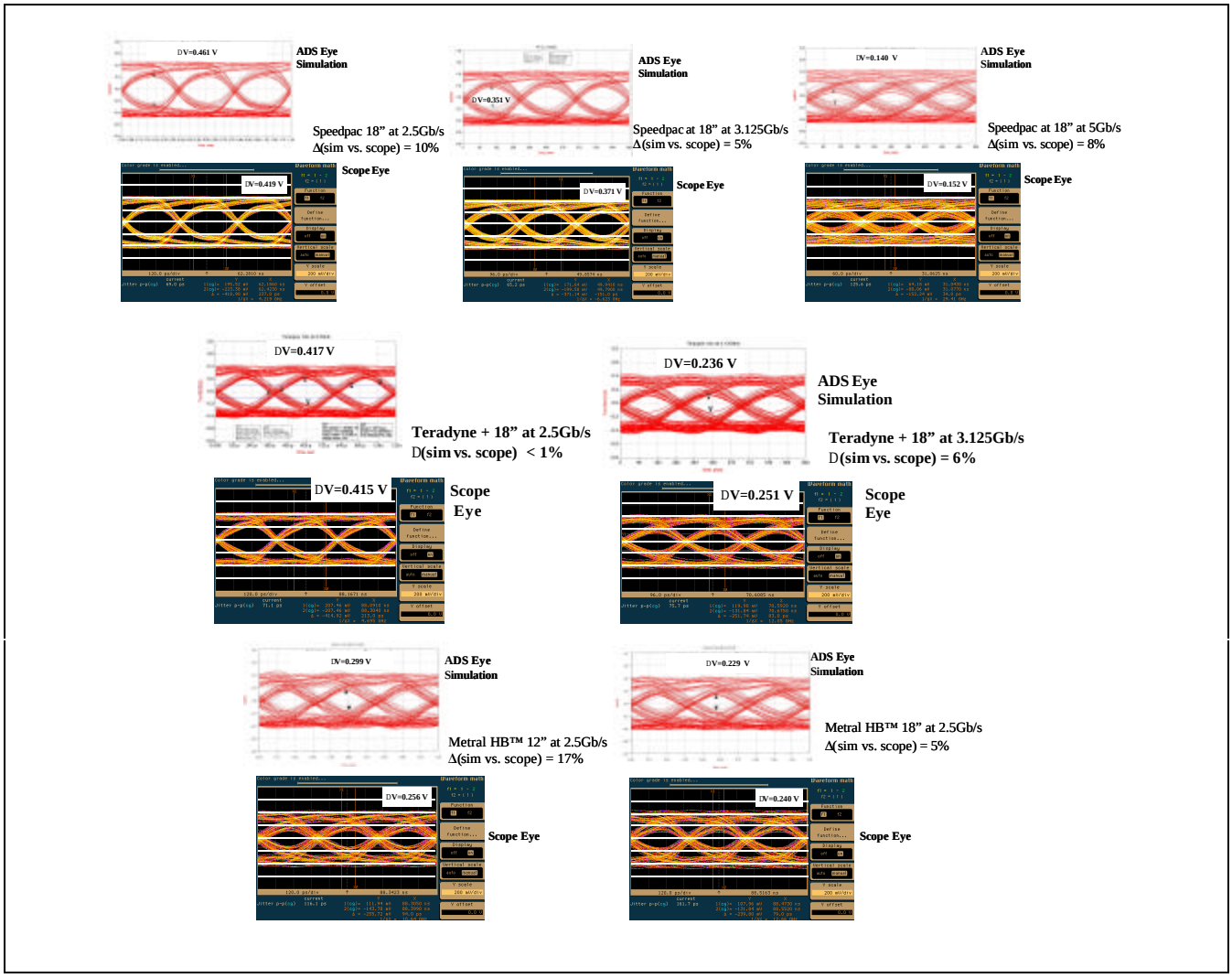

Figure 9 - Comparison of daughtercard/backplane/daughtercard simulations to scope measurements

Summary: Applicability for other systems

The value of the frequency-based modeling methodology is that it allows one to construct eye diagrams using ADS and measured S-parameter building blocks (for connectors). We've shown that in most cases quite reasonable agreement can be obtained between simulations and measurements. Further refinements (such as a more refined de-embedding block) should help tighten agreement between simulations and measurements. Once this is done, further simulations can be done to predict backplane/connector performance at a variety of speeds and conditions without needing to spend time and money constructing expensive PC boards.

Future studies can involve looking at other important signal integrity issues, such as cross-talk with different line densities. In this way, the usefulness of the ADS tool will continue to be extended.

Bibliography:

[1] Agilent Technologies Advanced Design System 1.3 CIRCUIT SIMULATION manual Ch4 pp 4-11 – 4-12. Nov. 1999.

[2] Agilent Technologies Application Note 154: **S-Parameter Design** (adapted from***S-Parameter Design Seminar*** video series.) 1990, 2000.

[3] Thanks to Rick Walker, Bill Brown, and Patrick Lee for analysis ideas and assistance in tracking down conversion errors in the inverse FFT operation.

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