10GbE Technology and Device Characterization

Introduction

10GbE merges data communication and telecommunication and is the natural evolution of Ethernet in speed and distance. It defines two PHY types: LAN PHY and WAN PHY. This modularity is based on an interface called XAUI, which is a low pin count, self-clocked serial bus evolved from Gigabit Ethernet. The XAUI interface speed is 2.5 times that used in Gigabit Ethernet. By arranging four serial lines, the 4-bit wide interface supports ten-times the data throughput requested by 10GbE.

This definition drives the technology but also enables a high port count per switch volume.

A multitude of component vendors drive different "Multi-Source Agreements" (MSAs). Figure 1 on page 2 provides an overview on the agreements achieved over the last few years. These are accompanied by the activities of various standardization bodies, the most important of which for 10GbE is the IEEE802.3ae which was released in June 2002.

A wide range of measurements are described in the 802.3ae Standard, including optical transmitter and receiver testing, electrical XAUI test and jitter testing.

XAUI eliminates the alternative 36+36 bit wide TX and RX PCB trace with its associated skew problems and migrates skew into the logic layer. XAUI has its own set of test and measurement opportunities and needs. Many of the tests are essentially eye mask measurements. This paper focuses on tests that specifically require a parallel BER test set and will show how the Agilent Technologies ParBERT 81250 can be used in these applications.

10Gb/s Transponders

	Speed	XBI	XFP	XENPAK	XPAK	X2
optical	Gb/s					
SONET/SDH	9.95	✓	✓	✓	✓	✓
VSR-4	9.95					✓
10GbE 802.3ae	10.3		✓	✓	✓	✓
10GFC	10.5		✓		✓	✓
G.709	10.7		✓		✓	✓
electrical		300 pin SFI-4 like	30 pin XFI 10Gb/s	XAUI	XAUI, SFI-4/P2	XAUI, SFI-4/P2, FC

Table 1

The first higly integrated 10GbE solution was the XENPAK module. Since then there have been successors which cover 10GbE as well as other technologies such as SONET, VSR, 10 Gigabit FibreChannel and G.709 (see table 1 on the previous page for all supported combinations). The 10GbE capabilities remain the same in all implementations. The following document explains 10GbE technology with help of the XENPAK example. The later implementations basically differ with smaller form factor and lower power consumption. Electrically/optically they comply to the same functionality and specifications.

XENPAK Overview

In 2001, Agilent and Agere jointly announced the multisource agreement for 10 Gigabit Ethernet Transceiver Physical Standards "XENPAK.org". This has since been joined by a number of other companies. XENPAK is a module as can be seen in figure 1, and is small enough to fit in the palm of your hand. On the front are two fiber connections, and on the rear is the electrical connection for data power and control. The data interface is of XAUI type. The XENPAK module is used on line cards to do the data transport within a few meters up to 40km.

Figure 2 shows the data flowing from/to the Media Access Control (MAC) which is the Data Link Layer in the OSI model (See Figure 3). The interface to the XENPAK is based on XAUI, common to each type of XENPAK.

There are 7 types of XENPAKs defined: 3 WAN PHYs, compatible to SONET and 4 LAN PHYs. 3 of the LAN PHYs work with a 10.3 GB/s data stream, the LX4 type works with 4 data streams coded to different colors (WWDM), transmitted via one fiber.

The different types are suited for different length of fiber. Generally the longest wavelength makes the longest link. With up to 40km link length,

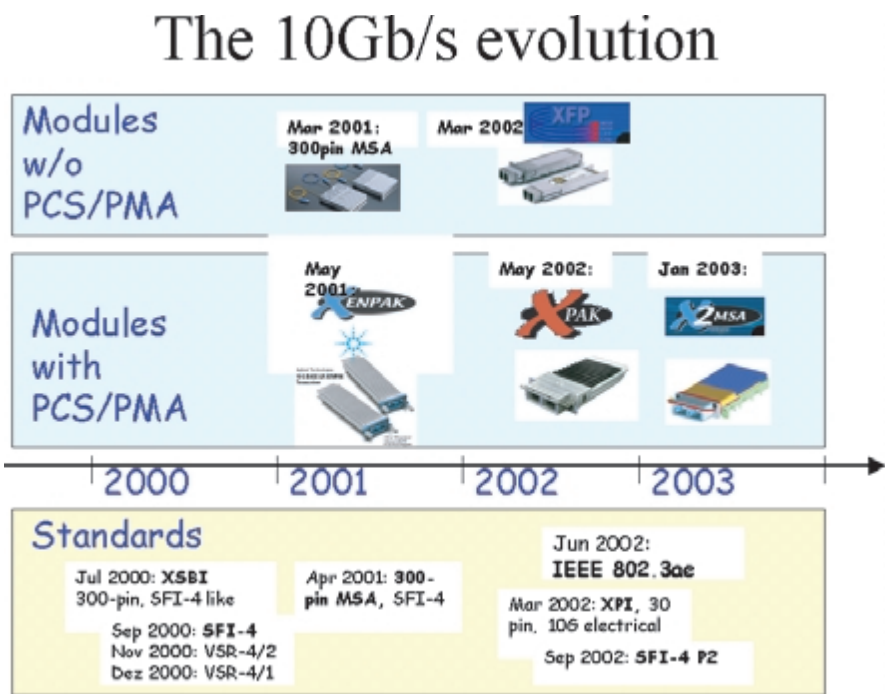

Figure 1

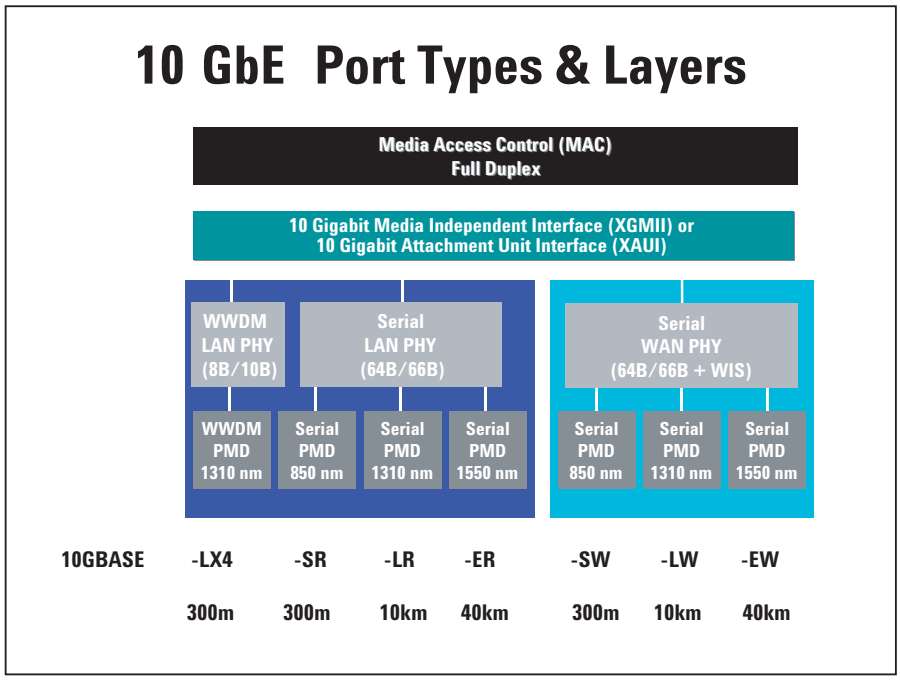

Figure 2

the Ethernet technology competes with the traditional SONET technology used in the Metropolitan (MAN) area. With the WAN Phys in place a very flexible networking architecture from WAN – MAN – LAN is possible.

OSI Seven-Layer Model

In the 1980s, the International Standards Organization (ISO), began to develop its Open Systems Interconnection (OSI), which has influenced Internet protocol development. In the model shown in figure 3, a networking system is divided into layers. Within each layer, one or more entities implement its functionality. Each entity interacts only with the layer beneath and above it.
The seven layers of the OSI Basic Reference Model are (from bottom to top):

The **Physical Layer** describes the physical properties of the various communications media, as well as the electrical properties and interpretation of the exchanged signals. i.e. this layer defines the size of Ethernet coaxial cable, the type of BNC connector used, and the termination method.

The **Data Link Layer** describes the logical organization of data bits transmitted on a particular medium, i.e. this layer defines the framing, addressing and checksumming of Ethernet packets.

The **Network Layer** describes how a series of exchanges over various data links can deliver data between any two nodes in a network, i.e. this layer defines the addressing and routing structure of the Internet.

The **Transport Layer** describes the quality and nature of the data delivery, i.e. this layer defines if and how retransmissions will be used to ensure data delivery.

The **Session Layer** describes the organization of data sequences larger than the packets handled by lower layers, i.e. this layer describes how request and reply packets are paired in a remote procedure call.

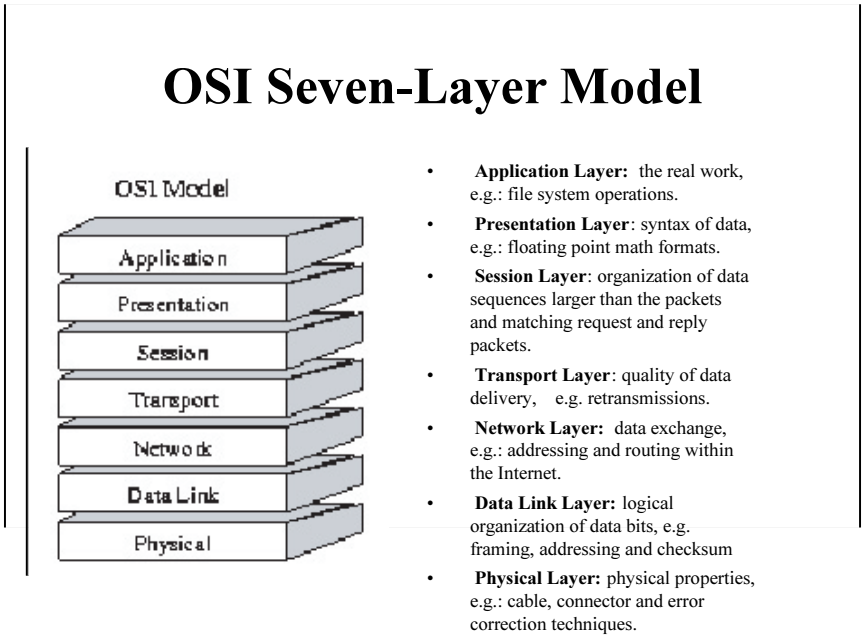

Figure 3

The **Presentation Layer** describes the syntax of data being transferred, i.e. this layer describes how floating point numbers can be exchanged between hosts with different math formats.

The **Application Layer** describes how real work actually gets done.
i.e, this layer would implement file system operations.

The original Internet protocol specifications defined a four-level model, and protocols designed around it (like TCP) have difficulty fitting neatly into the seven-layer model. Most newer designs use the seven-layer model.

The 10GbE implementation mainly deals with the physical layer. Other layers are not affected as long as the 10G data bandwidth is maintained through the upper layers.

The **Reconciliation sub layer** takes over the data from the DATA Link Layer with the XGMII interface. The XAUI interface is available at the extender sub layer (XGXS). Before the signal is put to the fiber (Medium), the Coding (PCS) and Medium (PMA & PMD) sub layers prepare the signal.

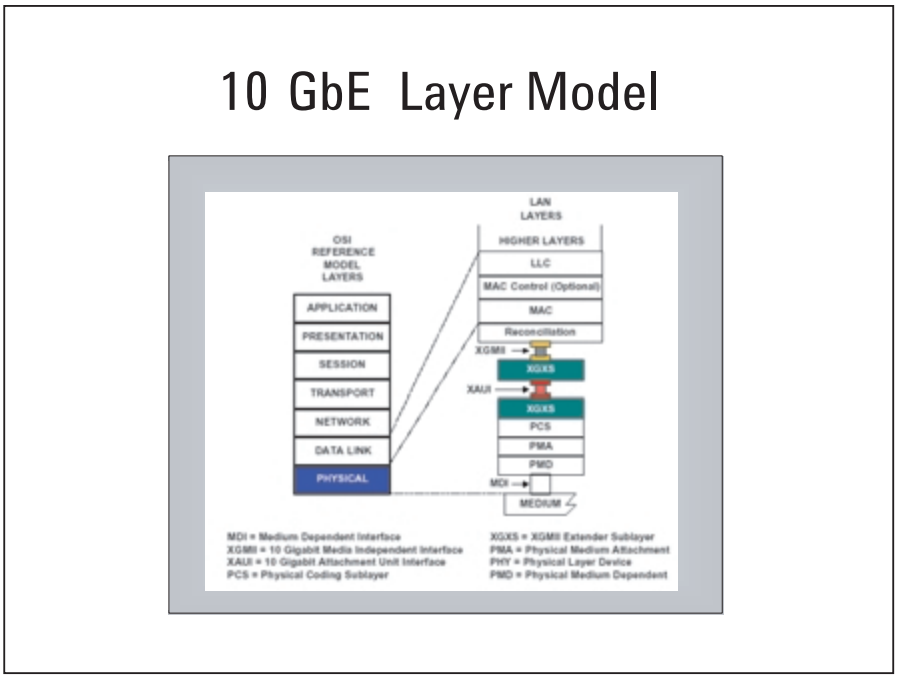

Figure 4

The XGMII interface is an 'evolution' from GbE. In order to obtain 10x the bandwidth from the GMII interface, the number of data lines increased to 2x 36 + 2 clocks. However, this type of bus is not a good solution to transmit data over a distance of 50cm, which is the typical distance inside the router between line card and switch fabric. This is the reason the XAUI interface was invented to be the physical media to bridge the gap.

XAUI consists of 4 lines up and 4 lines down running at 3.125GB/s. The lines are differential and there is no longer a clock.

Originally the idea was to use a simple chip to built the serializer/deserializer function and the XGXS layer function. Today's ASICs allow the integration of framing function and the XGXS functions on one chip. So on a XENPAK module there is basically one large chip working from the XAUI to the Laser and optical Receiver.

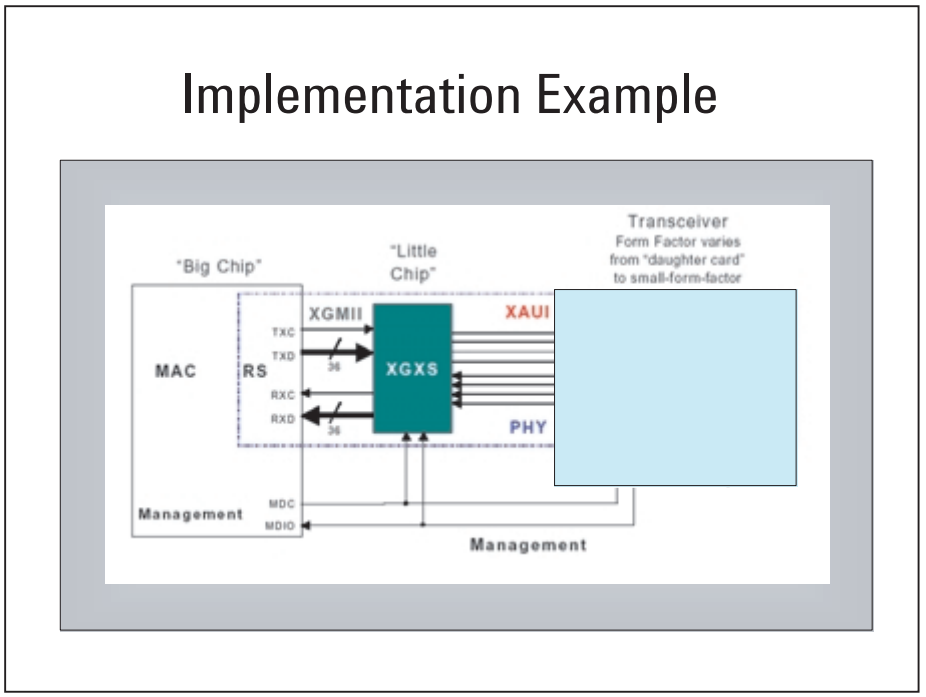

Figure 5

The XAUI electrical interface is based on low swing differential signals. It is a point to point connection. AC coupling is required at TX out and RX in. The link compliance point is defined to the receiver input, and the link length is typically 50 cm.

Differential transmission techniques are a good investment to eliminate common mode noise and reduce Electromagnetic Interference (EMI). Common mode noise on a non-differential interface lowers signal to noise ratio, and can completely corrupt data. On a differential connection the receiver operates from the difference of input to complement input, so common mode noise cancels there by itself. The trade-off of a differential connection is that it needs two physical lines for each data lane. Therefore connector layout, PC board layout and wiring are always twice the size.

XAUI adds AC coupling to the interface. This is a further improvement of common mode rejection. But this is a high price to pay: AC coupling does not have bandwidth down to DC. There is a low frequency limit, below this frequency the signals will start to droop heavily and the link may not operate error free. As a consequence, two requirements must be fulfilled:
1) any data sent must maintain the same average number of '0's and '1's. Some people call this 50% duty cycle, others call this Disparity. For equal distributed '0's and '1's the Disparity is 0.

2) If the link starts from idle, there is a settling time before the data can be transmitted. As this is not acceptable, the link is not actually quiet in idle. There are specific characters transferred which have the idle meaning. So physically there is activity with duty cycle 50% needed on the link at any time.

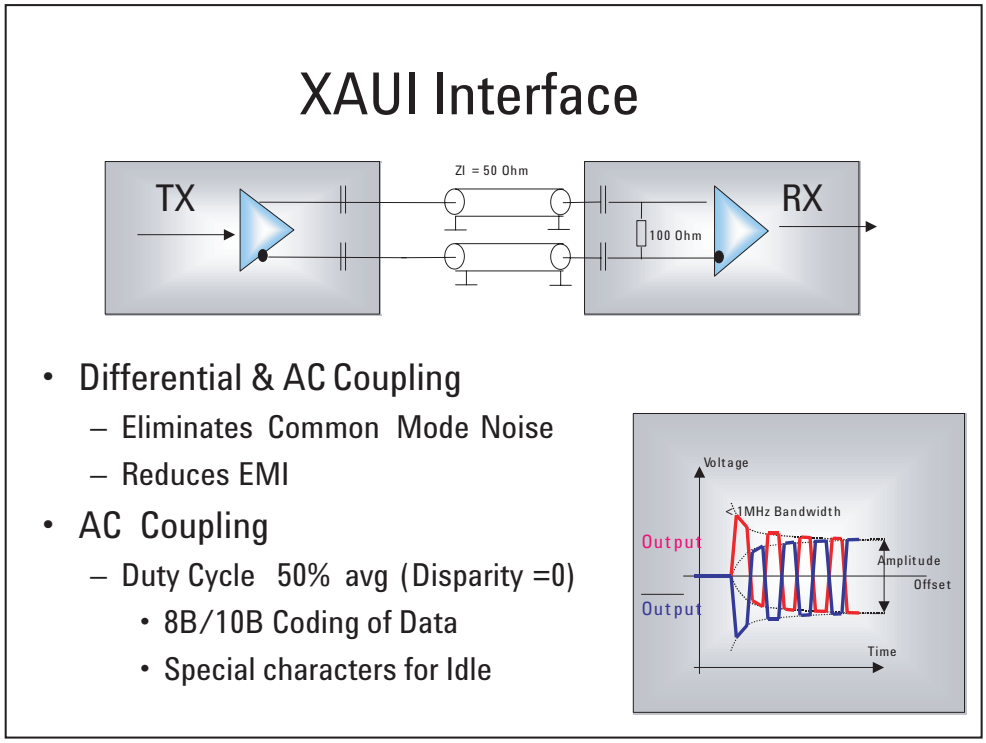

Figure 6

These requirements are achieved with help of the so called 8B/10B coding. This transforms an 8 bit character into a 10 bit word. So at 8 bit there are 256 characters, at 10 bit there are 1024 characters possible. The trick in the transformation is to use those 256 characters from the 1024 available, which have equally distributed '0's and '1's.

Beside the 256 data characters a few more 10bit words would be allowed with special meaning, e.g. idle, shown later in the application note.

Details on the XAUI Interface:

There is a specific Eye Mask defined for the transmitter to deliver its signal to the receiver. This is measured after 50 cm line length. The transmitter must maintain an Eye Opening of at least 55% according to the graph taken from the 802.3ae standard.

The receiver must recognize the input signal for a BER figure of 10^{-12} with additionally sinusoidal AM modulation. This modulation closes the eye opening down further to 37%.

Detailed information and requirements regarding jitter measurements within the 802.3ae standard can be found a few figures later on.

Another fundamental piece of the Ethernet architecture is that every system or sub-system runs on its own internal reference clock. To make designs cheaper, there is a specification of +-100 ppm for the accuracy of these oscillators. As this includes basic tolerances and any drift, there is no stable phase relation between the clocks inside the two parts communicating with one another. In other words: the clocks are asynchronous.

Figure 8 shows transmitter (TX) and receiver (RX), both with their own individual reference clock inside. The transmission of data is built in such a way that user data is packaged into frames. In between frames there is a minimal time where idles are transmitted.

This basic concept here is to have redudancy with the transmitted data to allow skip or insertion of specific bytes at the receiver side to compensate for clock speed tolerance. If the transmitter is slightly faster, the receiver is allowed to remove a byte, and if the transmitter is slightly slower it is allowed to insert a byte.

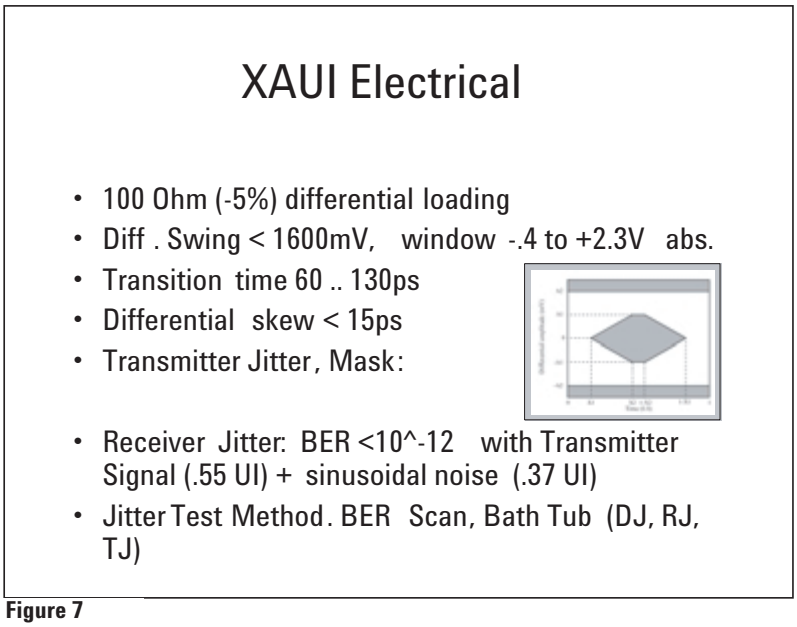

Figure 7

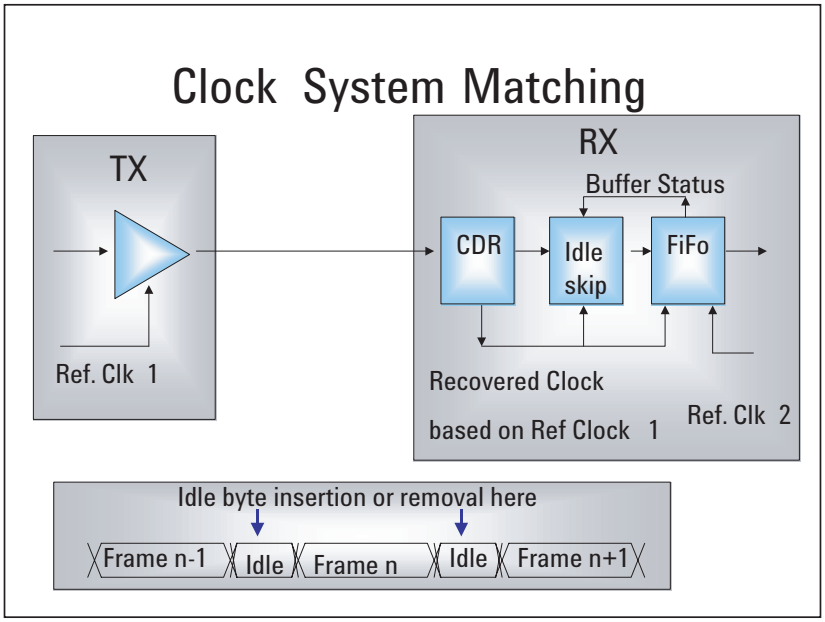

Figure 8

Discarding and insertion of bytes is allowed in the idle phases, but not within a valid frame.

The circuit needed to accomplish such a re-timing is indicated in the RX block: firstly, a clock data recovery (CDR) from the incoming data signal is needed. Then there is the circuit which does the skip/insertion based on the status of an elastic buffer written with the incoming clock, read with the local reference clock.

The picture is so far simplified that there is no frame recognition, this basic circuit would skip/insert anywhere.

10GbE has implemented an idle sequence consisting of 3 different characters. The idle insert/skip is only allowed after one specific character occured. This ensures the frames will never be touched.

An Ethernet frame has a maximum length of 1518 bytes. Assuming the TX and RX have worst case clock tolerance against each other, there is a difference of roughly 1.5 UI (unit interval = bit cycles) over the length of one frame. Therefore a skip byte will not occur after each frame.

As mentioned already, Ethernet principle is to put the data into blocks, called frames. Basically, the way this works is that user data (e.g. a picture) runs through the functions of the 7 OSI layers, and is built into this structure. Each layer adds its information like a header to a block of data. The next layer below treats the block from above as payload again and then adds its own info as a new header.

Finally the frame is ready in the Data Link Layer. Ethernet has several slightly different frame types. The most commonly used is the 802.3 “Raw“ Frame. It consists of Preamble, Start Destination Address, Source Address Length indicator, Payload and finally a Check Sum. All parts have a fixed length in bytes, except the payload.

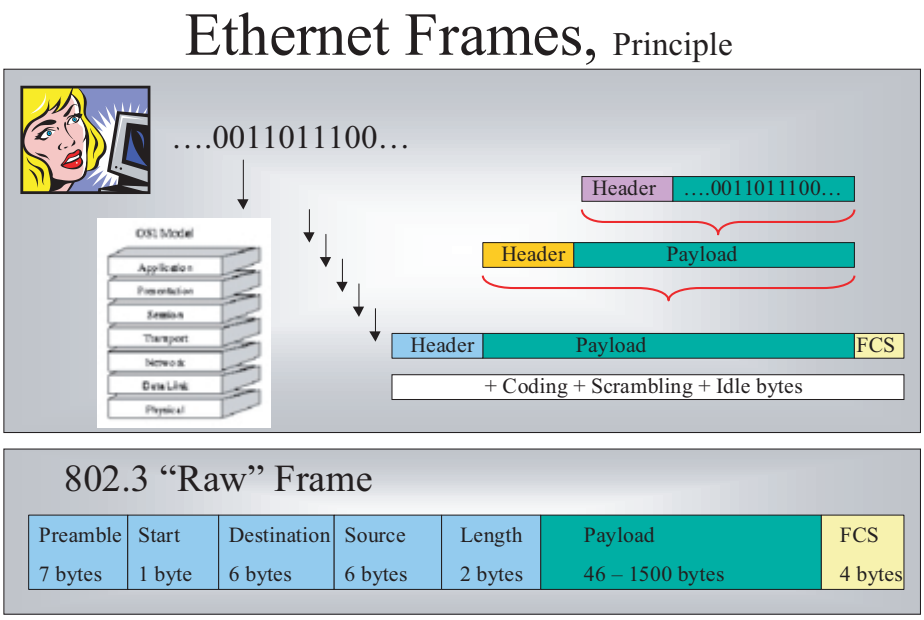

Figure 9

XENPAK and XAUI Details

This is the block diagram of a the XENPAK 10GBASE-LR type. On the left is the XAUI interface, on the right is the fiber media.

The upper part is the TX Path taking data from the XAUI and transmitting the optical signal, the lower part is the RX Path receiving the optical signal and transferring the data to XAUI.

The sub layers inside the XENPAK are: XGXS Extender Sub Layer, PCS Physical Coding, PMA & PMA Physical Media Attachment & Media Dependent Sub Layer

Further elements are the Reference Clock Generation with the various rates needed internally. Figure 11 takes a closer look at the XGXS sub layer.

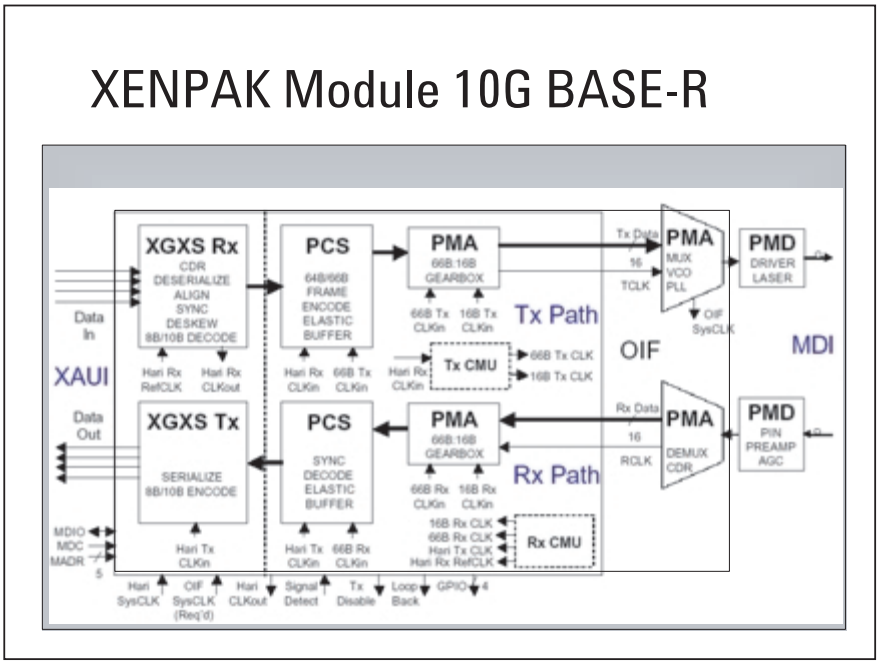

Figure 10

XGXS Functionality

The XGXS Extender sub layer converts the data between XGMII (2x36 bit for TX and RX + 2x clock) and XAUI. The XGMII interface is physically not available, hidden inside of large scale ASICs as it is not suited to be routed over a long distance. However, according to 802.3ae it is a reference for functionality.

The XGXS exists on both sides of the XAUI interface. It ensures a robust data transfer over the XAUI link. In order to do this, the XGXS does the functions according to the table given in Figure 11. What can be a little confusing is that the table refers to the XGXS inside the XENPAK, where the XGXS RX sits in the overall TX path, as we are talking about data flowing from top to bottom. And the XGXS TX sits in the RX path with data propagating from bottom to top. XGXS functionality is now closely examined.

Figure 12 deals with the Idle Mapping from the XGMII interface to the XAUI and vice versa.
First look at the Ethernet frame again. There is some reference (S, dp,d,df) for the different parts in the frame which is now represented on byte level on the XGMII and XAUI interface.

On the XGMII we see the data grouped in bytes + control bit which get serialized into a 10 bit word on a XAUI Lane. On the XGMII a cell starts with the “S‘ character always to be in Lane 0. This is actually the first character of the frame‘s preamble modified into the “S‘ character. All the other frame bytes follow including the 4 check sum bytes. Finally there is a “T” character, which is not defined in the frame format, but is added by the Physical Link. Around the frame are Idles (I). On the XAUI there is no logical change made to the frame, because 8b/10b coding does not change their meaning. The idle coding is different in that the pure I‘s change to a sequence of three specificl characters called “A”, “K” and “R”. The “A” character will randomly repeat every 16 to 31 columns, the others fill in alternately.

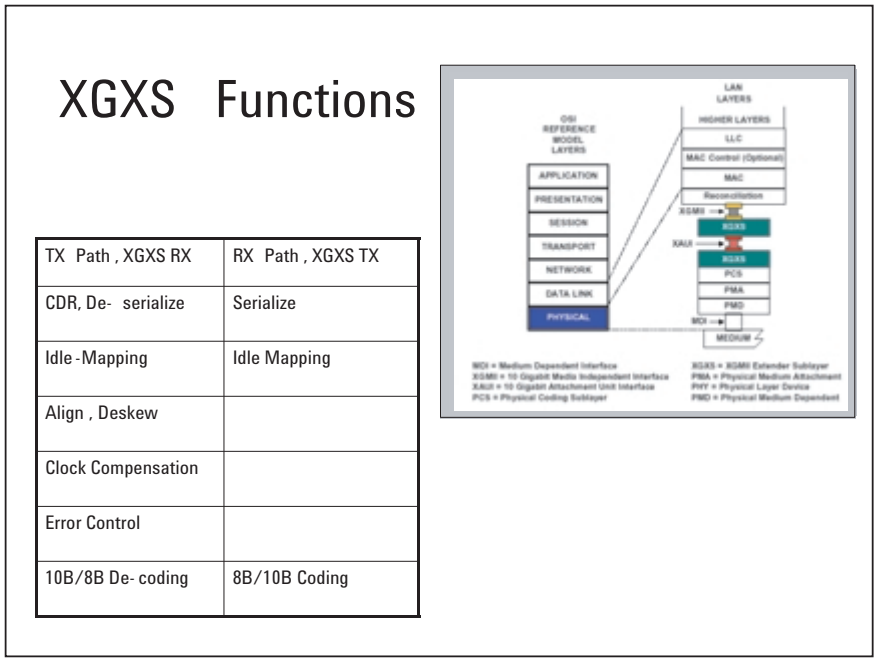

Figure 11

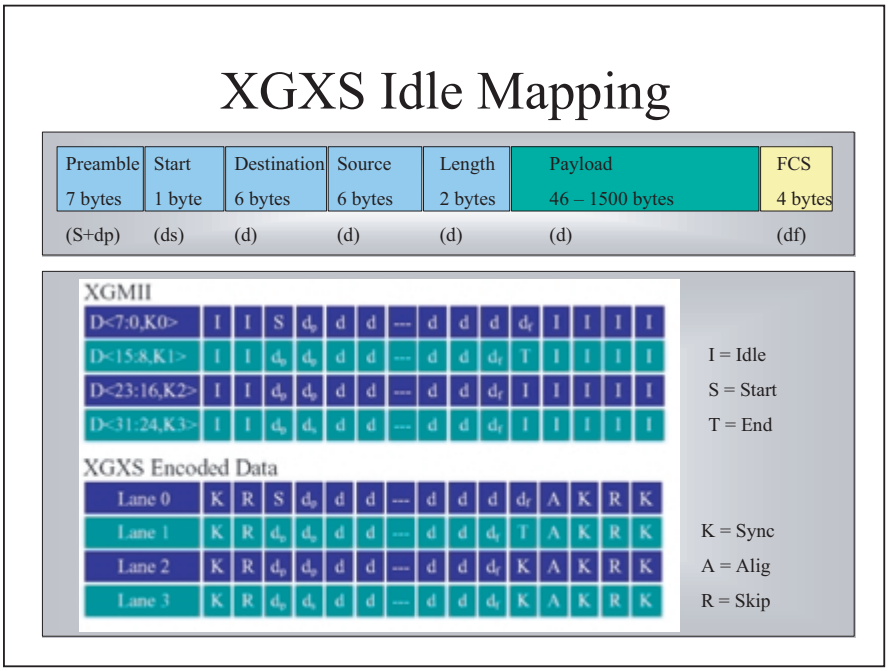

Figure 12

Figure 13 shows the list of control codes and their meaning, which the XGXS sub layer uses. These control characters are special 10 bit words defined on top of the 256 data characters.

The 802.3ae Standard allows a skew of up to 41 UI between the 4 XAUI lanes. Be aware this is not the skew within a differential pair, the differential skew has to be closely controlled in the layout. This is the skew of one differential pair against another, allowing different propagation delay for the 4 XAUI lanes. This should make the life of a PC designer simpler and save cost as propagation delay matching for a bus can consume a lot of layout space. The skew budget also includes tolerances from the functional behavior: there are serializers and deserializers. These parts do not start up every time with same phase relation between high speed and low speed size. The Deskew procedure takes care of this.

The XAUI Deskew is done with help of the “A” character. The XGXS sub layer will recognize them and align the 4 XAUI lanes against each other. After the alignment the data from all 4 lanes can be converted to a single clock again. To make this alignment robust, the “A”s occur not periodically but pseudo randomly.
Figure 15 shows how the skip/insert works. This is the process to align the data for slightly different clock speeds within two subsystems with individual reference clocks. Remember a basic tolerance including drift of +- 100ppm is allowed.
The “R” character is used as skip byte. The slightly faster system will insert it after an “A” character. This simple rule ensures it will never placed inside a frame (in between “S” and “T‘). So the insertion is guaranteed to be done within the AKR... Idle sequence only. Figure 15 is slightly incorrect: the insertion of the ‚R‘ character is done as the bit period of the lower system is slightly shorter. So with the new “R” included the time should be the same again. On figure 15 the last K of upper slower is missing on the lower faster system.

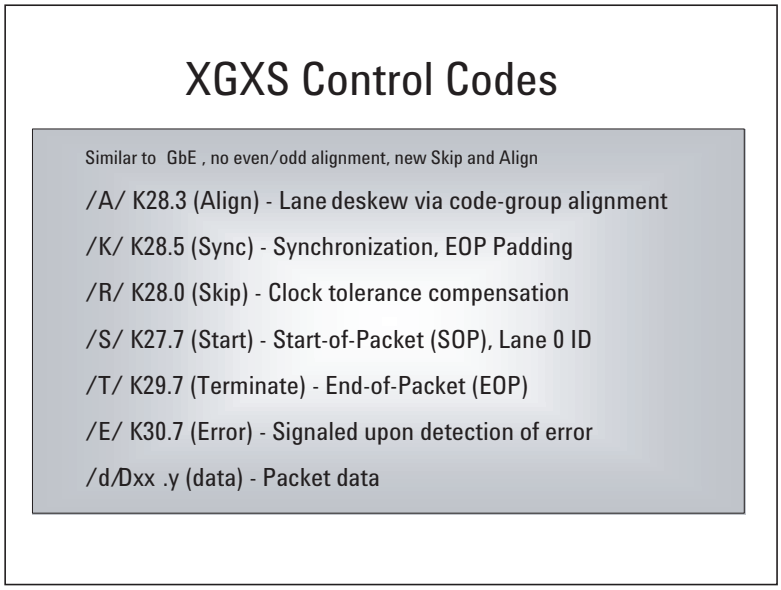

Figure 13

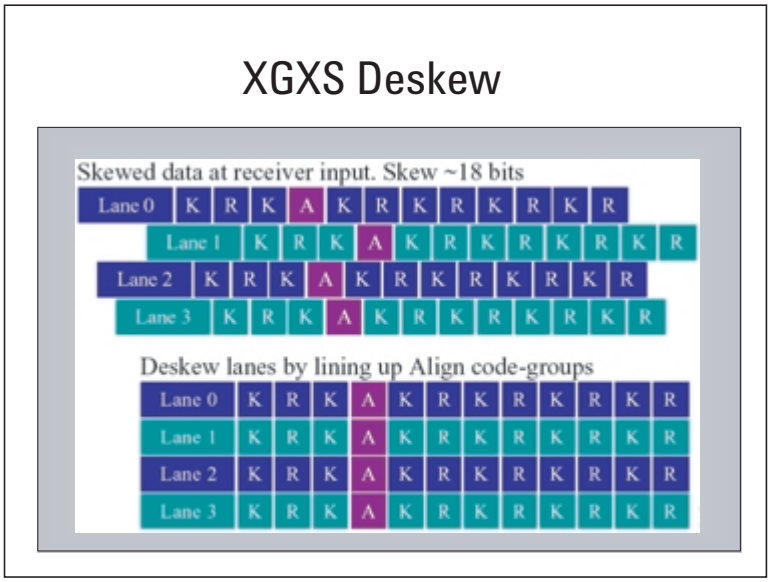

Figure 14

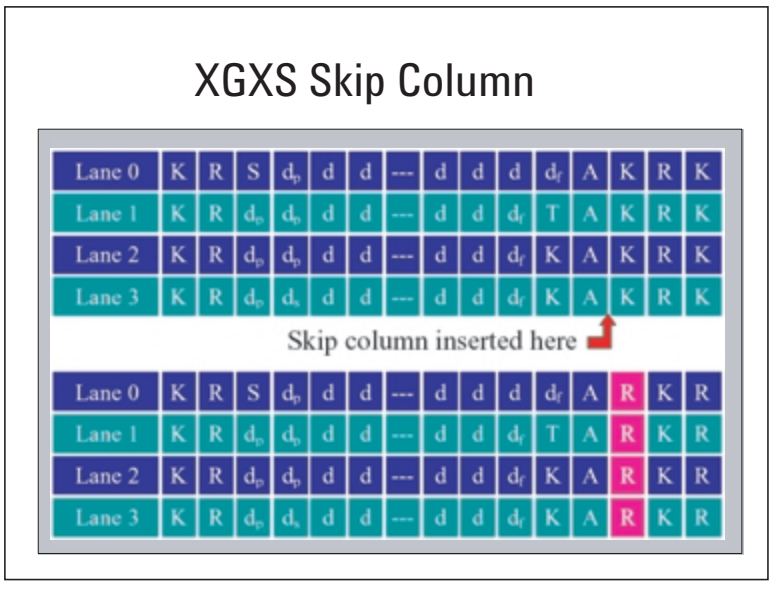

Figure 15

Figure 16 shows the other sub layers: PCS, PMA & PMD

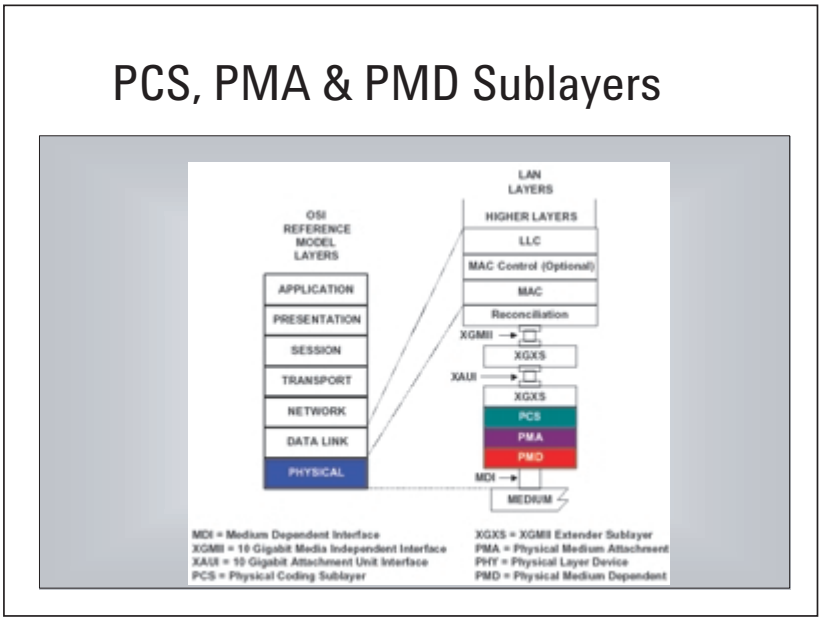

Figure 16

Figure 17 examines the other sub layers more closely:
PCS is the Physical Coding sub layer. This coding is done by scrambling. PMA is the Physical Media Attachment sub layer. This is responsible for the 64b/66b coding. Then the 66 bit words are re-mapped into 16 bit blocks with help of the gearbox as shown in figure 17. Finally, the 16 bit words are serialized and fed to the Laser for transmission. This is performed in the PMD Physical Media Dependent sub layer.

Look at the Bit Ordering diagram in figure 17 again: there are two bits added for the 64b/66b coding. These bits will be defined on the content of the unscrambled 64 bit word. And these two bits bypass the scrambler. Figure 18 shows more on the scrambling.

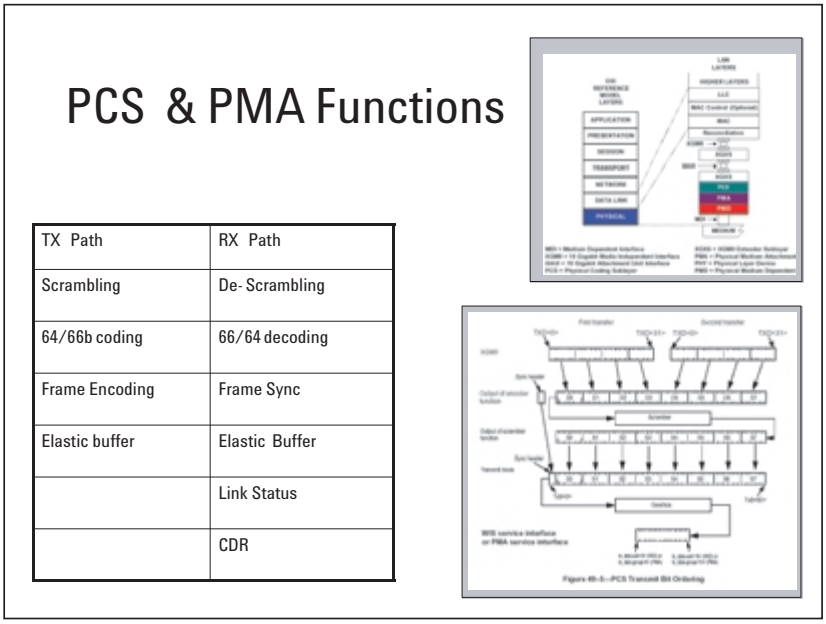

Figure 17

Why scrambling is done

The function of the scrambler is to tune the data for disparity = 0 on the link and lower EMI.

The scrambler uses a long polyinomial (58 stages). This converts the data into a wide band frequency spectrum which is good for low emission. This achieves low energy radiation at many frequencies against high peaks at few spectral lines.

The scrambler is built as a shift register with 58 stages. There is one feedback taken from stage 38. On the transmit side the scrambler may be started with a preload of a specific data content. This is important later on when we talk about testing. This preload is also called seed. With a known seed and a known input pattern the scrambler output is deterministic, which means the output of the scrambler can be calculated.

On the receive side the de-scrambler synchronizes automatically from the incoming data.

Once pretty obvious data - meaning a sequence of data with known a pattern and easily recognizeable -is sent through a scrambler, it is no longer meaningful to the human eye. Even a repetitive pattern will no longer be periodic as the scrambling adds the total history to the current data stream. So any periodics or specifics inside the patterns cannot be seen inside a scrambled stream. It needs to be de-scrambled again.

Another notable characteristic when dealing with scrambled and unscrambled data is as follows: assuming the transmission of scrambled data and a single bit error occurs on the link, then this single bit error when de-scrambling will obtain a bit sequence with several bits different compared with the original sequence. So for BER testing it is not the best idea to do this when a scrabler/de-scrambler is in place, because you may end up with a BER figure way off expectations.

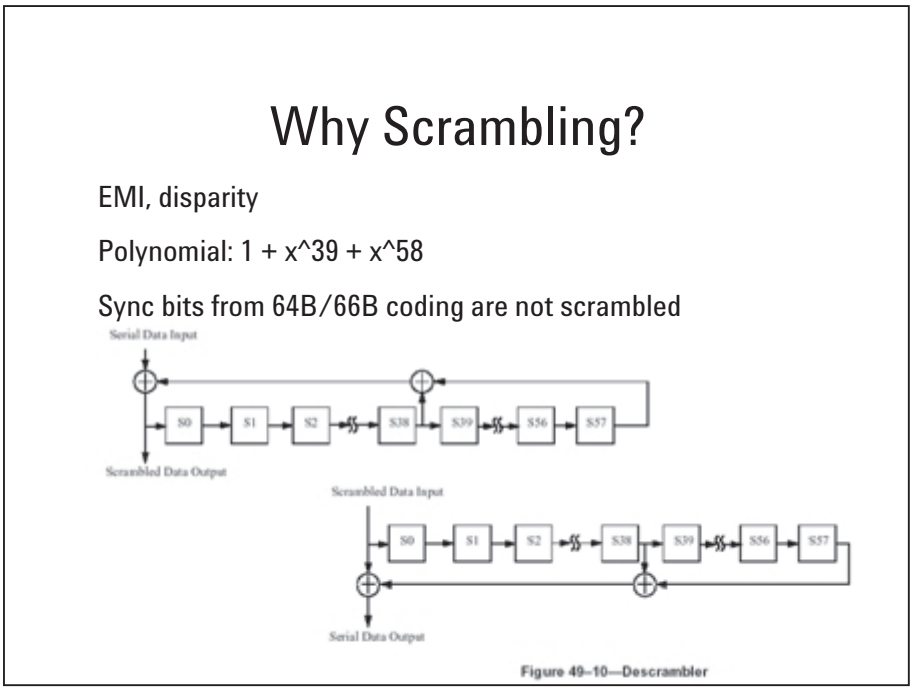

Figure 18

Figure 19 is for the 64b/66b coding overview. The coding itself is a complex mapping of 64 bit blocks into new 64 bit words including the addition of two control bits for the final 66 bit word.

The first step of the process is to combine 8 bytes into one 64 bit word. Basically this word can contain pure data, pure control (idle or "S"...) or a mixture of data and idle. If it contains pure data, the two control bits are assigned "01", otherwise they are assigned "10". The values "11" or "00"for the control bits are not allowed.

Second step: a 64 bit word with pure data will not be touched, but a 64 bit word with pure control will get a new first byte with value "1E" and a compressed bit combination for the control characters. The 64 bit words containing a mix of data and control will get a new fixed first byte depending on how many data bytes are in, while the room for the new first byte is taken by compressing the original control characters.

The "01" / "10" bit insertion which does not run over the scrambler is used for detecting the 66 bit boundaries at the receiving side. With detecting these boundaries, the decoding can be achieved again. These two bits are basically the total overhead occuring for transmission. The penalty for overhead on the physical layer is that the link speed needs to go up. Link speed needs laser performance which drives the cost up. So in terms of overhead, the 64b/66b coding is much more efficient than the 8b/10b coding would be. Link speed needs to be just 3% faster than data rate is. So the idea is to squeeze the 10.3125 Gb/s out of common 10G laser technology.

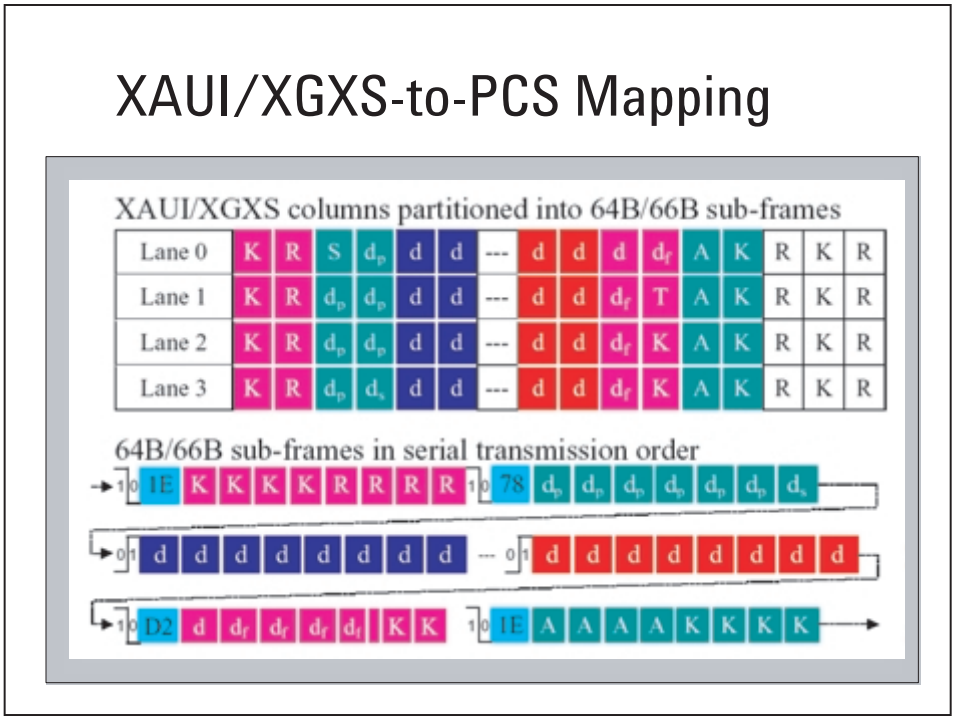

Figure 19

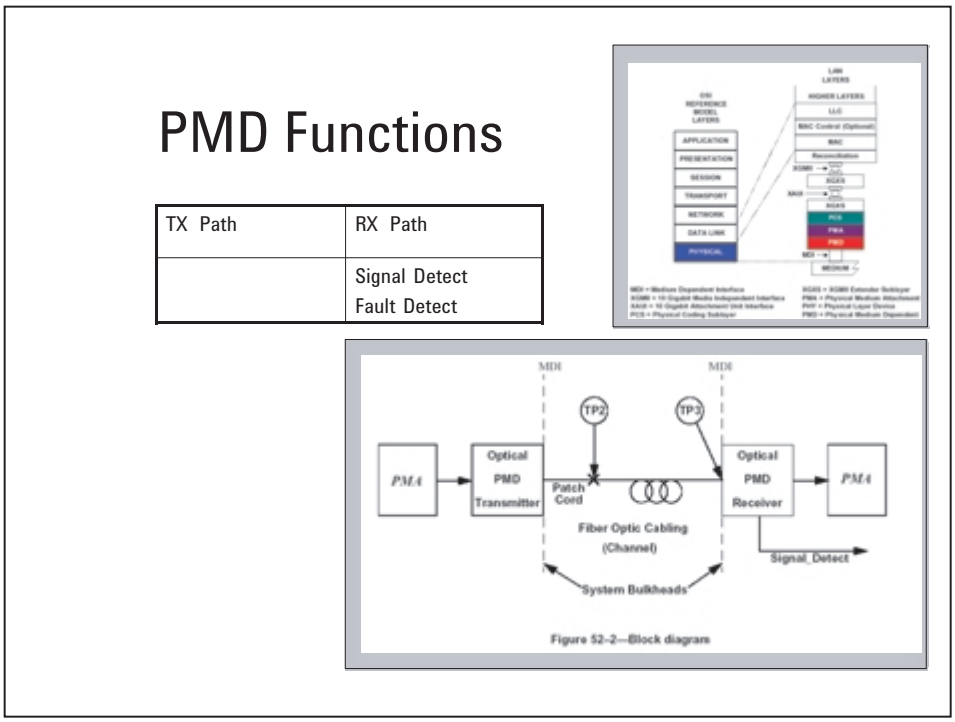

Figure 20

The PMD sublayer functionality is not complicated. There is just a signal

Physical Media Dependent (PMD) Sublayer

and fault detect for the media. But the PMD specifies a lot for E to O, O to E conversion fibers and connector types to be used. Electro-optical parameters, test methodology and scenarios for setup and perform measurements are defined.

The PMD parameters can basically be grouped into three cathegories: optical power and OMA (optical modulation amplitude), which is just another way of taking former extinction ratio measurements.

Transmitter Eye Mask is specified as decagon (10 corner points), and there is a specific TPD (transmitter and dispersion penalty) measurement.

For the receiver there is a specific Stressed Receiver Conformance Test defined, which works with FM and AM modulated input signal to achieve a well defined eye closure.

IEEE802.3ae and Testing

Jitter issues in particular fill a couple of pages within the 802.3ae standard. There have been significant changes in the documented methodology recently. The TDP and the stressed Receiver method have been replacing the traditional BERT scan and Scope scan methods. These new methods are suited for manufacturing. Unfortunately “golden” devices are necessary in the test setups. Test equipment manufacturers need some time to prepare and provide this.

This method is not suitable for R&D as the characterization will still need the bath tub and eye opening measurements.

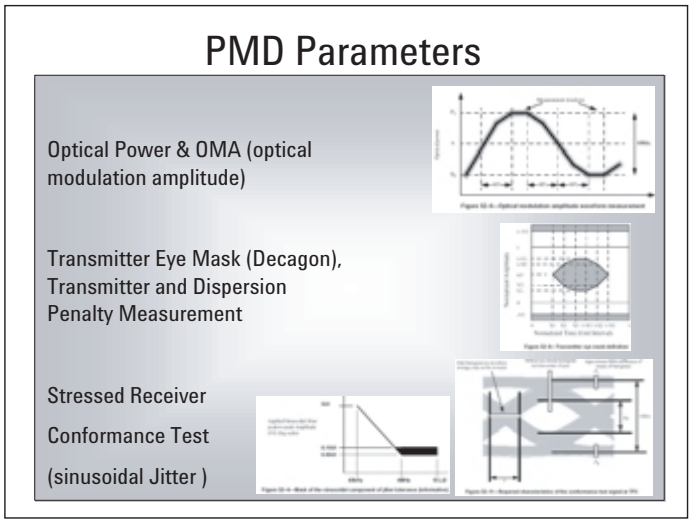

Figure 21

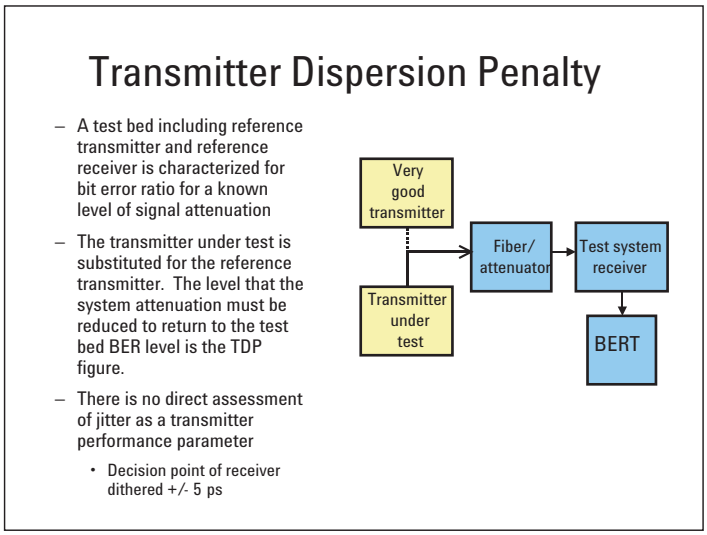

Figure 22

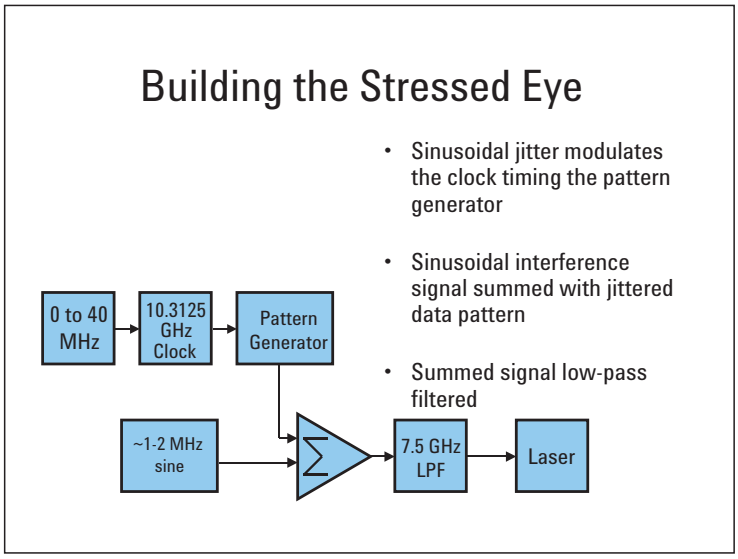

Figure 23

Beside specific methodology for jitter testing, the 802.3ae standard specifies Loop-Back and optional Test Pattern Generation and Checking.

With the help of Loopback and specific Test pattern (e.g High-Low-Mixed Frequeny Pattern, CRPAT, CJPAT) the XAUI side can be tested.

The 10G side can provide a built in pattern generator with 2^{31}-1 PRBS polynomial on the TX side. The RX side includes a similar error detector. Unfortunately this is declared as optional only.

Specific vendor implementation offer much more test support:
- Loop-back within XGXS
- Loop-back at the 10G electrical
- PRBS generator and Error detec tor on each XAUI Lane

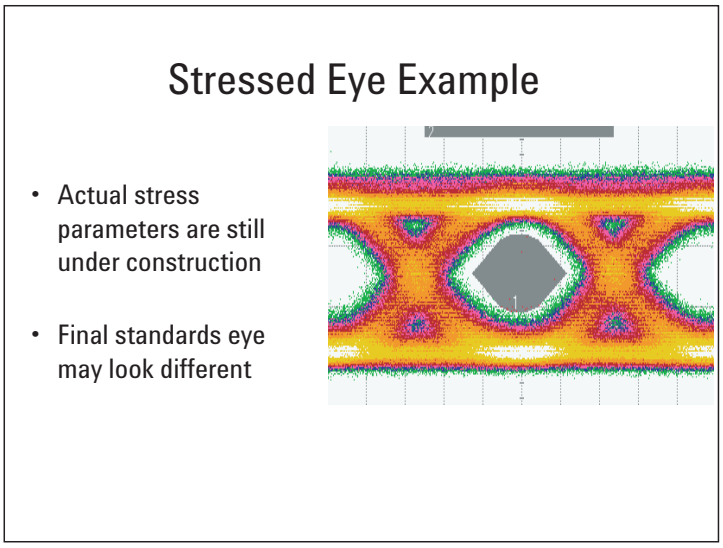

Figure 24

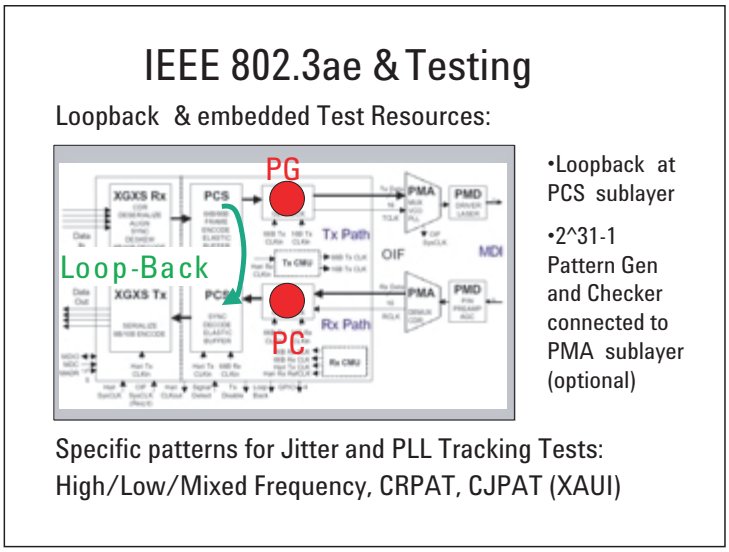

Figure 25

From the point of view of a tester manufacturer, the definition of clockless interfaces is not a good idea. Test equipment always needs a clock for reference. Clocks can be re-generated with help of CDRs, but there is always the question of performance as there might be additional jitter and there might be bandwidth and tracking limitations.

It is therefore a good decision if a designer puts a reference clock signal on at least the manufacturer specific pins. This is important help for the test engineer.

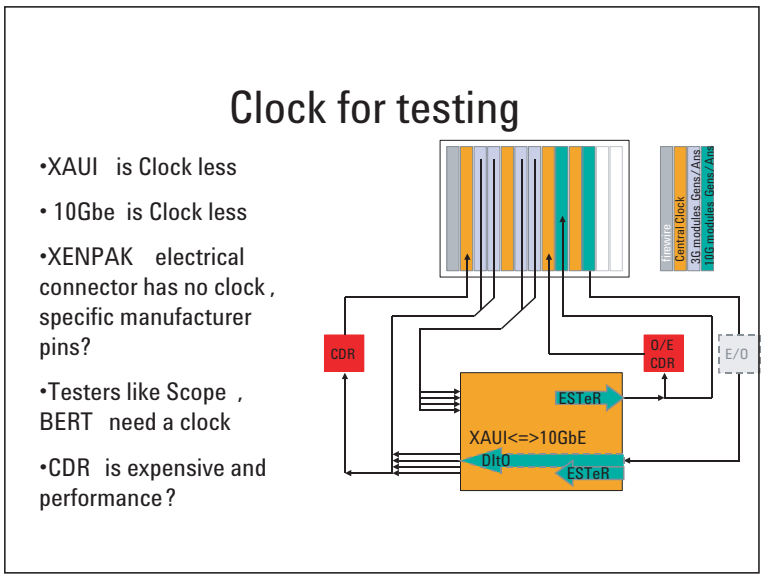

Figure 26

Test System Considerations

The first important issue is that a test system should provide all necessary channels to stimulate and analyze all inputs and outputs. A modular system is ideal, because you can install the appropriate number of channels with just the performance you need. So a pin on the XAUI side does not need same performance as the serial optical channel. Therefore a modular system offering just the right channels keeps overall costs to a minimum.

Figure 27 shows just such an approach. The system shown is a purely electrical system with E/O and O/E converters. The test system channels are 1x 10.8Gb/s generator and analyzer, and 4x 3.35Gb/s generator and analyzers. These generator and analyzers can run the 10.3125 GBs serial speed as well as the 3.125 Gb/s required on the XAUI side.

XAUI inputs and outputs are differential. With a test system providing differential inputs and outputs, it is possible to connect exactly the way the XAUI will work in real life. This avoids any problems and uncertainty with balance or unconnected inputs / outputs. A test system with parametric channels in timing and levels is able to provide all necessary signal conditions with min/max swing and specific deskew conditions.

The Reference Clock inside the XENPAK is 156.25 MHz +- 100ppm. The XAUI rate is 3.125 Gb/s and the serial rate is 10.3125 Gb/s with the same accuracy.

There are frequency ratios of:
- 20 for XAUI to ref clock
- 66 for serial to ref clock
- 33/10 for serial t o XAUI

A test system with flexible m/n ratio in the clock input allows these ratios to be adapted.

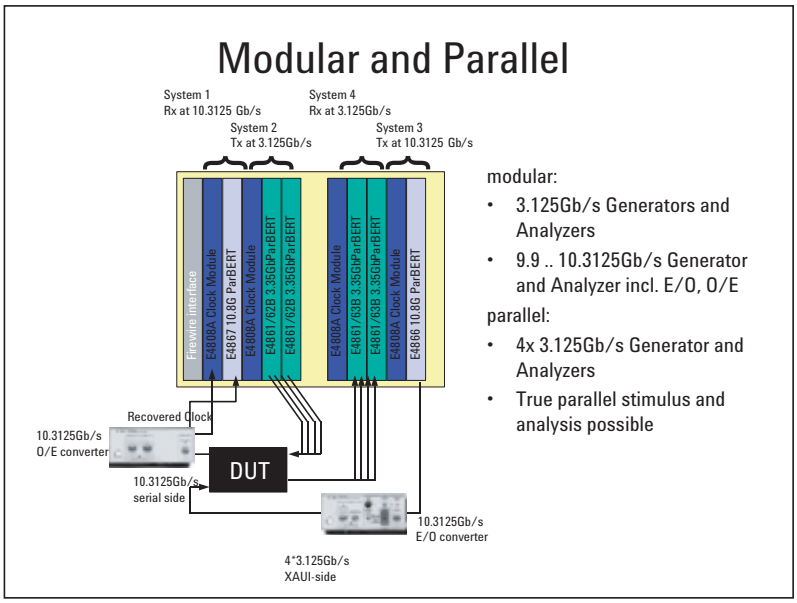

Figure 27

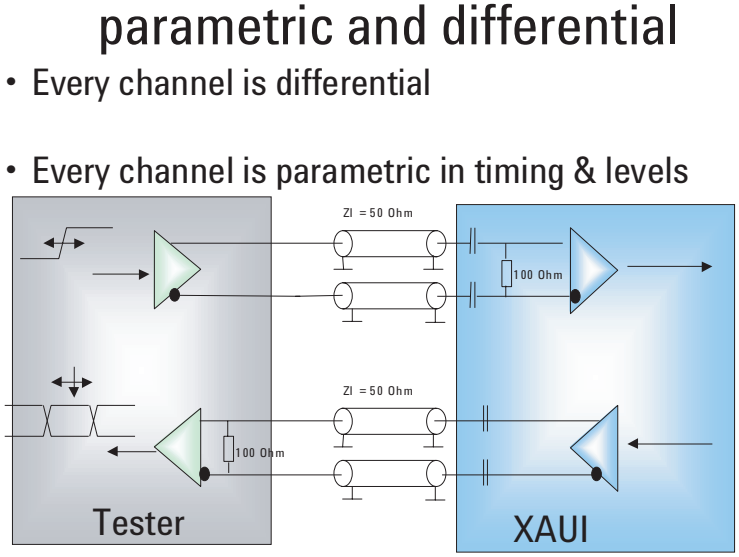

Figure 28

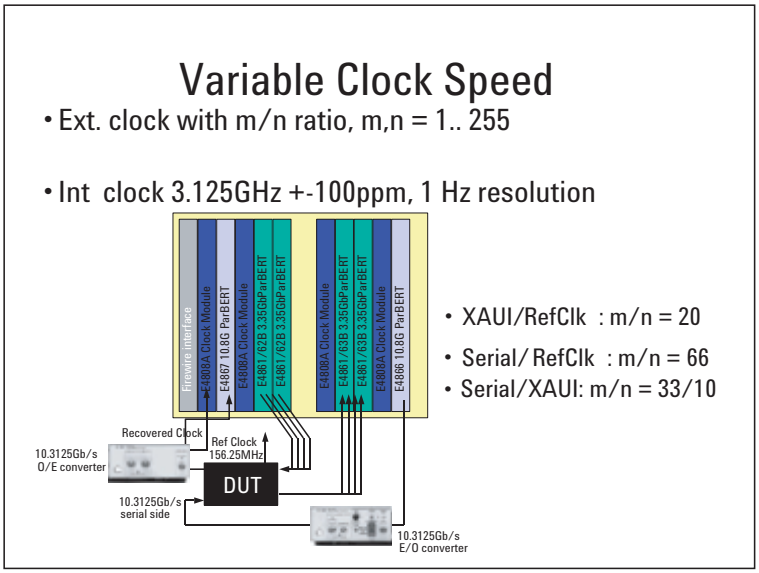

Figure 29

The 802.3ae standard deals with jitter as UI versus frequency, where UI = unit interval which is the equivalent for data cycle. Frequency is the modulation frequency of the data transition, but this is NOT the data rate.

At low modulation frequencies the jitter – or better called drift and wander – can be multiple UIs.

A PLL will follow this drift as it is below the cut-off frequency within its feedback loop. So this can be compensated. At high modulation frequency there is only a fraction of 1UI jitter allowed. Here there is no mechanism to compensate. The modulation is too fast for a PLL to compensate. It will simply ignore this jitter. But the jitter is still there reducing the eye opening. Now it is the task of the input buffer to identify the proper bit within the remaining stable part of the eye. It is a matter of bandwidth of the input circuit to detect the remaining pulse width. This way of describing the jitter allows a well defined stress signal to be created. This is fed to an input and it is easy to check if input circuitry and CDR will work to a proper bit error level.
So a test system provides a modulated clock which goes through and generates a data pattern stream with this modulation on the data transitions.
Another simpler setup for the high frequency modulation can be achieved with a test system capability in figure 31.

The 3.35 Gb/s Generator has a Control Input for modulating the delay with help of an external signal. This modulation can be used to emulate jitter. Figure 30 shows this modulation for different types of control voltage. The modulation can be used to test a DUT for jitter tolerance.
The modulation with a square wave generates two peaks in the histogram. This is emulating deterministic jitter.
For emulating true gaussian distributed jitter, a noise source would be needed to be connected to the modulation input. Such a modulation input can provide quite a high bandwidth, here 200MHz is posssible.

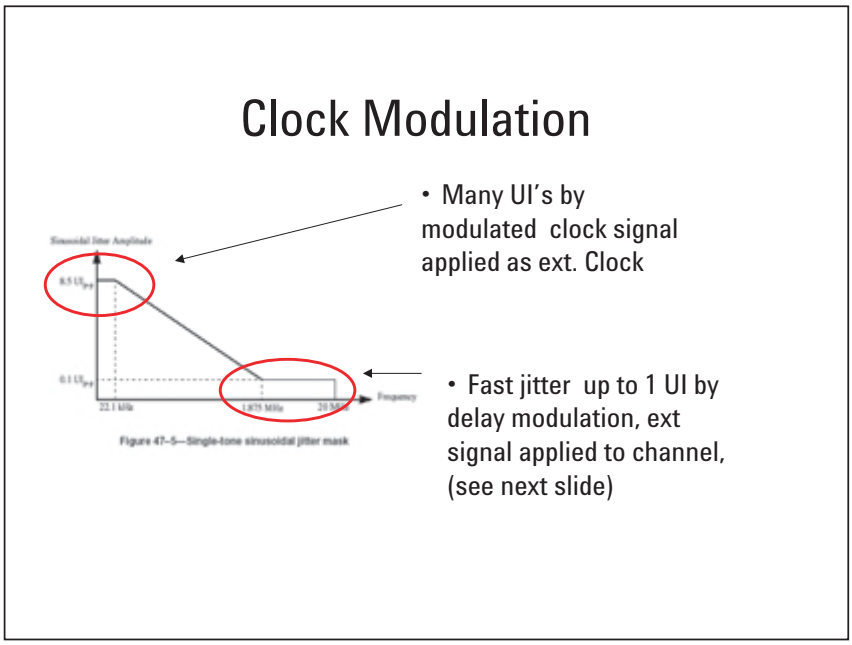

Figure 30

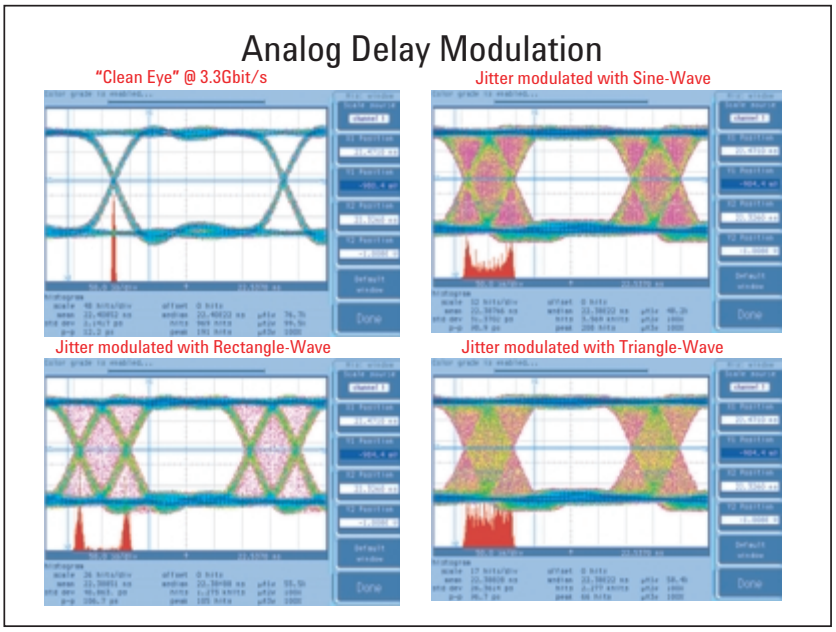

Figure 31

The 802.3ae standard specifies specific test pattern for tests at XAUI and serial side. With help of a simple software tool this pattern can be generated for easy use on the test system. Predefined patterns for the serial and XAUI side serial: square wave & PRBS 2^{31}-1

XAUI: High Frequency, Low Frequency, Mixed Frequency, CRPAT, CJPAT (incl 8b/10b coding)

Further information on this subject can be found in our Product Note “10GbE Testing with 81250 ParBERT. The 10GbE Ethernet Tool” Publication #5988-8278EN.

Figure 33 shows the so called “Sequence Editor”. Here we see the two XAUI ports defined in the Connection Editor and all the data handling is within the columns below the ports (green). The individual bits are located within the segments (blue boxes) defined by name. These segments in this example have been created with help of the editor shown in figure 32. These segments can be edited further, for example for inserting an error, which is shown in Figure 34.

In this example we see a setup for a loop test on the XAUI ports. There are three blocks (grey boxes):
The first for intialization: the generators fire a pattern of A, K & R characters for initialization, at this point in time the test system analzer is paused. This block is done once and the test flow moves to the next lower block.
The second block is for aligning the analyzers. The generators fire the CJPAT segment in this case while the analyzers will align bit wise.
The third block is infinitely repeated for BER measurement.

This is the example for a segment editor, which allows view and also modify individual bits.
From right to left the 4 XAUI Lanes are represented, starting from top to bottom the bits are shown. The view mode can be changed from binary to other formats, e.g. hex. The editor represents any kind of data, such as stimulus, expected or captured. The type is defined when a segment is associated with the sequence editor into a generator or into an analyzer, as shown in figure 33.

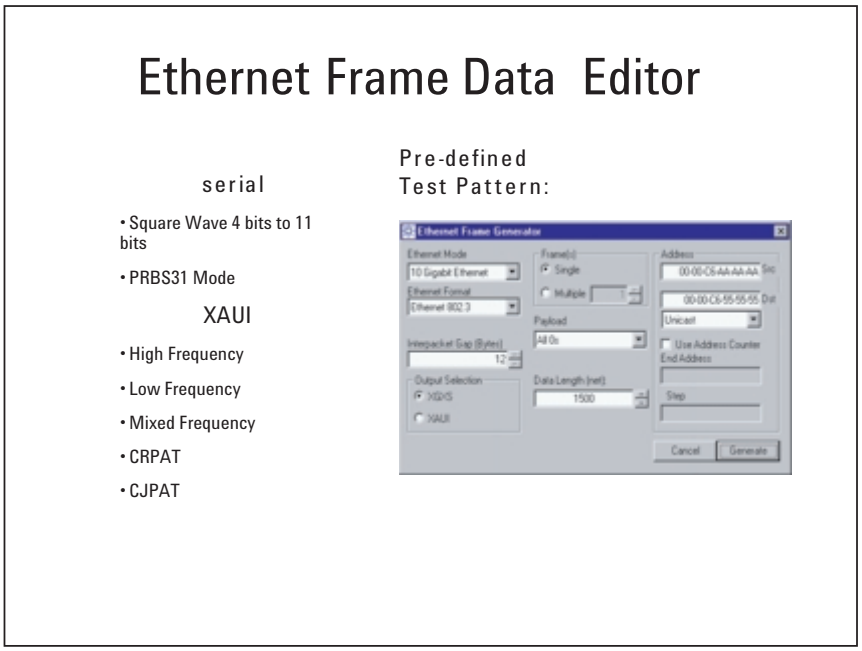

Figure 32

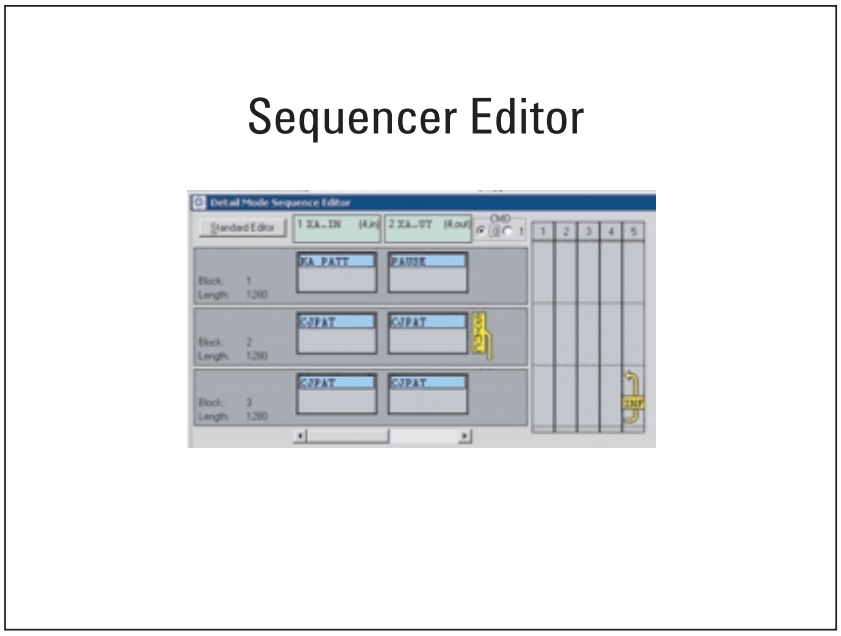

Figure 33

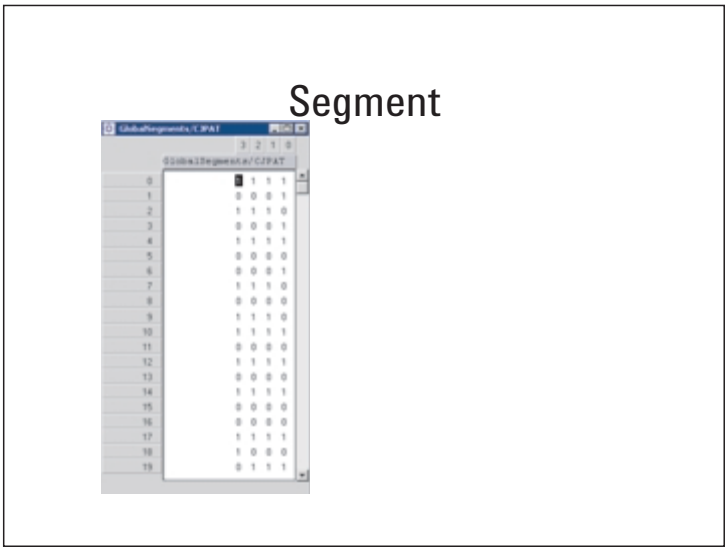

Figure 34

This is the BER measurement showing the BER figure for a XAUI Interface. On the left are the 4 XAUI Lanes. The BER is given for each XAUI Lane individually and in the bottom line there is the summary for all 4 lanes together. An error is defined as a mismatch of the incoming bit versus expected.

BER is defined as the number of errors divided by number of bits processed.

The BER test is a real time test. The incoming bits are compared with expected “on the fly”, which means from cycle to cycle. The BER measurement can be performed with PRBS or user defined patterns, e.g. the patterns obtained from the Ethernet Editor.
The analyzer can be adjusted for proper bit match between incoming data and expected data:
- either with the sampling point delay (which is a proper method if the delay between stimulating and analysis is a constant propagation delay.)
- or with help of the synchronization block in the sequence editor. (For the XAUI this is the proper method, as the propagation delay is not predictable.)

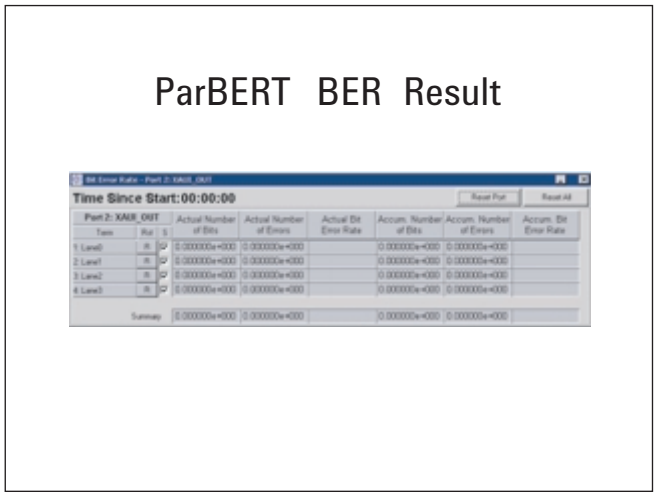

Figure 35

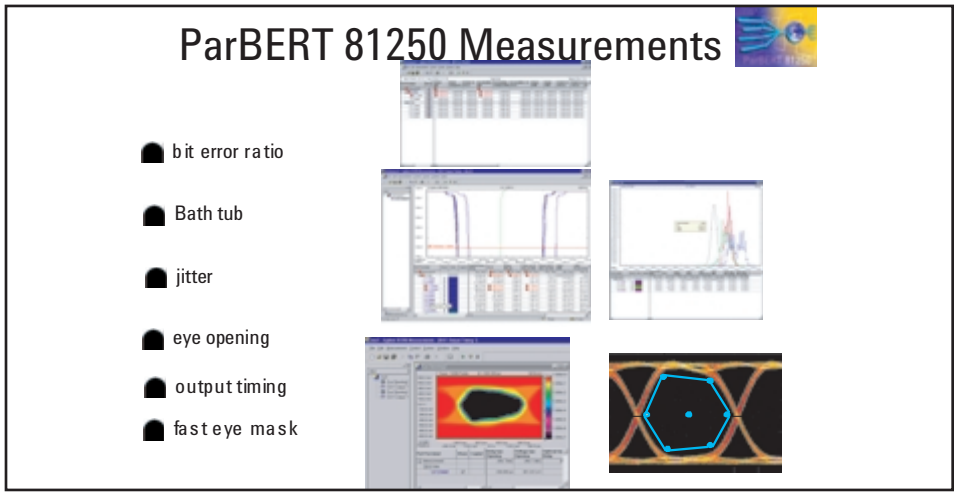

Figure 36

High Level Measurement Software

This visualizes the result of parameter sweeping. A common measurement is the Bath Tub, visualizing the BER figure versus time. A bath tub applied to multiple DUT outputs can measure skew and phase margins at the same time for all outputs.
Another measurement is the Eye Opening measurement, which shows voltage versus time. The BER figure as the color coding as third dimension. So this is used to extract the so called “ISOBERs”, lines with same BER figure.
The eye opening measurement with the ISOBERs is the tool in characterization. Here the points for a given BER can be found over any worst case operating conditions.
For production there is the so called “Fast Eye Mask” measurement. At first glance it looks similar to the Eye Mask. But the diagram given is a little misleading. The Fast Eye Mask is simply a table where you specify how many points inside the eye should be measured (up to 32 are possible) and for each point an offset in time and voltage from the ideal sampling point in the middle is specified. The offset can be absolute or given as percentage. Finally you may specify a limit for the BER figure at each individual point. To define these points, you may take the ISOBERs found under worst case operating conditions or just take the corner point given from the standard eye templates.

The routine will then work the way to set time and threshold, get BER figure and compare against given limit. It will return PASS or FAIL. As this routine works with no overhead in drawing a graph, it is very fast, just 1-2 seconds depending on how many points are specified (2-32). As in a parallel hardware architecture, every channel does the measurement at the same run-time. It does not matter how many outputs are measured, the measurement time will be always the same.

Functional and Parametric Testing

Funtional testing means that data put in to the XAUI side will be correctly transported to the serial side and vice versa. Here this is called DITO (Direct Input To Output). Jitter and eye openings are examples of parametric testing. PG & PC stand for the built-in test pattern generation and checking capability. “Ester” means embedded test resources.
The table in figure 37 tells you what tests can be achieved for the scenario: DITO, Ester and Loopback.

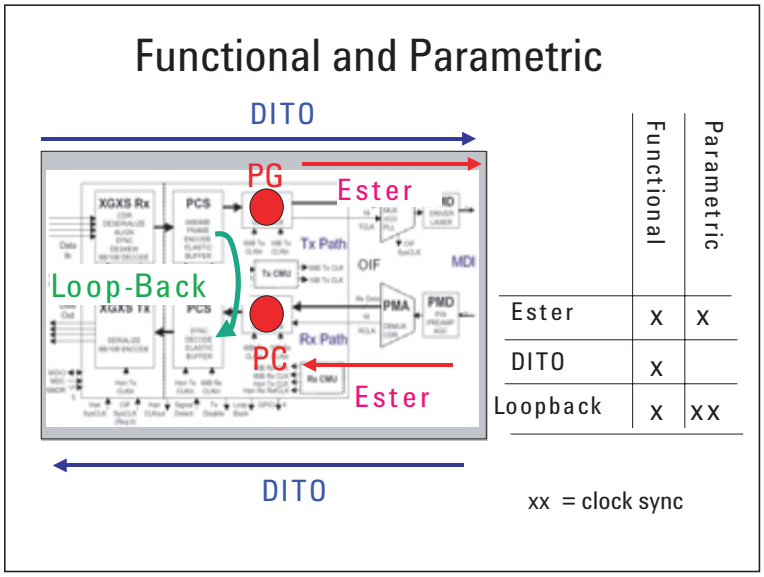

Figure 37

Some first results

Figure 38 shows a setup of the ParBERT 81250 together with E/O and O/E converters connected to a XENPAK evaluation board loaded with a XENPAK. There are also two power supplies and a PC running the control software for the XENPAK as well as the ParBERT 81250 software.

This setup used 2 clock modules. One for the 10 Gb/s generator and Analyzer, the other for all the 3.35 Gb/s channels. This first setup showed a slight inconvenience in that the speed of generators and analyzers could not be varied against each other. So as a consequence the recommendation for final test configuration would be to use 4 clock modules to separate all generators and analyzers. This will allow the test to be run with the +- 100 ppm frequency offset.

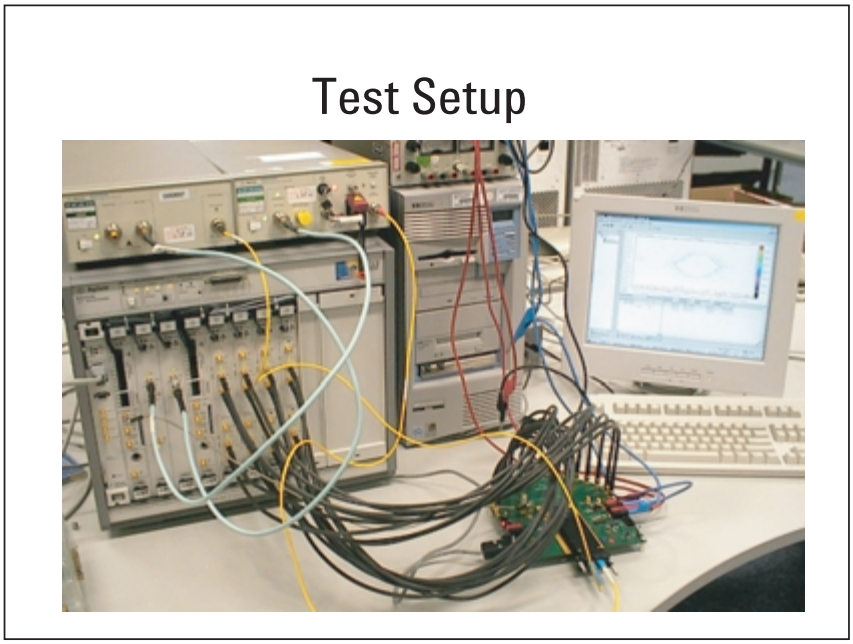

Figure 38

Figure 39 shows the “connection editor” for a ParBERT with 4 independent clock groups.
Here we see a system with a 10.8G generator, a 10.8G analyzer, 4x 3.3G generators and 4x 3.3G analyzers. The 3.3G channels are grouped into so called ports to handle the XAUI lanes. Each can run on its own frequency.

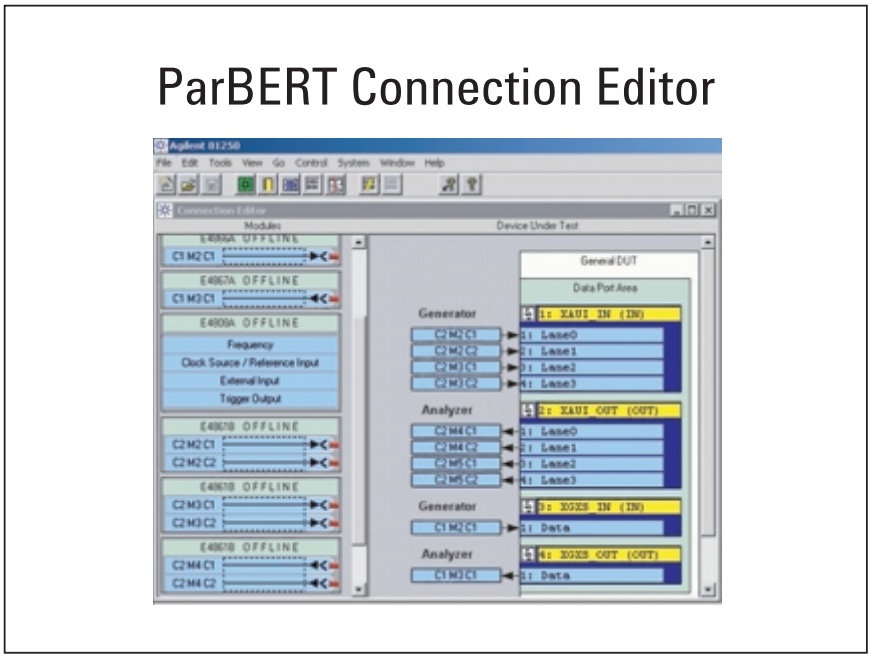

Figure 39

This is a first result of an eye opening at the XAUI Lane0. This is measured with the setup shown in figures 38 and 39.

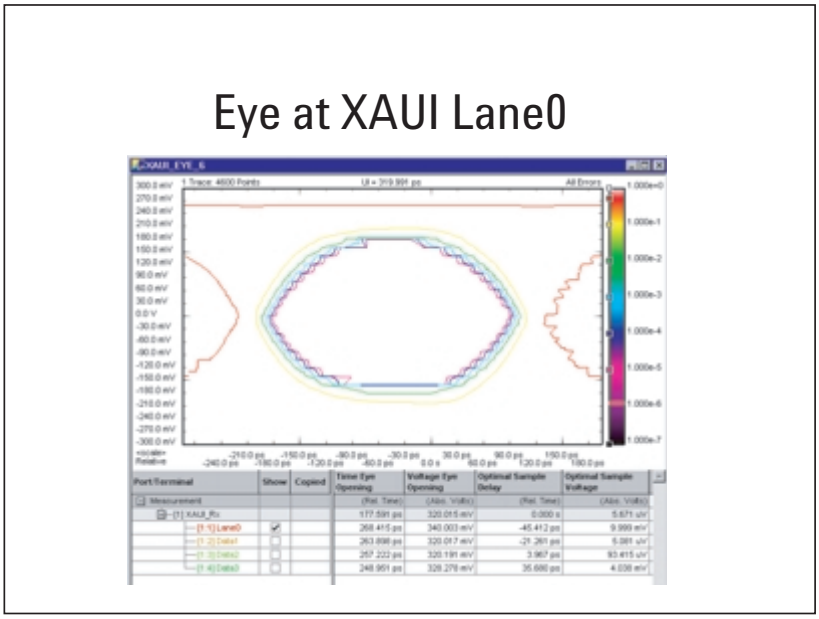

Figure 40

These are abbreviations used within this product note and common with the 802.3ae standard.

10 GbE Terminology

- 10GEA: **10 Gigabit Ethernet Alliance**
- CSMA/CD: **Carrier-Sensing Multiple-Access/Collision Detection**
- CWDM: **Coarse Wave Division Multiplexing**
- DWDM: **Dense Wave Division Multiplexing**
- EOS: **Ethernet Over SONET**
- MMF: **Multi Mode Fiber**
- PCS: **Physical Encoding Sublayer**
- PICS: **Protocol Implementation Conformance Statement**
- PHY: **Physical Layer**
- PMA: **Physical Media Attachment**
- PMD: **Physical Media Dependent**
- XAUI: **"Zowie" Extended Ethernet Attachment Unit Interface (extends XGMII)**
- XSBI: **10G 16 bit Interface**
- XENPAK: **XAUI Module Spec. (started by Agere & Agilent)**
- XGMII: **10Gb Media Independent Interface**
- XGXS: **XAUI Extender Sublayer**
- RPR: **Resilient Packet Ring**
- SMF: **Single Mode Fiber**
- WIS: **WAN Interface Sublayer**
- WWDM: **Wide Wave Division Multiplexing**

Related Literature	Pub. Number
Need to Test BER?, Brochure	5968-9250E
Agilent ParBERT 81250, Mux/Demux Application, Application Note	5968-9695E
Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Photo Card	5980-0830E
Agilent Productivity Assistance	5980-2160E
Agilent ParBERT 81250 43.2/45G Product Overview	5988-3020EN
Agilent ParBERT 81250 Paralel Bit Error Ratio Test Platform	5988-5901EN
Agilent 81250 ParBERT Product Note (The influence of Generator Transition times on Characterization Measurements)	5988-5948EN
Agilent ParBERT 81250 Automatic Phase Margin Measurements at 43.2 Gb/s	5988-5654EN
Agilent ParBERT 81250 Product Overview	5968-9188E

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