IBIS Modeling and Simulation of High-Speed Fiber-Optic Transceivers

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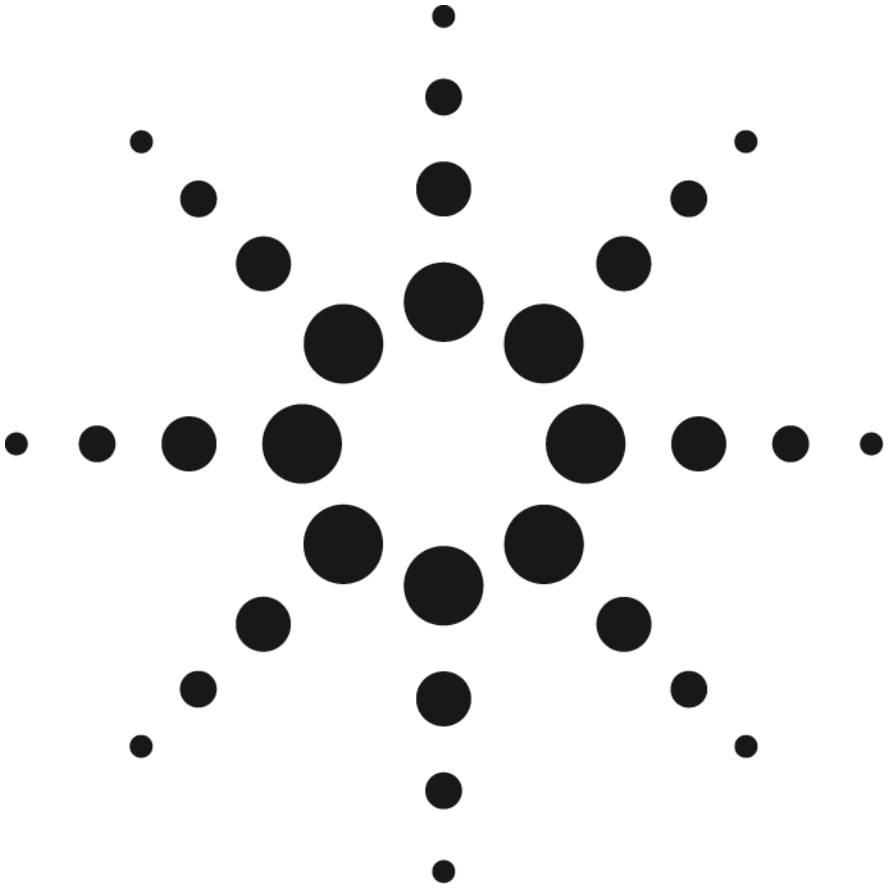
White Paper



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Abstract

The I/O Buffer Interface Specification (IBIS) in its current version 3.2 allows the use of Electrical Board Description (EBD) files which make the accurate modeling of very-high speed, internally AC coupled transceivers possible. At data rates of 2Gbit and higher the internal Printed Circuit Board (PCB) layout of the transceiver has an influence on the signal shape at the component pin. This paper reviews some of the techniques that are used within Agilent Technologies to develop and verify models for the latest generation of 2.5Gbit transceiver components. Signal integrity simulations for typical applications, which employ these models, will be discussed.

Introduction

The wide adoption of the Gigabit Ethernet networking standard has increased system data rates well into the 1000MHz range in recent years. This boundary has been pushed even further by the latest transceiver components. Fibre-Channel transceivers operating at 2Gbit/s data rates are available, and the first 10Gbit/s Ethernet transceiver components conforming to the Xenpak Multi Source Agreement with its 4*3.125 Gbit/s XAUI interface are just a few months away. Digital system design has therefore moved deep into the Multi-GHz range, with signal rise and fall-times of the order of 100ps or less.

It is a well-known fact that Signal Integrity (SI) simulations become necessary when system designs break the 50-100MHz barrier [1], and are virtually mandatory in the GHz range. SI simulations are used to ensure the quality and accurate timing of electrical signals [2]. The benefits of SI analysis early in the design cycle are well established, as it allows the identification and resolution of SI problems like overshoot, ringing, crosstalk, delay mismatches, etc. before the first prototype is built.

Good component models are a prerequisite to carry out meaningful and realistic SI simulations. Component models can be created in Spice, IBIS, and a number of proprietary formats; a thorough discussion of the advantages and limitations of the various approaches can be found in [3]. Due to its standardization, IBIS has increasingly gained support with component manufacturers and acceptance within the SI community in recent years. Discussions and details of the IBIS standard can be found in [4], [5], and on the official IBIS website of the Electronic Industries Alliance: http://www.eigroup.org/ibis/ibis.htm

IBIS Models for High-Speed Fiber-Optic Transceivers

Agilent Technologies has recently released a range of Small Form Factor (SFF) high-speed transceiver products for the Ethernet, Fibre Channel and the Metropolitan Telecom markets. Pluggable SFF Fibre Channel transceivers like the HFBR-5720L operate at a data rate of 2.125Gbit/s, while the SONET compliant family of the HFCT-5942L operates at the OC-48 data rate of 2.488Gbit/s.

The construction of IBIS models for components operating in the 2-3Gbit/s range poses additional challenges. The rise- and fall times of these high-speed components are on the order of 100ps, which equates to an electrical length *le* of about 1.5cm in FR-4. In order to treat a transceiver as one single lumped component, the physical dimension *lp* needs to satisfy the following condition [6]:

$$lp < le / 6$$

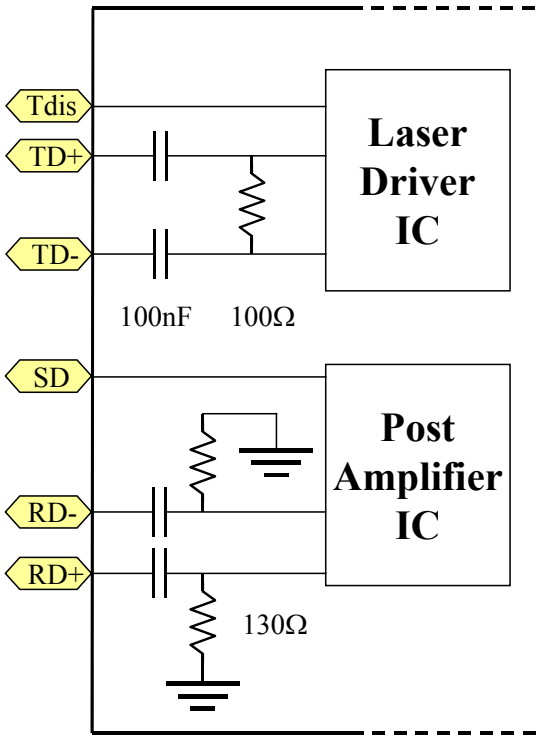
The physical length *lp* of SFF transceivers without the optical connector is about 1 to 2cm and therefore clearly too large to meet the above condition. This implies that the structure of the internal Printed Circuit Board (PCB) of the transceiver component needs to be accounted for and treated as a distributed element.

The short effective length of signals with such fast edge rates makes it furthermore necessary to provide termination of the inputs and outputs as close to the laser driver and receiver postamplifier ICs as possible. Termination resistors and AC coupling capacitors for the high-speed signals are therefore included on the internal PCB of the transceiver and need to be accounted for in accurate electrical models of the components. Figure 1 shows a circuit diagram of the input and output connections of fiber-optic transceiver HFCT-5942L as a typical example.

The IBIS standard version 3.2, which was ratified in September 1999, allows for the description of component internal PCBs. The IBIS 3.2 standard document refers to components with such a level of complexity also as “board-level components”. The connections between the active and passive elements on the PCB are defined in an Electrical

Board Description (EBD) file, which model developers will supply in addition to the IBIS files of a component. The IBIS files themselves contain the electrical characteristics of the Input and Output buffers of Integrated Circuits (ICs) inside the board-level component, and also the parameters of any additional passive elements like termination resistors or series capacitors. For a complete description of a board-level component both the EBD and IBIS files are required.

Figure 1. AC coupling, termination and bias resistors for the high-speed data inputs (TD+, TD-) and outputs (RD+, RD-) of transceiver component HFCT-5942L



This paper will describe the techniques that are used within Agilent Technologies to develop and validate complete IBIS models, i.e. the combined IBIS and EBD models. The emphasis will be on the effect of the EBD model file on the combined models. Details of the development of Input and Output buffer models for the IBIS file itself can be found in [7].

In order to check the validity of using behavioral IBIS models at 2Gbit/s data rates and higher, the results of simulations using a Spice model will be compared with IBIS simulations. For this we will go beyond standard test load verification checks and we will analyze the effect of real-world topologies on the signal shape launched by the outputs of a high-speed transceiver. This should indeed provide a stringent test of the IBIS model quality and enable us to check out the limits within which IBIS modeling can provide accurate results. After the validity of the IBIS modeling approach has been established a typical signal integrity case study utilizing IBIS models will be carried out.

The Electrical Board Description File

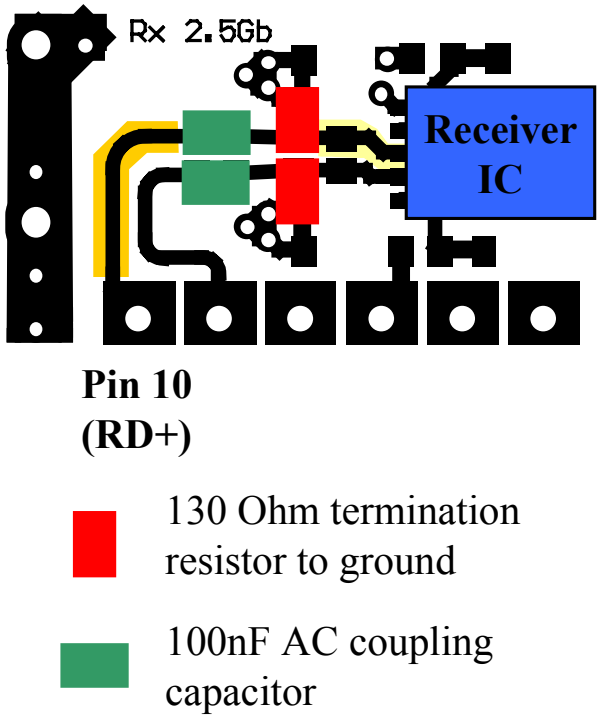
The EBD file describes how the user accessible pins are connected with the internal structure of a component, e.g. a fiber-optic transceiver. EBD files are structured very similar to IBIS files. The syntax specification can be found in Section 8 of the IBIS 3.2 standard document and will not be repeated here in depth, however, some key aspects that are important for the understanding of the models for fiber-optic transceivers shall be highlighted.

An EBD file must contain certain keywords like [IBIS Ver], [File Name], [Manufacturer] etc., and a complete list of the user accessible pins of the component under the heading [Pin List]. The actual description of the signal paths follows after the keyword [path description]. A path description is required for each pin whose signal name is not “GND”, “POWER”, or “NC” (Not Connected).

Figure 2. EBD File: Path description for pin 10 of transceiver HFCT-5942L

```
[Path Description] RD+
Pin 10
|
Len = 1 L=1.50n C=0.60p R=0.01 /
Len = 1 L=0.78n C=0.18p R=0.01 /
Node c02.1
Node c02.2
Len = 1 L=0.57n C=0.06p R=0.01 /
Node r131.1
Len = 1 L=1.85n C=0.09p R=0.01 /
|
Node hfct_5942.10
```

Figure 3. Receiver PCB of the HFCT-5942L showing the signal path from external pin to the postamplifier IC.



An example for a path description is shown in Figure 2 for pin 10 (Receiver Data Out, RD+) of the HFCT-5942L. The corresponding section of the internal PCB is shown in Figure 3.

It is evident from Figure 2 that all path descriptions either start or end in an external pin. They are always read from the top, i.e. the example begins at external pin 10, which is followed by two transmission line sections, which then connect to node "c02.1" This node links the EBD file with the IBIS file containing the component parameters for the serial 100nF capacitor. A table at the end of the EBD file following the keyword [Reference Designator Map] must resolve the node names and map them onto IBIS file names that have to reside in the same directory as the EBD file. The path description shown in Figure 2 finally ends in node "hfct_5942L.10" which is a reference to the IBIS file containing the properties of the high-speed output buffer of the receiver's postamplifier IC.

It is also worth noting that transmission lines are described in terms of their total series inductance L, total series capacitance C, and total resistance R. The statement "Len=1" tells the simulation software to interpret this line as a distributed element (with the length of one 'unit'). The transmission line parameters L and C can be easily converted into the perhaps more familiar impedance $Z0$ and time delay t_d parametric description [8]:

$$ZO = \sqrt{\frac{L}{C}}$$

$$t_d = \sqrt{LC}$$

Verification of IBIS Models

Before IBIS models are released it is important to verify that the model accurately reflects the component's performance characteristics. Within Agilent Technologies we have adopted the following approach for the verification of the high-speed signal lines:

i) The simulated eye diagram of the component's data output pins into a typical load needs to closely resemble measured receiver eye diagrams.

ii) If available, differential Time Domain Reflectometry (TDR) measurements of the high-speed inputs will be fitted in order to confirm parasitic capacitances and inductances of the input signal paths.

iii) The differential input signal must be reproduced with little deterministic jitter at the input buffers of the laser driver *die*. This is a necessary condition for the generation of jitter-free optical eye-diagrams.

We will discuss the merits of this approach in the following. Figure 4a shows a measured receiver eye-diagram in comparison to the simulated output of the unpackaged postamplifier *die* in Figure 4b. The data in Figure 4b therefore excludes any contribution from the IC package parasitics and the EBD file. It is clear from these two eye-diagrams that the edge rates and the overall signal shape of the post amplifier output are altered under the influence of the package parasitics and the layout of the internal PCB.

Figure 4a. Single-ended receiver eye-diagram of the HFCT-5942L

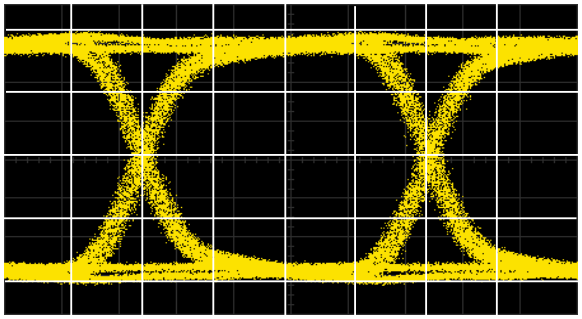


Figure 4b. Output signal of the unpackaged receiver postamplifier *die*

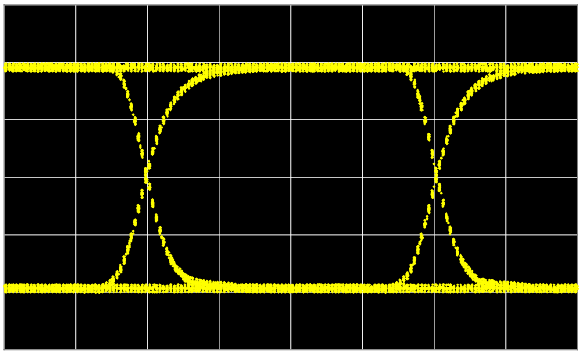
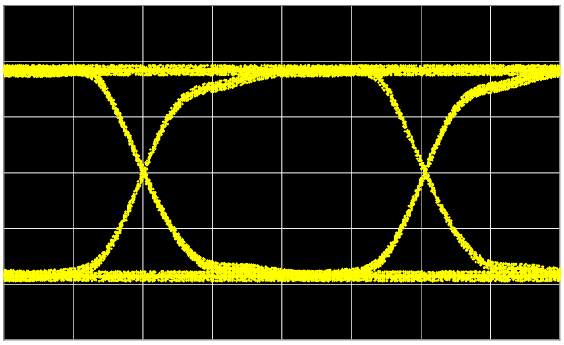


Figure 4c. Simulated single-ended receiver eye-diagram using the full component model including the EBD file



Adding IC package parasitics and the electrical description of the internal PCB leads to the eye-diagram in Figure 4c. A low level of noise has been added to facilitate the comparison with the measured eye in Figure 4a. It is apparent that by using an accurate IBIS 3.2 model a good overall fit between the simulation and the measurement could be achieved, where the model also reproduces the finer details in the ones and zeros.

It is worth noting, however, that such a good agreement between component model, simulation, and measurement was accomplished by increasing the impedance Z0 of the short transmission line between the termination resistor and the postamplifier IC pin above its nominal value of 50Ω. The increase that is required for a good match is beyond typical manufacturing tolerances. Even though it is not entirely clear at this point why this is necessary, we believe that the excess distributed inductance provided by this increase reflects either IC package parasitics or discontinuities between the IC and the PCB that could not be captured in the package model parameters of the IBIS file. This effectively blurs the line between the PCB description which is provided by the EBD file and the IC package model parameters normally accounted for in the IBIS file. It should be emphasized that this level of detail is only resolved due to the extremely fast rise- and fall-times of the HFCT-5942L's post amplifier IC of about 50ps (at *die* level). Here the EBD file provides the model developer with the means to expand the model's complexity to match the requirements of today's high-speed fiber-optic components.

The high-speed inputs of the HFCT-5942L have been characterized with differential TDR measurements. A description of this technique can be found in references [9], [10], [11]. Differential TDR proves to be particularly useful for the characterization of differentially terminated input signals where single-ended measurements are difficult to interpret or would require modifications to the transceiver circuit board. The measured TDR signal is shown in Figure 5 together with a fit to the data using a detailed representation of the component internal PCB. Again, the overall fit is satisfactory. Similar to the case of the high-speed outputs, the impedance of the transmission lines between the 100Ω differential termination resistor and the laser driver IC pins (see also Figure 1) had to be increased above their nominal value of 50Ω to achieve a good match. As in the case for the outputs, this is more likely to be a contribution of the IC package parasitics that is rolled into the transmission line rather than an actual deviation of the transmission line from 50Ω. Unfortunately, a more detailed analysis is not possible at this point, as it would require a higher measurement resolution. Higher resolution measurements or an independent characterization of the IC package should help us to further clarify the details of the transceiver IBIS model at the interface of the internal PCB and the IC package in the future.

Figure 5. Differential TDR measurements and simulation taking into account the internal PCB and the IC package parasitics.

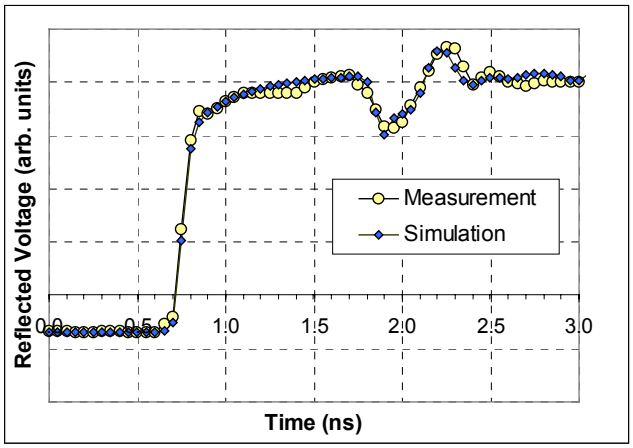
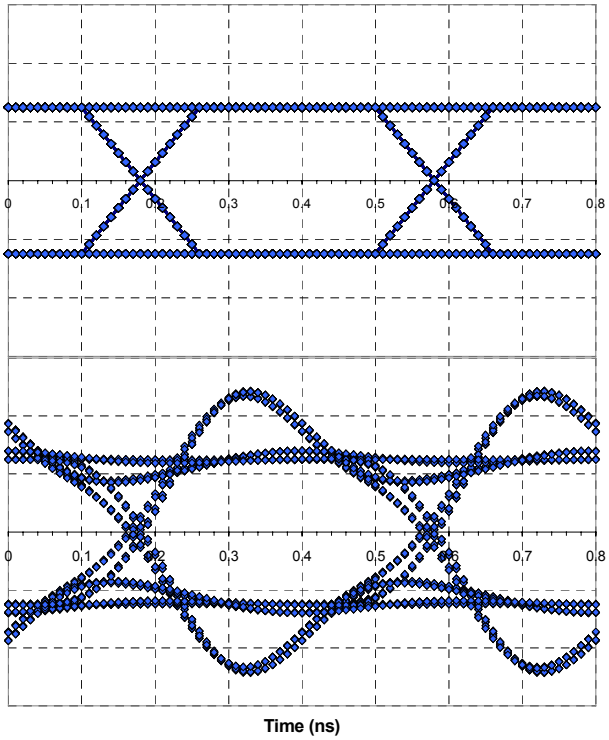


Figure 6. Differential input signals, the upper eye diagram shows the externally generated signal, the lower eye diagram shows the differential voltage at the input buffer of the laser driver *die*.



The EBD model and IC package parasitics that have been derived from the fit to the TDR measurements are checked in a simulation where a pseudo-random signal is supplied to the high-speed inputs TD+ and TD- of the transceiver. In order for the model parameters to be consistent, the jitter of the differential input voltage at the input buffer of the laser driver *die* needs to be less than the jitter of the optical output signal. Furthermore, the eye diagram needs to be open with little infringement of the inner section. The results of the simulation are shown together with the eye of the driving pulse sequence in Figure 6.

It is evident from Figure 6 that even though there is some overshoot in the differential signal at the leading edges of the eye diagram, there is very little infringement of the inner section. In addition, the deterministic jitter that is created by the parasitic inductances and capacitances of the input stage are of the order of 20ps (equivalent to 50mUI) peak-to-peak, which is below the measured maximum jitter generation of 70mUI [12]. This gives us confidence that the developed IBIS model accurately reflects the electrical performance characteristics of the transceiver inputs.

IBIS Models in "Real-World" Circuits

In the previous section we have seen that simulations utilizing IBIS models can accurately reproduce the behavior of components in "ideal" environments, i.e. when the buffers drive the same test loads that were used to generate the IBIS models. However, in order to gain confidence in using IBIS models at multi-gigabit data rates, it will be very interesting to compare the signal shapes of simulations of "non-ideal" circuits utilizing IBIS as well as Spice model representations of the same buffers. This will be a much more stringent test of the quality of the IBIS model and of the validity of using a behavioral modeling approach for transceiver components at these elevated bit rates.

Let us consider the following the situation: A transceiver of the HFCT-5942L family drives a 250ps long transmission line (nominal Z0=50Ω) which is terminated by a 50Ω resistor. However, due to manufacturing tolerances the actual line impedance is 60Ω, and resistors with a 10% tolerance have been chosen for the termination. The worst reflections will therefore occur for a resistor value of 45Ω. Figure 7 shows this situation schematically.

The results of a full Spice simulation are compared with a simulation utilizing the transceiver's IBIS model in Figure 8. A pseudo-random 2.5Gbit/s pattern was used in both cases. The signal displayed in Figure 8 is the voltage drop at the termination resistor. Both simulations were carried out in Avanti HSpice that allows the

simultaneous use of IBIS and Spice models of the same component. For the full Spice simulation an HSpice model of the PECL output buffers of the postamplifier IC of the HFCT-5942L was used. In both cases the EBD file was translated into a Spice netlist using the T-Line element for the description of sections with distributed elements.

The comparison is very encouraging. The overall signal shapes are very similar; the edge rates and dc-voltage levels are accurately reproduced by the IBIS model. There is a little difference in the fine detail on a sub 100ps timescale that will require further investigation in the future. However, this difference is only 5% in terms of the total signal

Figure 7: Circuit schematic for the simulation test comparing Spice and IBIS component models

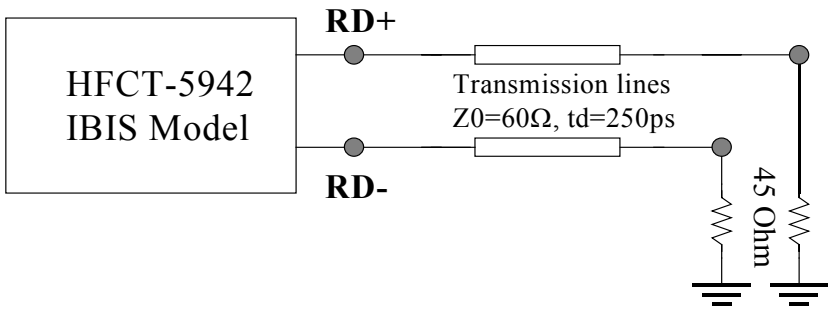


Figure 8: Simulation results for the set-up shown in Figure 7. Displayed is the voltage at the termination resistor.

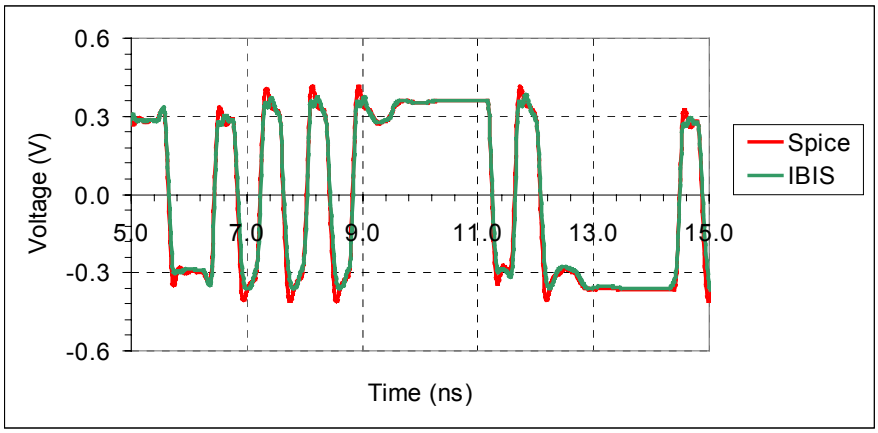
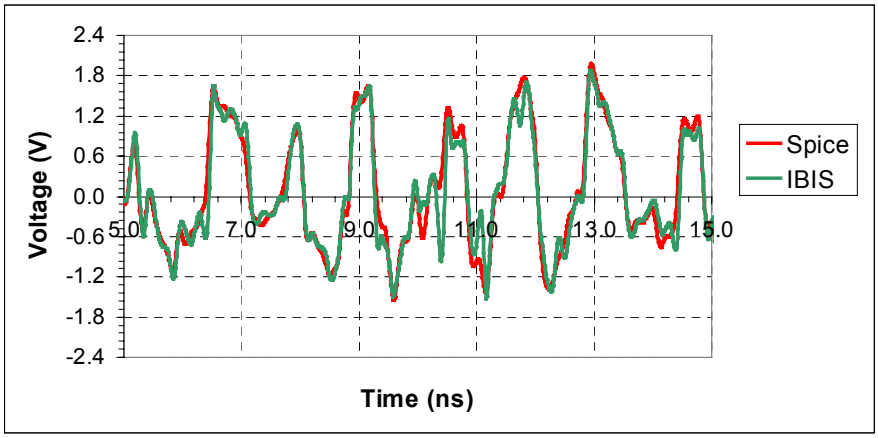


Figure 9: Same bit sequence as in Figure 8, but the termination resistors in Figure 7 have been removed so that the transmission lines are now open ended.



swing and we believe that this is acceptable given the differences in the modeling approach between transistor-level Spice models and the behavioral IBIS description.

In order to test the IBIS model under more extreme conditions we removed the termination resistors and left the ends of the transmission lines unterminated. The open ends of the transmission lines fully reflect the output signal from the component. Since the component's output buffers cannot fully absorb the reflected signals due to the low impedance of the emitter followers, a fraction of the signal will be bouncing back and forth. The precise signal shape at any point in time depends on the previous bit sequence. This is a stringent test for the IBIS model as it is possible in this set-up for small differences to accumulate over time. The same pseudo-random sequence as for the simulations in Figure 8 was used.

The result of this extreme-case simulation is displayed in Figure 9. The IBIS model simulations trace the HSpice model simulations with a high degree of accuracy. As expected, some differences get more pronounced, as can be seen in the finer details between the main peaks. However, the main peaks are accurately reproduced, both in terms of edge rate and maximum peak level, even though the reflected voltage levels can reach up to three times their steady state value. This is a very encouraging result proving that IBIS models can be used with confidence in signal integrity simulations. It furthermore indicates that the results of simulations using IBIS models can be trusted even when extreme cases are analyzed.

The quality of IBIS models critically depends on the quality of the Spice model from which it is derived, or, if the IBIS model is based on measurements, on the accuracy of the measurements. The high bit rate makes tough demands on both, and it is imperative to verify the model's performance against either Spice simulations or additional characterization data of a large population of parts as can be found e.g. in the characterization report of transceiver components.

Signal Integrity Case Study

In the previous section we have seen that simulations utilizing IBIS models can be very useful tools for the analysis of the Signal Integrity of a relatively simple high-speed electrical circuit. We will take this one step further in this section and take a look at one of Agilent Technologies' recent reference designs comprising a Fibre-Channel transceiver, HFBR-5720L and a Serializer/Deserializer IC (SerDes), HDMP-2630.

The reference design is described in detail in references [13] and [14]. One characteristic feature of the reference design's PCB is that due to the pin layout of the two components the high-speed differential pairs connecting the transceiver outputs (inputs) with the inputs (outputs) of the SerDes need to cross each other. This is achieved by re-routing the differential pair starting at the RD+/- pins of the HFBR-5720L from layer 3 of the PCB to layer 6 halfway between the transceiver and the SerDes.

Figure 10: Schematic circuit diagram for the Signal Integrity study of the 2.125Gbit/s Fibre Channel physical layer reference design for Agilent Technologies' HFBR-5720L and HDMP-2630/2631.

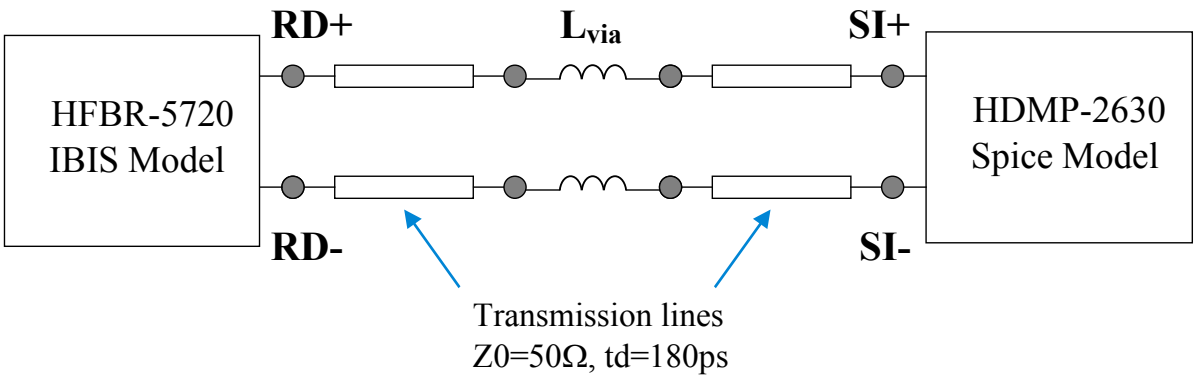


Figure 11: Signal at pin of SerDes HDMP-2630

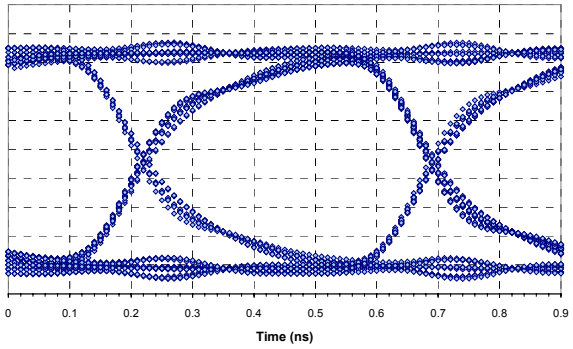
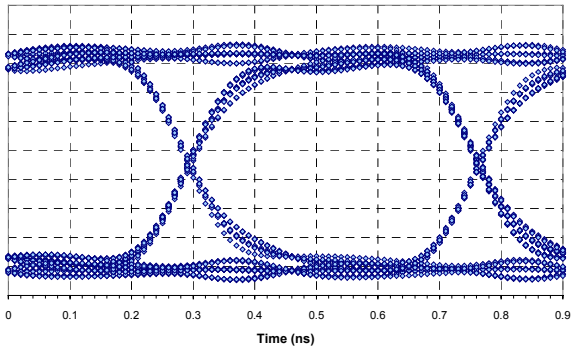


Figure 12: Signal at *die* of SerDes HDMP-2630



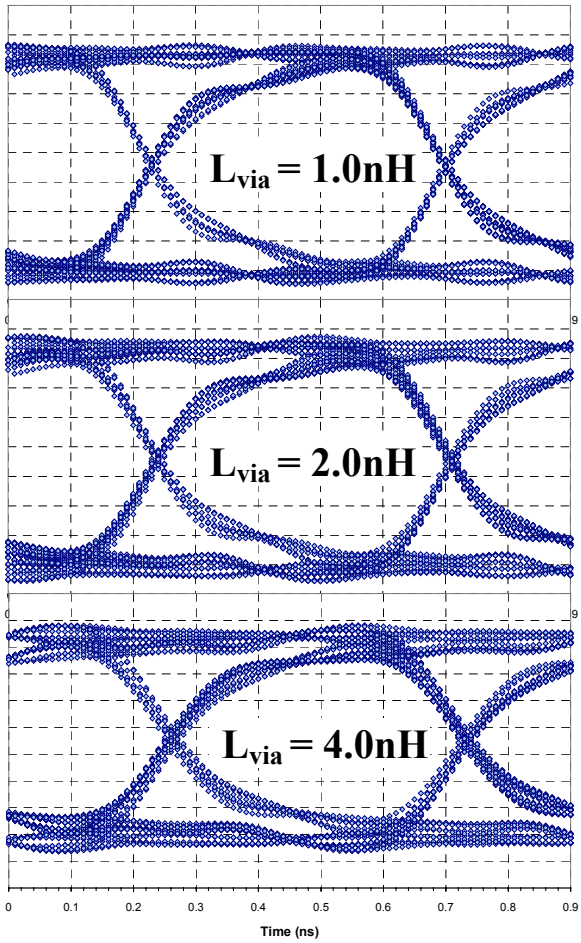
This situation is schematically shown in Figure 10 where the via has been modeled as a single lumped inductive element. This is a very simple model neglecting the via landing pad capacitances, but we still expect it to be a reasonable first order approximation [6]. For the simulation of the two components, an IBIS model was used for the HFBR-5720L transceiver, and an HSpice model for the HDMP-2630 SerDes. The HFBR-5720L IBIS model is available for download from Agilent Technologies website, the HSpice model for the HDMP-2630 SerDes can be obtained from Agilent Technologies upon request.

The single-ended eye diagrams of the electrical signal at the pins of the SerDes and at the *die* are shown in Figures 11 and 12, respectively. L_{via} has been set to 0.5nH in this simulation to provide a lower limit reference for the following case study where we will systematically increase L_{via} to investigate its effect on the signal propagation. The signal will be probed at the SerDes IC pin.

The effect of increasing L_{via} in steps to 1.0nH, 2.0nH and 4.0nH is displayed in Figure 13. The succession of graphs nicely shows that the increase of L_{via} not only creates jitter on the rising and falling edges, but also leads to a closure of the eye as it takes more time for the signal to reach its steady-state level. Increasing the via inductance from 1nH to 4nH almost doubles the deterministic jitter from 14ps to 27ps, and leads to a 10% reduction of the eye opening.

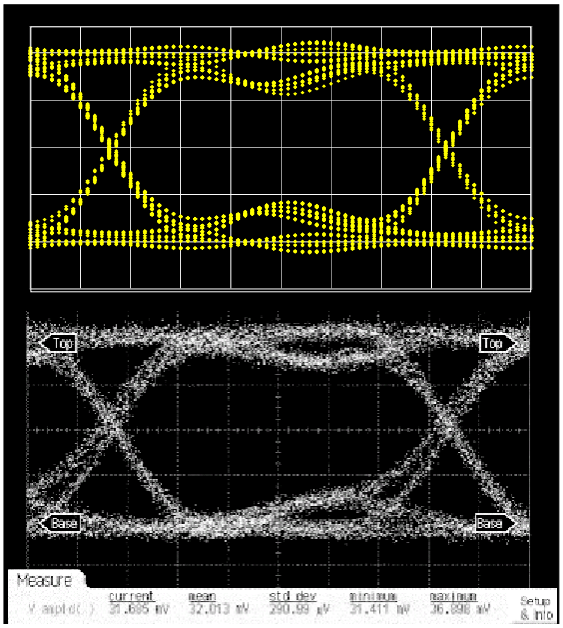
It is also clear from Figure 13 that the via only has a small effect on the signal shape as long as its inductance does not exceed approximately 2nH. Care has been taken in the reference design to provide as good a connection between the transceiver and the SerDes as possible. The most likely value for the via inductance will be between 1 and 2nH, which is in line with typical lumped

Figure 13: Eye diagrams for L_{via} =1.0nH (top), 2.0nH (middle), and 4.0nH (bottom). Shown is the single-ended signal at the pins of the HDMP-2630.



parameter values for multi-layer PCBs [15]. This is also evident in the measurements shown in reference [13], which are reproduced below in Figure 14. The diagram at the bottom shows measured data at the test points of the reference board where clear and open eye-diagrams are a good indicator for the low inductance of the via and thus the high quality of the PCB design. The upper eye diagram has been simulated by adding the required circuit connections for the test points to the schematic in Figure 10. The via inductance was set to 1.5nH. We believe that the agreement between measurement and simulation is very satisfactory.

Figure 14: The diagram at the bottom shows the signal at the test point RX(+) of the Reference Design Board. The diagram at the top shows the simulated signal at the test points.



Summary

In this article we have reviewed the IBIS 3.2 standard and highlighted the importance of the EBD file for the description of fiber-optic transceivers at 2Gbit/s and higher data rates. We have shown that accurate models can be developed and we have reviewed some of the verification techniques that are used within Agilent Technologies to ensure the accuracy of the IBIS models at these high data rates.

The validity of the behavioral modeling approach has been verified by comparing Spice and IBIS models of the same output buffers at OC-48 data rates for a "real-world" circuit simulation where good agreement was achieved. This then allowed us to carry out a Signal Integrity study for one of Agilent Technologies' reference designs where the effect of vias on the signal propagation along differential pairs was investigated. This showed that up to about 2nH inductance of the via can be tolerated. Higher inductance causes the received signal to deteriorate visibly.

Acknowledgement

I am indebted to my colleagues in the Application Engineering and R&D teams for their ongoing and invaluable support of this work. I would further like to express my gratitude to Tom Dagostino of Mentor Graphics for his advice in the model development process.

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