Making Matching Measurements for Use in IC Design

Application Note

Agilent 4073A Ultra Advanced Parametric Tester and 4156C Precision Semiconductor Parameter Analyzer

New 4073 Features

Voltage Accuracy
- **Resolution 0.1 µV**
- **Reading 0.01%**

Current Accuracy
- **Resolution 1 fA**
- **Reading 0.06%**

New 4156C Features

Voltage accuracy
- **Resolution 0.2 µV**
- **Reading 0.03%**

Current accuracy
- **Resolution 1 fA**
- **Reading 0.04%**

Introduction

Matching applications play a key role in modern IC design: they act as the heart of a system on a chip (SOC) IC by providing a buffer between the exterior analog world and the IC's internal digital circuitry. These matching applications depend on the fine analog matching characteristics of transistors, resistors, and capacitors found in today's IC process technologies. For example, a cellular phone receiver or transmitter uses a high-frequency mixer or modulator that requires accurate transistor matching in several circuits. These circuits include analog-to-digital and digital-to-analog (AD/DA) converters, which use both transistor matching and resistor or capacitor techniques, as well as operational amplifiers, which depend upon the precise matching of transistors and resistors. In the past, these analog circuit blocks were separate components that were connected to the digital ICs on a circuit board. With the advent of the SOC paradigm, however, these circuit blocks are now integrated into a single IC, both to increase performance and to reduce cost.

The continuing trend in SOC design is to use a state-of-the-art, fine line-width process to achieve both performance and cost targets. While the use of finer line widths on ICs results in a more competitive product, they unfortunately work in direct opposition to performance matching goals. Therefore, the optimization of device matching characteristics has become increasingly important both to ensure IC perfor-

mance and to enhance IC yields as the industry design philosophy moves toward SOC solutions.

Matching applications often exceed the specified resolution and repeatability limits of the instrumentation used to measure them. Consequently, special measurement techniques to overcome these limitations present unique challenges. In addition, since matching characteristics must be compared across dies, wafers, and wafer lots, any ability to perform automated measurement greatly improves the overall efficiency of a measurement solution. The Agilent 4156C Precision Semiconductor Parameter Analyzer and Agilent 4073A Ultra Advanced Parametric Test System satisfy these requirements as long as certain measurement procedures are adhered to.

This application note addresses the issue of component matching from a measurement perspective, and it explains how to utilize both Agilent semiconductor parameter analyzers as well as parametric test systems to make these measurements. In particular, this application note provides information on how to utilize the full capabilities of both Agilent instrument and system products to make measurements that initially appear to be beyond their measurement capabilities.

Matching Definitions

There are four terms to consider when discussing device matching or device mismatching performance: random mismatch, systematic mismatch, pair matching, and long-distance matching. These are illustrated in Figures 1 and 2.

Random and systematic mismatch describe the type of mismatch variations that are observed. Pair and long-distance matching describe the types of applications in which circuit components are used.

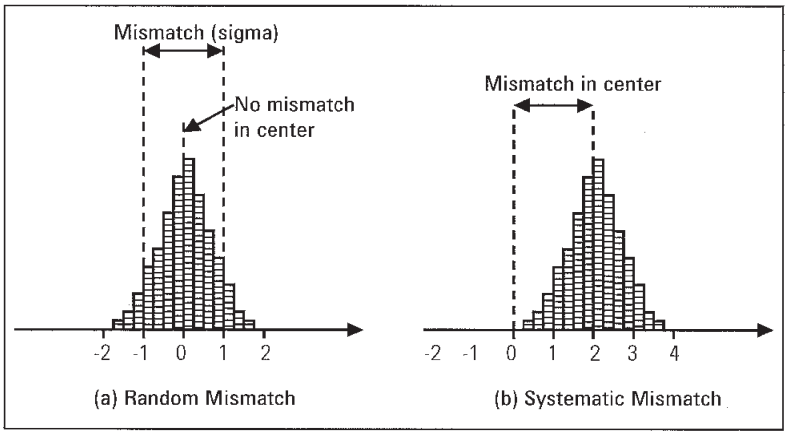

Figure 1. Two types of matching error

Random mismatch

Random mismatch is a truly random variation caused by factors such as physical irregularities, process variations, noise, and so fourth. Figure 1(a) shows a typical random mismatch distribution where the average mismatch is zero and where the distribution is symmetrical around zero.

Systematic mismatch

Systematic mismatch is usually due to asymmetrical circuit layout, uneven mechanical stress from other circuit layers, spot thermal effects from adjacent circuitry, or noise. In all of these cases some sort of systematic offset occurs. Figure 1(b) shows a typical systematic mismatch distribution where center of the distribution is offset and where the distribution is symmetrical around this offset.

Pair matching

Pair matching (sometimes referred to as short-distance matching) is illustrated in Figure 2(a). It is used when two devices are located very close to each other on a chip. Pair matching provides the best matching performance, since the two devices are physically close to one another and therefore have electrical characteristics as identical as is realistically possible.

Long-distance matching

Long-distance matching, which is illustrated in Figure 2(b), is used for measuring the matching characteristics of two or more devices located more than 100 μm apart

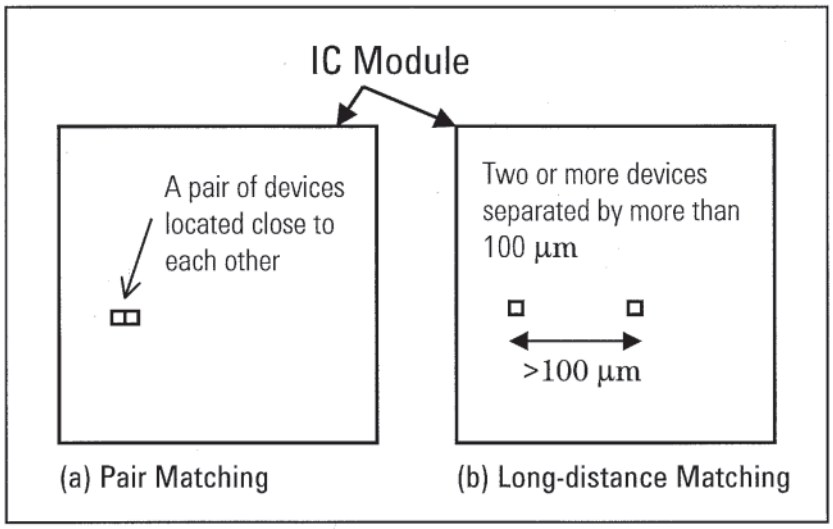

Figure 2. Pair and long-distance matching

on a chip. While pair matching provides better matching performance than long-distance matching, many applications such as AD/DA converters require long-distance matching. Long-distance matching behavior depends more strongly on process variation than does pair matching, so extensive analysis for process dependency is generally required.

Matching Requirements for Device Type

Typical matching characterization includes bipolar junction transistor (BJT) pair matching, MOS field effect transistor (MOSFET) pair matching, resistor matching, and capacitor matching. All of these devices can be used in both pair matching and long-distance matching situations. In general, matching performance degradation is inversely proportional either linearly or to the square root of the device size. Again, this increases the difficulty of the design of an SOC device because SOC devices are typically created in the most advanced process (e.g., tightest design rules available).

Requirement for BJT matching

Bipolar junction transistors provide superior matching and low noise capability over a wide range of operating frequencies (basically from dc to the GHz range). Typical parameters for characterizing bipolar transistor matching are

- β matching
- Vbe or Ic matching.

These parameters are usually compared at several bias points. The accuracy required for parameter matching is typically below 1%. Therefore, the accuracy of the instrumentation needs to be roughly 0.1%, or about one-tenth that of the required parameter accuracy.

Typical transistor characteristics for matching comparison can be expressed by Equation 1.

Equation 1

$$Ic = \beta \times Ib$$

where,
β is DC current gain and,
Ib is base current at Vbe > 0.1 V condition.

At room temperature, Equation 1 can be expressed as follows:

Equation 2

$$Ic = Ico \times \exp(Vbe \times q/KT) = Ico \times \exp(Vbe/0.026\ V)$$

where,
Ic is collector current,
Ico is extrapolated Ic at Vbe = 0 V,
q is electronic charge 1.6×10^{-19} C,
K is Boltzmann's constant 1.38×10^{-23} J/K,
T is Kelvin temperature (K) and,
Vbe is Base – Emitter voltage.
Note: J/C = V

The matching evaluation is made by relating the parameters in Equations 1 and 2. Equation 1 shows that Ic versus Ib is in a linear relation and, therefore, the accuracy requirements for the Ic and Ib measurements are the same.

Equation 2 expresses the relation of Ic versus Vbe. It shows, for example, one percent IC change is generated by only a 260 μV shift in the base bias voltage. (ΔVbe : 260 μV = (0.026 $\times$ ln1.01) Since achieving 1% characterization accuracy requires 0.1% measurement accuracy, 26 μV (=0.026 $\times$ ln1.001) accuracy typically is required for transistor Vbe matching characterization.

Requirements for MOSFET matching

MOSFETs can also be used for matching applications where only moderate performance is required. Although the MOSFET is noisier than the BJT and exhibits more variation in matching performance, MOSFETs have the advantage of fitting in easily to a standard CMOS IC process resulting in a lower overall cost. Typical parameters for characterizing MOSFET matching are

- Vth matching
- Id or Idss matching
- Vg - Id matching

These parameters are compared in a linear, or saturated, operating region.

The basic relation of Id and Vg in the saturation region can be expressed using the square law model in Equation 3.

Equation 3

$$Idsat = Gm \times (Vg - Vth)^2$$

where,
Idsat is drain current at saturation region,
Gm is transconductance,
Vg is gate voltage, and
Vth is threshold voltage.

The square law theory expressed in Equation 3 can be used to derive a relationship showing the sensitivity of Vg to small changes in Id and to verify the required instrument accuracy for matching characterizations. Using simple calculus we can take the differential of both sides of Equation 3 and arrive at an expression showing the sensitivity of Vg to small variations in Vg and Id. The result is shown in Equation 4.

Equation 4

$$\Delta Vg = \frac{(Vg - Vth)}{2} \times \frac{\Delta Id}{Id}$$

where,
ΔVg is gate voltage change, and
ΔId is drain current change.

From this equation we can see that for a fixed Vg and Vth, any percentage change in Id results in approximately a one-half percent change in Vg. If we assume that for advanced processes Vd has about 1 V applied to it, then a

good estimate for (Vg – Vth) is 0.2 V. Therefore, from Equation 4 we can see that a 0.1% change in Id will produce a change of about $0.001/2 \times 0.2 = 0.0001$ V, or 100 μV in Vg. This value gives a rough estimation of the minimum instrument resolution requirements for characterizing MOSFET Vth matching characterization in future MOS transistor designs.

Requirement for resistor matching

Two examples of typical of resistor matching applications are: pair matching for precision operational amplifier design; and semiconductor process alignment checks and ratio matching for applications such as AD/DA converters and voltage dividers.

When matching resistors are placed on an SiO_2 insulator, current flowing through the resistors generates heat via Joule heating ($I^2 \times R$). This restive heating effect limits resistance measurement accuracy because it changes the resistor value. The resistor matching accuracy requirements limit the amount of resistance change that the circuit can tolerate due to the Joule heating effect. This maximum tolerable resistance variation can then be translated into maximum allowable power dissipation which, in turn, can be related back to a minimum voltage resolution necessary to meet the circuit matching requirements. In order to determine the maximum allowable power, the following three parameters must be known: 1. the area of the resistor; 2. the temperature coefficient of the resistor; and 3. the required matching accuracy. Once the maximum power applicable to the resistor is determined (and the area of the resistor becomes known), the maximum allowable voltage to the resistor can be calculated as shown in Equation 5.

Equation 5

$V_{max} = SQRT(P_{max} \times R)$

where,
Vmax is allowable maximum voltage,
Pmax is allowable maximum power, and
R is resistor value

For example, to obtain a voltage resolution with 0.1% accuracy in a copper Van der Pauw structure with an equivalent resistance of 10 mΩ typical for a 1 μm-thick film, the measurement instrumentation must be able to resolve down to about 1 μV. *For more detail, refer to Agilent Application Note 4156-11, "Precision Measurement of Metal Line Width in Sub-quarter Micron Interconnect Systems," (Publication number 5988-2695EN).*

The Van der Pauw structure is a relatively extreme example. A metal line 1 μm wide and 100 μm long typically requires that the measurement instrumentation be able to resolve to the tens of microvolts in order to obtain 0.1% accuracy. Equation 5 shows that required voltage resolution increases as the square root of the resistance value. Since this is a relatively weak dependence on R, 10 μV is a good estimate of the measurement resolution requirement for most resistor matching applications.

Requirement for capacitor matching

The capacitors in an IC that are used for matching applications are usually too small to be measurable, even using a precision capacitance meter. Moreover, the capacitance of the metal lines necessary to connect the internal capacitors to the external capacitance meter adds too much error to the overall measurement. Therefore, capacitance matching requires special circuitry built into the wafer to determine the capacitor matching characteristics. For these reasons, capacitance matching is beyond the scope of this application note and is not covered.

Matching Measurement Techniques

The measurement accuracy of an instrument is usually expressed in terms of percent accuracy plus an offset error term.

A key concern in matching characterization is having sufficient measurement resolution to detect small differences in the components being measured. When the general specification limits of a measurement instrument do not ensure sufficient resolution, special measurement techniques are necessary in order to make the measurement. These techniques are discussed later in this application note. Percent accuracy, in contrast with resolution, is less

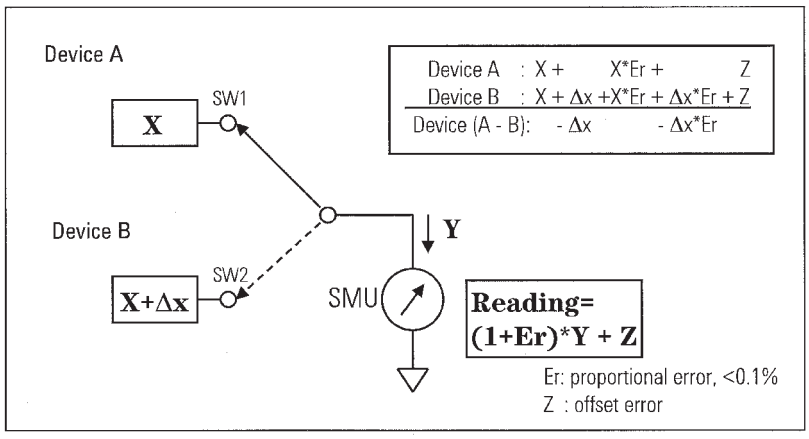

Figure 3. Cancellation of SMU error

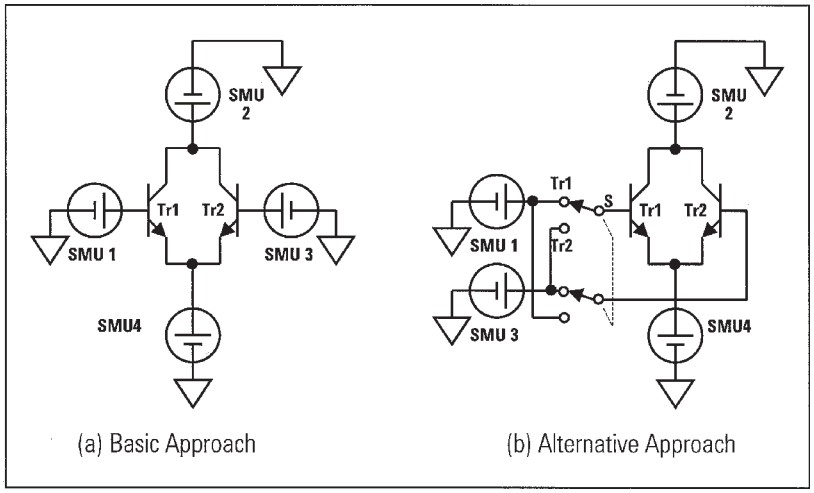

Figure 4. Typical setup of transistor matching measurement

of a problem when making matching measurements. This is because the required performance is usually within the general measurement specifications of the instrument, or it can be obtained with minor modifications to the basic measurement technique. The following are some of the techniques that are commonly used in matching characterization.

Utilize the same SMU

One means to eliminate measurement error in matching measurements is to use the same measurement resource to measure both matching elements. For parametric test, this means using the same SMU to measure both matching structures. Assuming the SMU is stable while the matching measurements are executed, a percentage error "Er" and an offset error "Z" that is the same for both measurements can be expected. Figure 3 illustrates this general case, where the measurement yields a value of "X" for device A and "X + Δx" for device B. In this example, "Δx" is the pair mismatch. The difference between the two measurement readings, "Δx (1 + Er)" in Figure 3, can be approximated as "Δx." This is because "Er" is typically less than 0.001, which is negligible compared to 1.

Typical configuration for making a transistor matching measurement

Figure 4 shows a typical configuration for making a transistor pair matching measurement. For the collector and emitter measurements, the same SMU is used. Two different SMUs are used for the base connections of Transistor 1 (Tr1) and Transistor 2 (Tr2). In this configuration, it is important to remember that either of the transistors can be turned on or off by applying the appropriate bias to the SMUs connected to the bases, and only one transistor at a time can be measured without changing the transistor connections.

Figure 4(a) illustrates the basic configuration where SMU1 measures the base parameters of Tr1 and SMU3 measures the base parameters of Tr2. This configuration presents a potential problem for Vbe measurement when the SMU measurement accuracy specification is larger than the matching requirement. Figure 4(b) illustrates how this problem can be avoided by using one SMU for Vbe measurement.

In the alternative configuration illustrated in Figure 4(b), SMU1 measures both Tr1 and Tr2 by switching the DUT connection. (In this case, there is an expectation that no error is associated with the switching.) If error-free switching can be accomplished, this approach is correct. There are, however, several issues regarding the use of reed relays, which are described later in this application note.

Thermo Electro-motive-force (thermo-EMF)

Conventional reed relay switches, which are readily obtainable from a variety of sources, typically generate a thermo-EMF ranging from a few tens of micro-volts to a few hundreds of micro-volts after the relay activation current is turned on or off. This voltage drift, which can continue for several minutes before dying out, is usually not acceptable when making precision measurements such as those required for BJT matching characterization. An example of thermal-EMF generated by a reed relay is shown in Figure 5 on the following page.

The Agilent 4073A test system uses specially designed reed relays that almost completely eliminate the thermo-EMF problem. Figure 6 illustrates the dramatic improvement in voltage drift from the case shown in Figure 5. Figure 6 shows the output of the 4073A switching matrix immediately after the relays have been switched.

Managing the use of a reed relay switch

The relays used in the 4073A act as almost ideal switches. The reed relays used in semiconductor parameter analyzers and switching matrices, however, are not as close to the ideal case. The specifications of the parameter analyzer SMUs take the thermo-EMF effects into account so users do not have to worry about this effect for normal applications. However, when performing measurements for matching applications that require extremely high levels of accuracy beyond the normal specifications, the following guidelines can minimize or eliminate the thermo-EMF effects.

• Wait until the thermo-EMF has stabilized to its final value. To

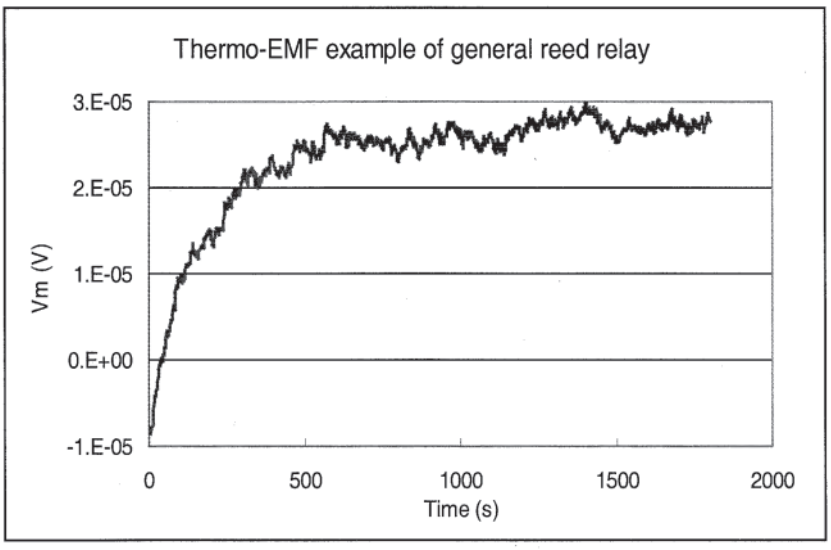

Figure 5. Thermal EMF of reed relay

accomplish this, make sure that the reed relay is set at the output of the SMU to its on (closed) state after the instrument has been turned on, and keep it closed between measurements. This is very important to remember when using the Agilent 4156C parameter analyzer.

• Complete the measurement as quickly as possible. If the measurement is completed within approximately 10 seconds, drift will be less than a few microvolts (as shown in Figure 5). This amount of drift will not affect measurement accuracy in most applications. When using the 4073A, however, there is no need to be concerned about making the measurement quickly to avoid drift, as illustrated by Figure 6.

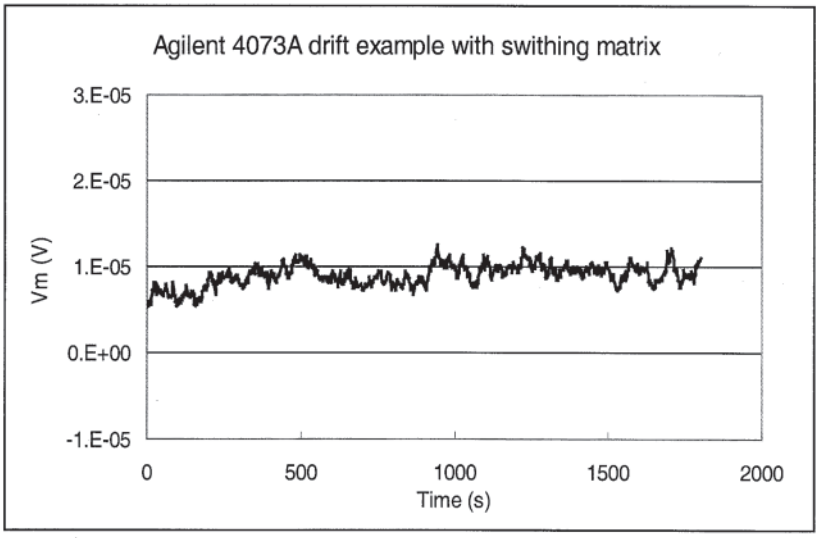

Figure 6. 4073A drift example characteristics including relays.

Technique for Making a BJT Matching Measurement

The general technique for making a transistor matching measurement is discussed in the following section.

Configuration example for a BJT matching measurement

Figure 7 shows a setup example for a BJT matching pair measurement (basically the same configuration illustrated in Figure 4(a) on page 5).

The SMU attached to the transistor emitters (SMU4) can be either a voltage source or a current source, depending on the measurement needs. For example, if a constant collector current (Ic) is required, then obviously SMU4 must be set to be a current source. On the other hand, if the measurement requirement is for a fixed base-emitter voltage (Vbe), then SMU4 must be set to be a voltage source. If the matching requirement for Vbe exceeds the SMU specifications, however, then there is a problem. In this case a special calibration technique described later in this application note must be utilized.

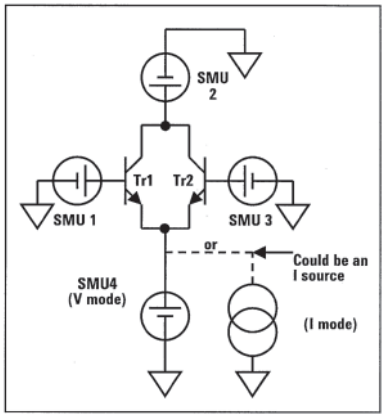

Figure 7. Basic setup for typical transistor matching

Figure 8 illustrates how Tr1 or Tr2 are selected in this measurement setup. The configuration for a Tr1 parameter measurement is shown in Figure 8(a). Here SMU1 is set to zero volts and

SMU3 is set to "–Vbe." Since SMU4 is also set to "–Vbe," the base-emitter voltage on Tr2 is zero and Tr2 is shut off. A positive base-emitter voltage of "Vbe" on Tr1 turns this device on. Exchanging the set values of SMU1 and SMU3 reverses the previous situation, turning off Tr1 and turning on Tr2. This case is shown in Figure 8(b).

The issue with this measurement procedure is that it does not satisfy the Vbe matching requirement of 26 μV. A special calibration technique that satisfies the 26 μV matching requirement is discussed later in this section.

Technique for Making a MOSFET Matching Measurement

The basic behavior of a MOSFET device can be described by an expression involving only Id and Vg. The major differences between a BJT matching measurement and a MOSFET matching measurement are that MOSFET gate current is insignificant, and MOSFET gate voltage sensitivity is relatively low compared to that of a BJT.

Figure 9 illustrates the two possible types of measurement setup for MOSFET matching characterization.

As shown in Figure 9(a), a MOSFET matching measurement can use the same measurement configuration as a BJT matching measurement. However, the measurement is easier to make in the case of a MOSFET matching characterization since the required voltage resolution is typically greater than 100 μV, as opposed to 26 μVf or the BJT case. This means that high-performance test equipment, such as the 4156C and 4073A, can be used without any special calibration techniques. *Note: The process to turn the two MOSFET transistors on and off is analogous to the BJT case and, therefore, it is not discussed here.*

A configuration that is specifically suited for making a MOSFET matching measurement is shown in Figure 9(b). Because making a MOSFET matching measurement does not require a gate current comparison and because the gate current itself is small compared to the drain current, one of the transistors can be turned on and off by setting the drain SMU to zero force current mode.

Figure 10 on the following page shows the details of the MOSFET switching operation for the case shown in Figure 9(b). Figure 10(a) shows that the case where the SMU connected to the drain of Tr1 is ON, and the SMU connected to the drain of Tr2 is OFF.

Figure 10(b) shows the case where the status of these two SMUs is reversed, so Tr1 is OFF and Tr2 is ON. This configuration uses the same SMU for both transistor gates and the same SMU for both transistor sources. Since these same SMUs are used in both transistors when they are in the ON state, it is possible to measure the difference of the gate voltages and source currents (which are approximately equal to the drain currents if the substrate current is negligible) with a high degree of accuracy. This is true because any SMU-to-SMU measurement variation is eliminated.

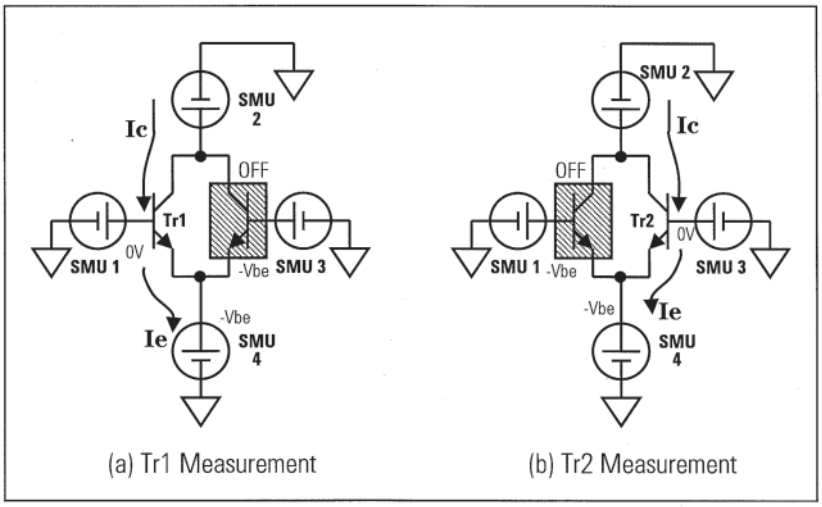

Figure 8. Tr1 and Tr2 selection for matching measurement

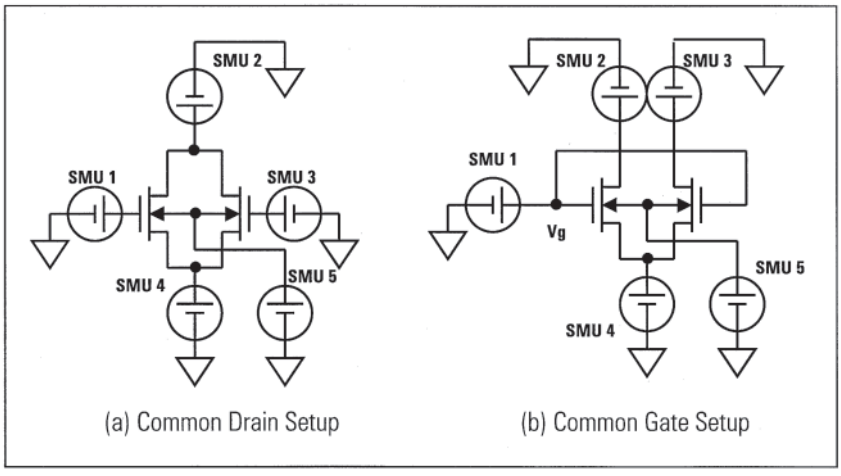

Figure 9. MOSFET matching measurement setup

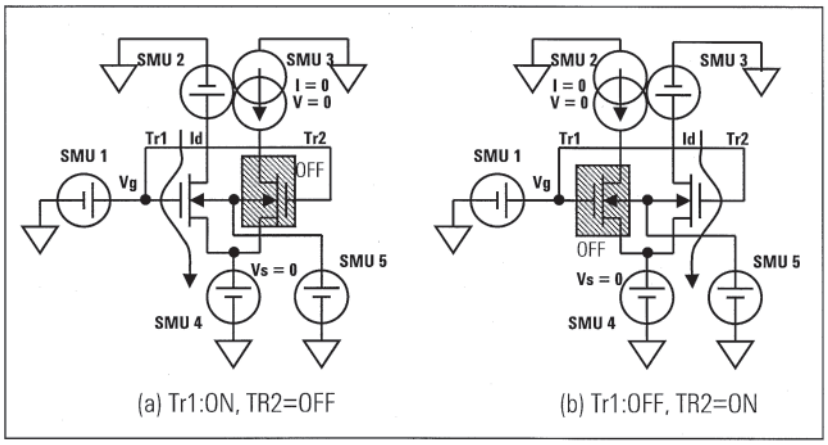

Figure 10. MOSFET matching measurement for Tr1 and Tr2

Technique for Resistor Matching Measurement

A resistor can be measured accurately in two ways: using the Kelvin (or 4-terminal) measurement method with a precision resistance meter, or using SMUs and VMUs as shown in Figure 11. To obtain a successful resistance measurement, two things are important: 1. elimination of the Joule self-heating effect, which will increase the temperature of the device; and, 2. measuring twice, which requires applying current in both directions by switching the polarity of the force current (I_F). By measuring twice, you can take the average of the two resistances to cancel the offset voltage of the VMU (or voltage sense) and the thermo-EMF of the connection terminal. The easiest way to measure resistors is by using the SMU/VMU method, because the current (effectively the power) applied to the resistor can be controlled.

Note: For details on the technique for measuring resistance, refer to Agilent Application Note 4156-11 "Precision Measurement of Metal Line Width in Sub-quarter Micron Interconnect Systems" (Publication number 5988-2695EN).

Pair resistor matching measurement technique

Verifying the alignment of a stepper is an important application of pair resistance measurement. By measuring the line resistance of two identical elements that are laid out orthogonally, information regarding the alignment of the stepper can be obtained. In the example of pair resistance measurement shown in Figure 12, the measurement setup uses two SMUs and one VMU, with the SMU being used in the current force mode. The measurement is done twice: first with connection A, and then switched to connection B. The difference between the two resistance measurements can be obtained by using the VMU readings as shown in Equation 6.

Equation 6

$$\Delta R = \frac{(VMU\_B - VMU\_A)}{(2 \times I)}$$

where,
ΔR is difference of pair resistor,
VMU_A is VMU reading at connection A setting,
VMU_B is VMU reading at connection B setting, and
I is force current of SMUs.

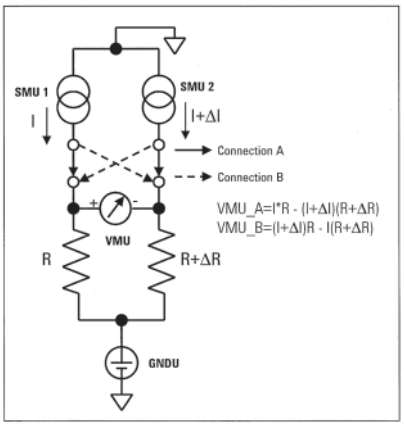

Figure 12. Resistor matching measurement example

Equation 6 is not affected by any thermo-EMF effect associated with the SMU connection changes, and it shows that a small difference in matched resistance can be obtained with a simple configuration. Two SMUs are used in current force mode and the themo-EMF relating to switching the connection to A and B does not affect the measurement result. A small difference ΔI is also cancelled and it does not appear as a source of error.

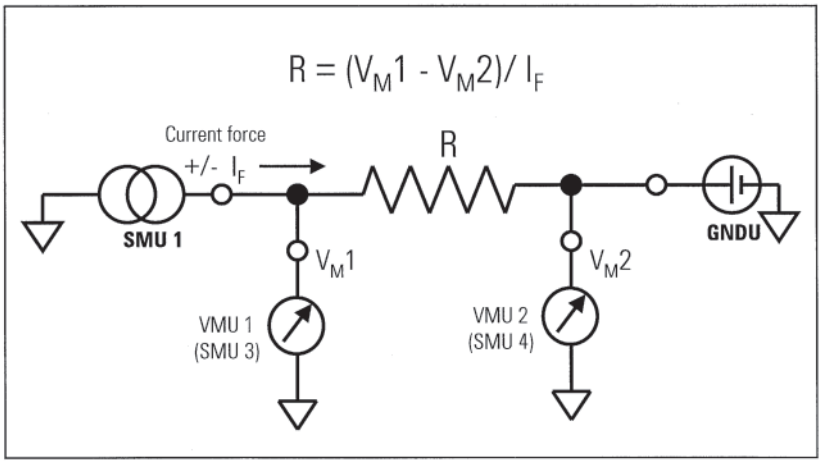

Figure 11. Kelvin resistance measurement

Summary of Required Accuracy versus Agilent Instrumentation Equipment Performance

The accuracy requirements for matching measurements that

Devise	Parameter	Required Accuracy
BJT	Ic, Ib	0.10%
	Vb	26μV
MOSFET	Id	0.10%
	Vg	100μV
Resistor	V	10μV

Figure 13. Required accuracy for 0.1% matching measurement

	4156C		4142B		4072A	4073A	
	SMU	VMU	SMU	VMU	SMU with Matrix	SMU with Matrix	DVM with Matrix
Current % error * offset/reading	0.02%/0.04%	--	0.1%/0.2%	--	0.05%/0.1%	0.04%/0.06%	--
Voltage error offset/resolution	200μV/2μV	10μV/0.2μV	1mV/40μV	400μV/4μV	800μV/2uV	500μV/2uV	100μV/0.1μV

* specification on 1mA range

Figure 14: Agilent test equipment performance

have been discussed thus far are summarized in Figure 13. The corresponding specifications for Agilent test instruments and systems are shown in Figure 14.

Conformation of current measurement accuracy

Figure 15 plots current measurement accuracy versus the relative percentage reading (relative to the full-scale ranges of the 4156C and 4073A) for sample 4156C and 4073A measurements made in the 1 mA range. As this data shows, measurement error increases several-fold as the measurement point moves from full scale (100%) to one-tenth of the full scale (10%). Figure 15 illustrates the need to take the following two steps for optimal matching characterization: 1. set the measurement current close to the maximum value allowable for a given measurement range (at least 50% above maximum allowable value); and 2. do not allow the measurement current to get so close to the maximum value of the measurement range that a range change occurs. Once a current range change occurs, the measurement is taken at close to one-tenth of full scale, and the consistency of the data is lost. Figure 15 also shows that the Agilent 4156C parameter analyzer and 4073A parametric test system both satisfy the 0.1% accuracy requirement without using any special techniques when measurements are taken close to the maximum value of the selected measurement range.

Conformation of voltage measurement accuracy

When measuring current, the scale is arranged logarithmically and that portion of the measurement range between 10% and 100% of the full range value can be utilized. When measuring voltage, however, both stability in the full measurement range and the fine resolution specified in Figure 13 are required. Unfortunately, the offset voltage specifications of all SMU types shown in Figure 14 exceed the maximum requirements shown in Figure 13. However, because the resolution of all of the equipment shown in Figure 14 exceeds the accuracy requirement specified in Figure 13, special measurement techniques can be used to meet the accuracy requirements. It is important to note that the VMU of the 4156C satisfies the voltage accuracy requirements without any special measurement techniques, so it can be used to calibrate the offset voltage of the SMUs.

Figure 13 shows that BJT matching measurements require the highest degree of voltage measurement accuracy (26 μV), so special attention is needed in order to make this measurement. The offset voltage of the SMUs must be calibrated and stable for the duration of the matching measurement. The voltage applied in these instances is typically one volt or less. Therefore, required stability is about 5 digits or 10 ppm (parts per million) of full scale range (i.e., 20 μV for a 2 V range).

The stability of the key components used in the SMU circuitry that determine accuracy typically varies about 10 ppm per degree Celsius. Thus, if the ambient temperature does not vary more than approximately 1 degree Celsius during the measurement, the accuracy during the measurement can be expected to be approximately 10 ppm in many cases. Figure 16 on the following page shows sample stability data for 0 V and 1 V output measurements in the 2 V range of the 4156C SMU over a 1,000-second interval. Both measurements in this example exhibit drift that is within a range of 10 μV. *Note: This performance is not guaranteed but, rather, indicates typical performance provided by these types of instruments.*

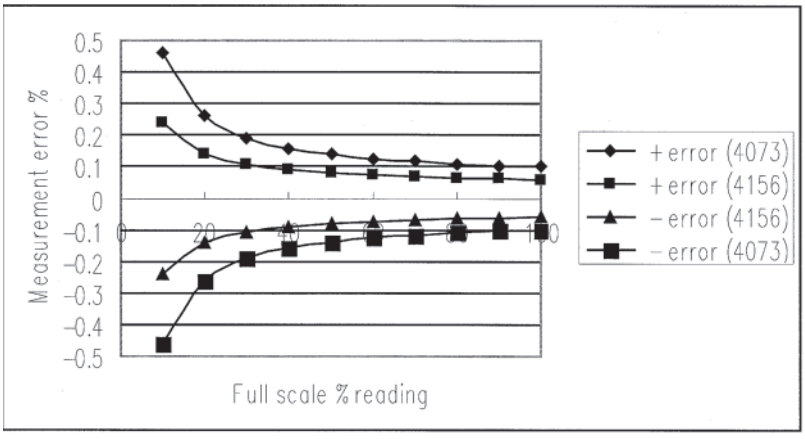

Figure 15: 4056C and 4073A measurement accuracy for 1 mA current range

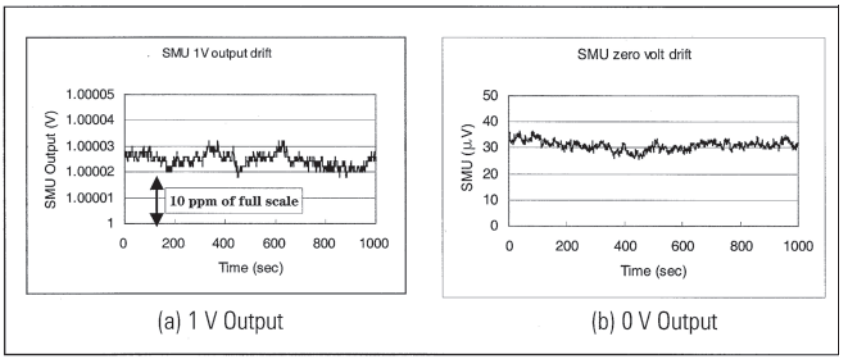

Figure 16. SMU output voltage drift over 1,000 seconds

When the measurements shown in Figure 16 were taken, the room temperature drift was within 0.3 degrees. While drift characteristics differ from instrument to instrument, the data in Figure 16 reflects measurement performance in this particular case under operating conditions and enables the user to decide upon a measurement strategy. Keeping the ambient temperature constant during measurement is a key environmental consideration when attempting a measurement that exceeds the general specification limit of the instrument.

The basic approach for making measurements out of the general specification limits is to calibrate the measurement resource for the desired measurement performance on a short-term basis. In the case of offset voltage cancellation, it simply involves subtracting an offset voltage from the measurement reading, then the accuracy of this correction can be improved by stabilizing the measurement condition. Two methods for calibrating the zero offset voltage when measuring Vbe for transistor matching are shown in Figures 17 and 18. The approach shown in Figure 17 is most useful when the readable resolution of the SMU exceeds the required resolution. If the readable resolution of the SMU is not fine enough but that of the VMU is, then the approach shown in Figure 18 is the better choice. For example, the SMU resolution of the 4142B is not fine enough (as shown in Figure 14 on the preceding page), but the 4142B SMU can be utilized for BJT and resistor matching measurements using the approach shown in Figure 18.

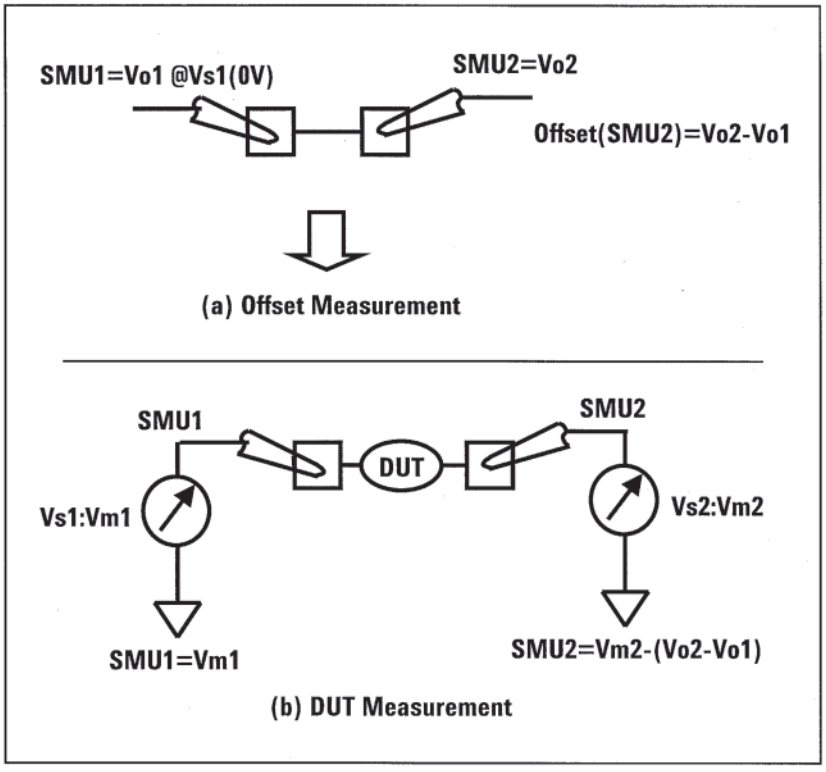

Figure 17. Offset voltage zero calibration with SMUs

Tips for Effective Matching Characterization

Instrument

• Keep the DUT temperature constant. The pn junction voltage drift is about 2 mV per degree, so the device temperature must be kept within a 0.013-degree range to maintain a 26 μV stability level (26 μV ÷ 2 mV ÷ degree = 0.013 degree). It also important to physically enclose the wafer chuck on the prober in order to isolate it from the flow of air in the room. This is true even though the room temperature can drift much more than the 0.013-degree limit, since the thermal capacitance of the wafer chuck slows down the effects of room temperature drift.

• Warm up the instrument long enough to stabilize the internal temperature and minimize the drift component.

• Keep the room temperature constant in order to eliminate DUT and instrument drift.

• Set the auto calibration mode to OFF after the instrument and room temperature have stabilized. Since the auto calibration function resets the previous calibration condition, auto calibration will create measurement discrepancies even when repeating the measurement on the same DUT. The purpose of the matching ap-

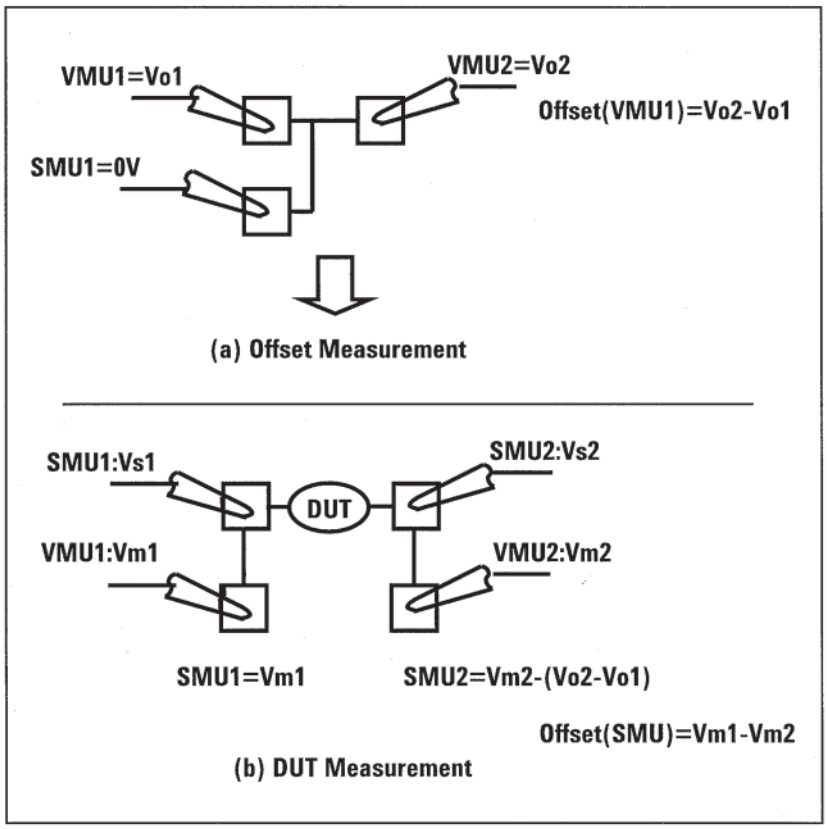

Figure 18. Offset voltage zero calibration with SMUs & VMUs

plication is to detect small differences, so it is better to have the auto calibration off once the initial calibration has been made and the instrument reaches a stable condition.

• Determine the offset stability characteristics versus test environment changes (e.g., the effect of a change in room temperature or the use of auto calibration). By understanding the relationship of offset stability to these factors, you can greatly improve your matching characterization results.

• Avoid performing a current or voltage measurement near a range changing point. If a change in range occurs during a matching measurement, it may result in data discontinuities as shown in Figure 15.

• Use a long integration time for low voltage and low current measurements in order to minimize the noise component and obtain a stable measurement.

• Set a wait time greater than zero to stabilize the device before measurement. This enables the DUT to reach thermal equilibrium before the first measurement is taken. In particular, if the first measurement point always appears not to conform to the rest of the measurement data, then there may be a thermal stability problem.

Connection

• Always keep the SMU output switch set to ON. Switching the output switch from ON to OFF will cause a small output voltage drift in the SMU after a period of time. Keeping the SMU output switch set to ON allows the relay to stabilize after it warms up, thereby minimizing the EMF drift component. Any external offset calibration should be performed only after the SMU output switch has stabilized.

Wafer Chuck

• Physically enclose the wafer chuck in order to isolate it from outside electrical noise and changes in temperature.

• Power off the thermo chuck if the wafer prober has one. A thermal chuck will constantly turn on and off, even after its temperature has stabilized, and this is a major source of noise. An air-isolated wafer chuck under stable room temperature conditions provides the best platform on which to make matching characterization measurements.

Conclusion

Matching characterization measurements require special techniques for both test structure design and measurement execution. This application note describes best practices that are useful for making matching measurements using the Agilent 4073A Ultra Advanced Parametric Test System and the Agilent 4156C Precision Semiconductor Parameter Analyzer beyond both of their general specification limits.

All Agilent SMUs can be used for matching applications utilizing the techniques discussed in this application note. However, the 4073A and 4156C are the best choices for making measurements of this type. The 4073A and 4156C solve many of the issues discussed in this application note without the need for any special measurement techniques, which is always the most desirable situation.

The 4073A is easily integrated with a fully automatic wafer prober. This test system/prober combination is best suited for the high-throughput and high-volume evaluation of matching characteristics across wafers and wafer lots. Moreover, the

near-ideal behavior of the 4073A relays eliminates the need to compromise measurement configurations.

The 4156C is best used with a manual or semi-automatic wafer prober. The extremely accurate SMUs and VMUs of the 4156C combine well with the measurement techniques described in this application note to enable you to obtain highly reliable matching characterization measurements.

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