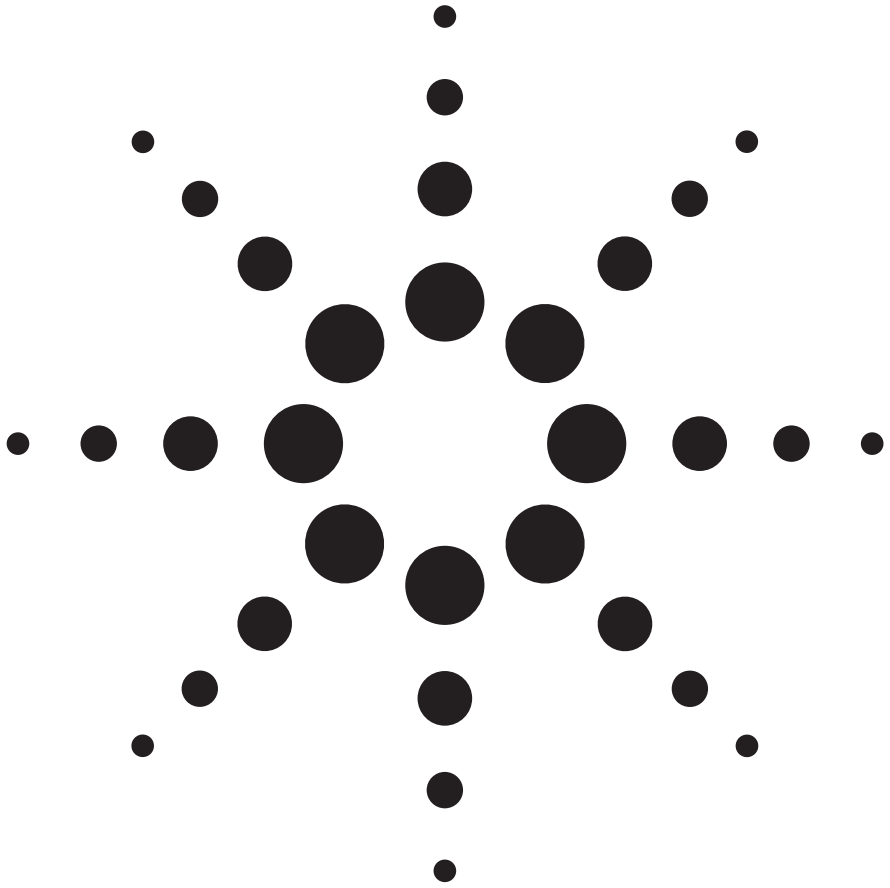
RF Probing Diode Wafers

White Paper



By Scott Wartenberg and Chris Mohr
Agilent Technologies
Semiconductor Products Group

Reprinted from the March 2001 issue of "Microwaves & RF," with the permission of Penton Media, Inc.

Agilent Technologies

Abstract

RF-measuring non-planar diodes can be a challenge. Such devices have the signal pad on top and the ground contact on bottom of the die. RF co-planar waveguide (CPW) probes require both signal and ground pads on the same surface. Rather than mounting the die in a test fixture, RF probing of non-planar diodes with co-planar probes is possible with this technique. Probing with CPW probes allows all the advantages of conventional RF on-wafer characterization. It provides faster design turnaround time and enhances model accuracy.

Introduction

Non-planar semiconductor devices pose a physical problem to RF measurements. Examples of non-planar devices are discrete Schottky and PIN diodes. These devices have the signal pad on top and the ground contact on the bottom of the die. This makes RF probing difficult. Figure 1 shows a diode wafer. IC processing requires the cathode on the top and the anode on the bottom. Mounting a single die to a connectorized carrier is the common solution. Compared to on-wafer testing, carrier parasitics cloud the RF results. In traditional on-wafer RF probing, the probes contact either the top or the bottom surface. How to measure a non-planar device using horizontal probes then becomes the task.

This technique permits RF on-wafer probing of non-planar structures using co-planar RF probes. Section II describes the unique test system. Displayed in Section III are the measured results. At the end, the Summary discusses future improvements.

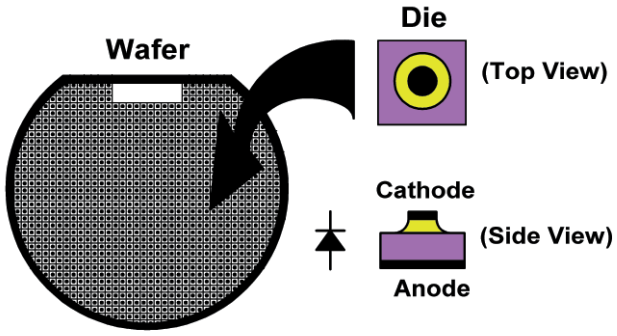


Figure 1. A typical diode wafer showing the vertical nature of the die.

System Description

The new test system centers on an Electroglas probe station (see Figure 2). Two areas, grounding and calibration, are essential to the system's operation. A key concept is ground isolation. Figure 3 shows a co-planar waveguide (CPW) probe making contact to two diode dice. These diodes are side-by-side on the wafer surface, aligning with the probe pitch. The ground probe contacts one diode and the signal probe contacts the diode-under-test (DUT). Both the signal and the ground probes are DC-isolated from lab ground. In the RF path are two connectorized DC blocking capacitors. One blocks DC from the Vector Network Analyzer (VNA) signal path and the other from the VNA ground path. This arrangement permits independent biasing of the signal and ground probes. Define the voltage on the signal probe V_s and the voltage on the ground probe V_g (see Figure 3). Both power supplies connect to a bias tee mounted in-line between the blocking capacitors and the DUT. Supplied to the chuck is a third bias, V_{ch}. Applying a chuck potential keeps leakage current from flowing to the wafer backside. The chuck itself is both DC- and AC-isolated from the lab ground. Force and sense lines run to opposite sides of the chuck. HP 4142B programmable power supplies provide three biases. Plugging equipment into isolation transformers rather than the wall outlet further isolates them from all grounds. The GP-IB control bus to each instrument connects through opto-isolators. Without the opto-isolators, ground sneaks in through the GP-IB bus. The net result of all this is full DC ground isolation to the DUT. The AC ground arrives to the DUT through a single path, the RF cable shield.

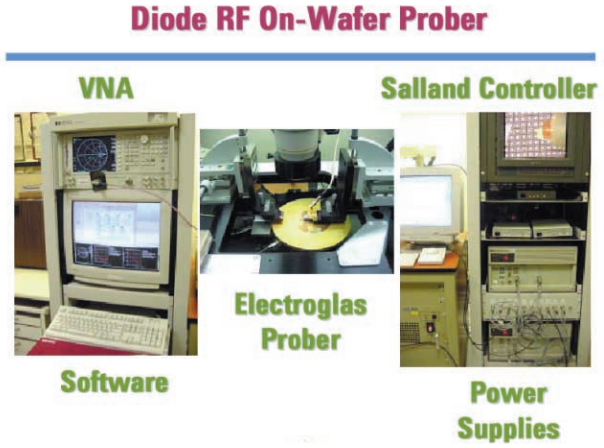


Figure 2. RF probe system to test PIN and Schottky diodes on-wafer.

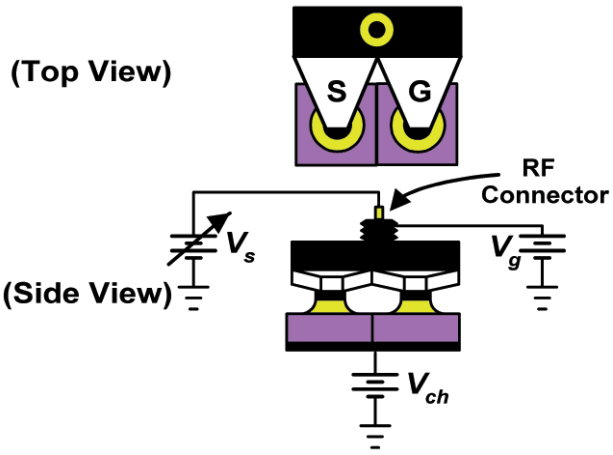


Figure 3. Voltage assignments for biasing through the co-planar probes.

Calibration de-embeds the blocking capacitors, bias tee and other system effects. An alumina substrate contains precision impedance standards for on-wafer calibration. Schottky diodes require low capacitance testing. Parasitic capacitance associated with the gold contact pads swamp the diode's junction capacitance. To quantify the parasitic capacitance, fabricate a dummy wafer with the same pitch and pads as the DUT wafer. This dummy wafer contains contact pads and no active devices underneath. Measuring it reveals the pad capacitance and any residual chuck capacitance. Isolating ground from the system lowers the parasitic capacitance of the system.

Another key concept is de-embedding. De-embedding the ground diode from the measurement should yield the DUT. Because the diodes are adjacent on the wafer assumes they are nearly similar. Biasing identically should give two diodes with nearly the same characteristics. Another way is to fully forward-bias the ground diode. This creates a small resistance from the ground probe to the backside of the wafer. De-embedding the S-parameters shifts the reference plane from the ground probe to the back of the wafer. Since the two diodes are biased independently, locating a problem with either diode becomes simpler. A virtual ground to the wafer backside along with ground isolation enables RF probing of non-planar devices.

Measured Results

Carrier lifetime τ and series resistance R_s are two diode figures of merit. High-volume production requires these be automatically tested on each wafer. Assembling an RF on-wafer test system to the above specifications met this need. Use Caverly's method[1,2] to calculate τ and R_s with S-parameters. A software routine written in IC-CAP, Agilent's device characterization program, enabled quick calculation of τ and R_s.

Calibrating the DC path is straightforward. Measuring a precision resistor with the CPW probes determines the cable voltage drop. Precision resistors and other standards are found on Cascade Microtech's impedance standard substrate (ISS). Also use it to calibrate the RF path. This sets the reference plane at the co-planar probes. Moving the ground reference plane to the back of the wafer is the next step. Fully biasing both diodes results in a small resistance and reactance between the signal and ground probes. Model the DUT as two identical diodes connected anode to anode. Half the behavior approximately equals one diode. De-embedding half from the total measurement gives the DUT. With the ground diode at a fixed bias point, the DUT diode can be characterized at any bias. Figure 4 shows a high-frequency wafer maps of R_s. These values fell within 15% of those measured using conventional time-domain techniques[3].

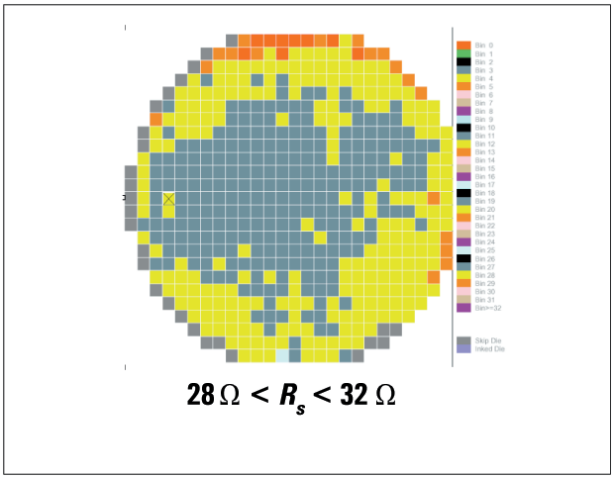


Figure 4. Wafer map of the PIN diode series resistance R_s.

Summary

This paper outlines a new system to RF test non-planar diodes on-wafer. The next phase of system development requires measurement of Schottky diodes. These have small junction capacitances. To accurately and repeatably measure will involve de-embedding the system capacitance down to the fempto-Farad level.

Acknowledgements

The authors thank Domingo Figueredo, Steve Randle, Alan Rixon and Ray Waugh of Agilent Technologies' Wireless Semiconductor Division, Newark, CA for their unwavering support.

References

1. Robert Caverly, "RF Technique for Determining Ambipolar Carrier Lifetime in PIN RF Switching Diodes," *Electronics Letters*, Vol. 34, No. 23, 12th Nov. 1998, pp. 2277-2278.

2. Robert H. Caverly and Gerald Miller, "The Small Signal A.C. Impedance of Gallium Arsenide and Silicon P-I-N Diodes," *Solid-State Electronics*, Vol. 33, No. 10, Oct. 1990, pp. 1255-1263.

3. Mohamed Derdouri, Philippe Leturcq, and Antonio Munoz_Yague, "A Comparative Study of Methods of Measuring Carrier Lifetime in P-I-N Devices," *IEEE Transactions on Electron Devices*, Vol. 27, No. 11, Nov. 1980, pp. 2097-2101.

www.agilent.com/semiconductors

For product information and a complete list of distributors, please go to our web site.

For technical assistance call:
Americas/Canada: +1 (800) 235-0312 or (408) 654-8675

Europe: +49 (0) 6441 92460

China: 10800 650 0017

Hong Kong: (+65) 271 2451

India, Australia, New Zealand: (+65) 271 2394

Japan: (+81 3) 3335-8152(Domestic/International), or 0120-61-1280(Domestic Only)

Korea: (+65) 271 2194

Malaysia, Singapore: (+65) 271 2054

Taiwan: (+65) 271 2654

Data subject to change.

Obsoletes 5988-2960EN
November 5, 2001
5988-4280EN

Agilent Technologies