Testing 10 Gb/s SONET/SDH equipment and components

71612C 12.5 Gb/s error performance analyzer

Product Note

Agilent Technologies

Contents

Introduction

This document describes key features of the 71612C 12.5 Gb/s error performance analyzer that are particularly beneficial in the development and production testing of components and sub-systems for SONET/SDH transmission equipment. The creation and real-time editing of custom patterns up to 8 Mbits in length using the 71612C analyzer's pattern editor are described. The examples shown are SONET patterns, however the techniques and measurements described are equally applicable to SDH systems.

Potential applications for the 71612C analyzer in SONET/SDH component and system test are identified.

An error location analysis option is available on the 71612C analyzer; this document shows how this may be used to measure the bit error ratio (BER) of a selected block of bits and any specific bit in the pattern being generated. Then, it describes how the 71612C analyzer can assist in the identification of systematic errors by indicating the position of each errored bit in turn and automatically measuring the BER of each errored bit.

A demonstration disk, supplied with the 71612C analyzer, contains some of the patterns described in this document together with other useful patterns.

The serial BERT in the synchronous era

Although telecommunications has moved into the SONET/SDH era with its layered or structured signal architecture, the bit error ratio test set (BERT) consisting of a serial pattern generator and error analyzer remains an essential tool in the R&D of communication systems, high-speed integrated circuits (ICs) and photonic components. A fundamental reason for this is the requirement to compare the theoretical and relative performance of systems and components using a pseudo-random binary sequence (PRBS). The PRBS is a suitable repetitive test signal that resembles a random signal, occurs in a mathematically predictable sequence and is easily generated by a shift register. This allows comparison of bits transmitted from the BERT pattern generator with those received by the error analyzer at the output of the device under test.

In addition to a range of industry standard PRBS patterns up to $2^{31} - 1$ bits in length, the 71612C analyzer has over 8 Mbits (2^{23}) of user-programmable pattern memory that allow the creation of complex custom test patterns for testing SONET/SDH systems and components. A pattern containing up to six identical or different STS-192/STM-64 frames may be constructed, thus allowing functional (pseudo-dynamic) and alarm testing to be carried out. The user-programmable memory also allows framed and unframed patterns to be constructed that stress timing recovery circuits, lightwave transmitters and receivers or, for example, induce baseline wander for margin testing.

Typical applications

Although the emphasis of this document is on the construction of complex custom patterns compatible with SONET/SDH operational equipment, the list below shows some of the tests routinely carried out on the constituent components of such equipment.

- Pattern dependency testing (eg, ITU-T CID test).
- Mean launch power (PRBS).
- Eye diagram and mask analysis (PRBS).
- Receiver sensitivity, eye contour measurements (PRBS).
- Dynamic baseline wander testing (alternate programmable word).
- Clock recovery circuit stress test (PRBS, variable mark and transition density).
- Regenerator test (PRBS).
- IC tests (PRBS and word).

SONET/SDH signals contain regions within the data stream where the possibility of bit errors occurring is greater because of the sequence of data in these regions. This may be caused by eye closure resulting from dc wander; ac coupling causing the mean level of the signal within the equipment to vary with pattern density; or failure of the timing recovery circuit to bridge regions of data that contain little timing information in the form of transitions. The ITU-T have defined a test pattern to verify the adequacy of timing recovery and low frequency performance of STM-n equipment. This consists of a user-programmable pattern comprising consecutive blocks of data as follows: The first row of section overhead bytes for the STM-n system under test, all ones (zero timing content, high average signal amplitude), pseudo-random data with 50% mark-density ratio, and then a repeat of the overhead bytes, all zeros (zero timing content, low average signal amplitude) and the PRBS. For full details see ITU-T Recommendation G.958. The pattern is referred to as a consecutive identical digit (CID) test pattern and is simply constructed with the 71612C analyzer's pattern editor.

Alternating long patterns that induce a known amount of baseline wander for noise margin testing of decision circuits and regenerators may also be programmed and generated with the 71612C analyzer. In the alternate pattern mode of operation it is possible to switch synchronously between two different programmable patterns each of which may be up to 4 Mbits in length.

Many SONET/SDH sub-systems and components are tested with PRBS patterns, however, to fully test a clock recovery IC requires the construction of variable transition ratio patterns with strong sub-harmonic content (for example, a repeating 11110000 pattern has a 25% transition density).

Creation and real-time editing of custom patterns

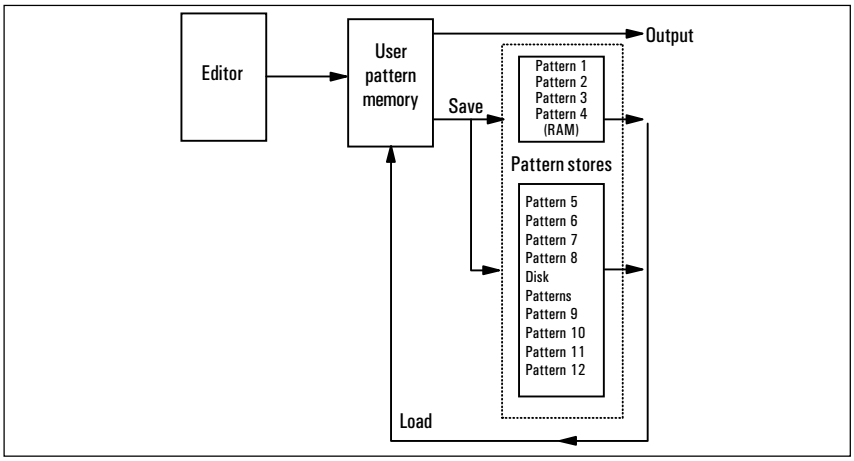

Figure 1. 71612C analyzer's pattern editor

Figure 1 shows the relationship between the three main functional blocks of the pattern editor: the editor, pattern stores and user pattern memory from which the instrument outputs a user pattern. The editor always edits the contents of the user pattern memory. To edit one of the twelve patterns from the pattern stores, the contents of the pattern store must first be loaded into the user pattern memory. It may then be edited and re-saved back to the pattern store.

The pattern editor supports the following operations:

- The contents of one of twelve pattern stores can be loaded into pattern memory, edited, saved and transmitted.
- Loading and editing of multiple copies of one of four fixed PRBS-based patterns in standard, zero substitution, or variable mark density options (2^7, 2^{10}, 2^{11} and 2^{13}).
- Copying of multiple copies of a pattern from one pattern store into a pattern at a precise point in the user pattern memory.
- Edit and display patterns in hexadecimal or binary notation.
- Saving of a marked block of bits within the user pattern memory to an internal or disk pattern store; the deletion of a marked block of bits.

Pattern stores

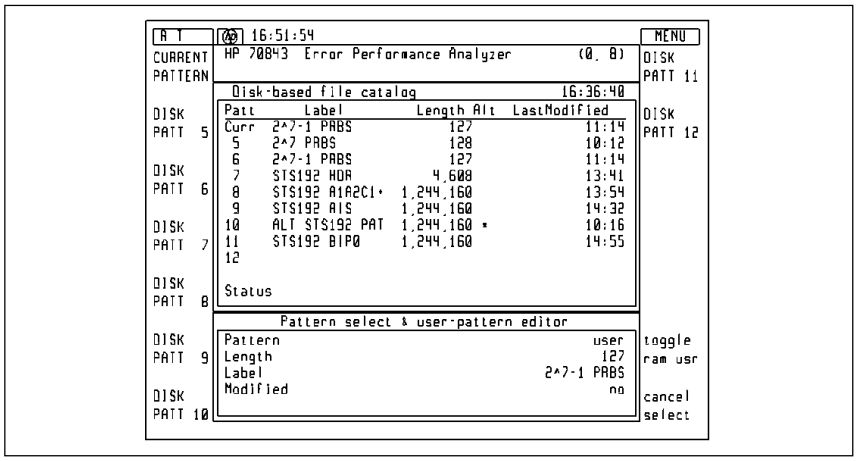

Figure 2. Contents of pattern stores

There are twelve pattern stores as follows:

- Pattern stores 1 to 4 can hold patterns up to 8 kbits in size (non-volatile RAM).
- Pattern stores 5 to 12 are held on the MS-DOS compatible floppy disk and can accommodate patterns of up to 8 Mbits in length in separate files on the disk.
- The pattern currently stored in user pattern memory is accessed with the <CURRENT PATTERN> softkey. This is the pattern that is generated when the user selects a user pattern as the active output pattern.

When a user wishes to select a pattern store, a display similar to that shown in figure 2 is shown on the screen. The information shown for patterns 5 to 12 details the patterns stored on the currently accessible disk which in the example shown includes patterns described in the next section. Any one of the twelve user patterns may be recalled and edited either while a pattern other than a user pattern is being output, or when the pattern to be edited is the active pattern currently being output. In the latter case, real-time editing is possible.

Setting up and editing an STS-192 SONET-compatible pattern

The user creates a pattern by editing the contents of one of the pattern stores. As an example let us construct a 1,244,160 bit pattern for STS-192 applications with valid A1, A2 framing bytes, C1 bytes, and B1 and B2 section and line error monitoring bytes. The B1 and B2 bytes provide error monitoring by means of a bit-interleaved parity 8 code (BIP-8).

It is convenient to create this pattern on a blank high capacity disk that has been formatted in the 71612C analyzer's disk drive.

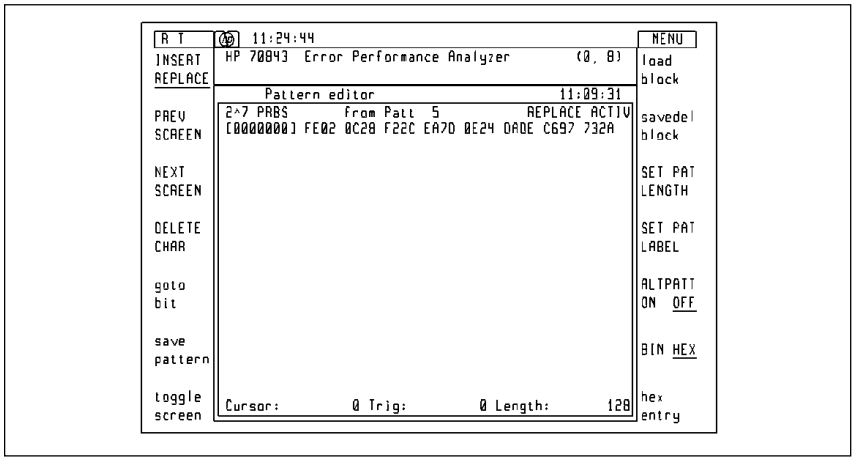

Figure 3. 2^7 PRBS in pattern store 5

The 'payload' in the STS-192 frame will consist of the recommended $2^7 - 1$ scrambling sequence that starts with the 1111111 sequence. To load multiple copies of this pattern into the STS-192 frame, the $2^7 - 1$ sequence must be stored in one of the pattern stores. The architecture of the pattern generator memory determines the length of the PRBS-based patterns that can be loaded into a user pattern by means of the <LOAD BLOCK> feature. This includes a 2^7 pattern but not the required $2^7 - 1$ pattern. This is only a minor inconvenience; we select (for example) disk pattern store 5 for editing, set the pattern length to 128 and <LOAD BLOCK> of 2^7. The pattern on screen will be FE02 0C28 F22C EA7D 0E24DADE C697 732A (figure 3).

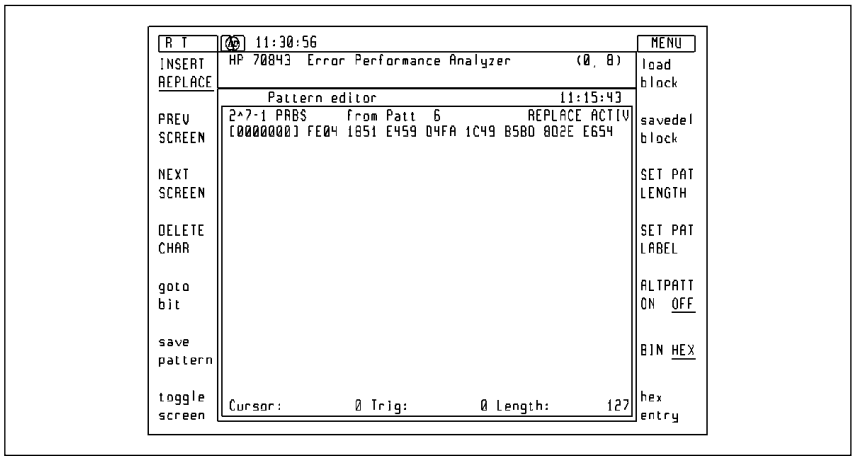

Figure 4. $2^7 - 1$ PRBS in pattern store 6

We change to binary display, delete bit 8, and set the pattern length to 127 bits. The sequence on screen is the correct SONET scrambling sequence FE04 1851 E459 D4FA 1C49 B5BD 8D2E E654. We save this to (for example) pattern store 6 for future use (figure 4).

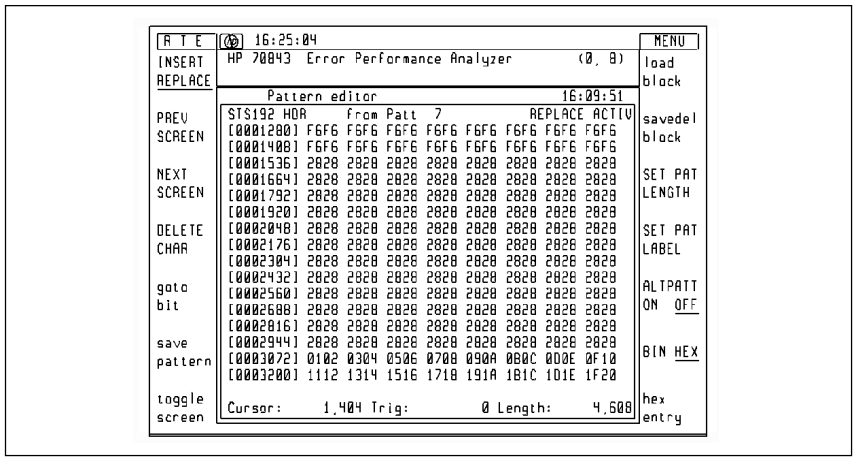

Figure 5. STS-192 header (A1, A2 and C1 bytes)

We now set the pattern length to 4608 to programme three of the section overhead bytes for each STS-1 in the STS-192 frame. We go to bit 0, enter 11110110 (A1 byte), and save this byte with the <SAVE BLOCK> function to one of the internal pattern stores. We move the cursor back to bit 0 and use the <LOAD BLOCK> function to load 192 copies of the A1 byte into the pattern being edited. We then perform a similar exercise to load 192 copies of the A2 byte (00101000) from bit number 1536. This completes the entry of the framing bytes for STS-192. The 192 C1 bytes are entered in hexadecimal starting with 01 and finishing with C0.

Figure 5 shows part of the A1 framing bytes (F6), the A2 framing bytes (28), and the start of the incrementing C1 bytes. The C1 byte is set to a binary number corresponding to its order of appearance in the byte-interleaved STS-n frame; it is provides in all STS-1s within a STS-n frame and the first STS-1 is allocated the number 1 (00000001) before scrambling.

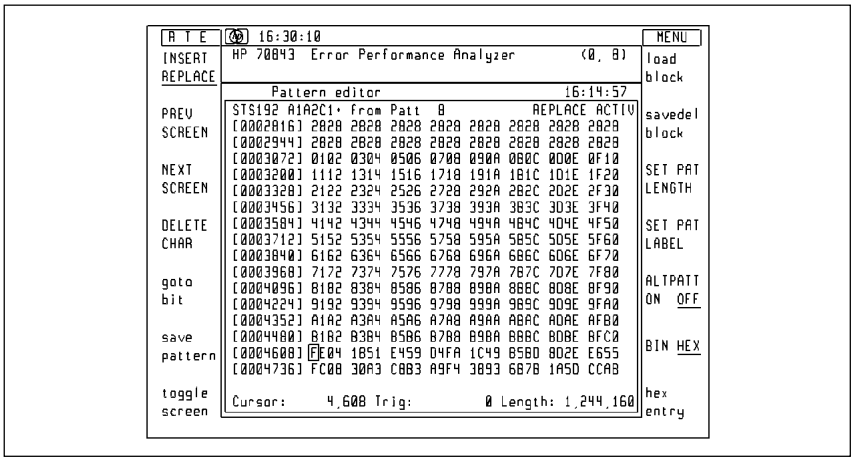

Figure 6. STS-192 basic framed pattern

To complete the construction of the pattern, the length is changed to 1,244,160 bits and the cursor is set to bit 4608. The <LOAD BLOCK> feature is used to copy 9761 repetitions of the $2^7 - 1$ PRBS from pattern store 6. This is equivalent to scrambling the all zeros pattern with the SONET scrambling PRBS. The pattern is saved to disk in, for example, pattern store 8 and is shown in figure 6 with the cursor at the start of the scrambling sequence at bit 4608.

This useful pattern may be edited and used to test SONET/SDH failure states and to simulate maintenance signals etc. To ensure compatibility with operational equipment there should be no parity errors detected by the terminal or equipment under test. SONET/ SDH performance monitoring at each level in the hierarchy is based on bit-interleaved-parity (BIP) checks calculated on a frame-by-frame basis. For example, the B1 byte provides section error monitoring, and in a STS-n the section BIP-8 is calculated over all bytes of the previous STS-n frame after scrambling and the computed value is placed in the B1 byte of STS-1 number 1 before scrambling.

This pattern may be simply edited to run error free with SONET/SDH systems and subsystems as follows:

- Leave the B1 and B2 bytes in the frame all zeros before scrambling.
- Compute the BIP-8 parity checksum for all the bytes in the frame.
- Choose a convenient byte in the frame, for example byte number 17282 which corresponds to the E1 byte of STS-1 number 2.
- EXOR the checksum byte with the current value in the chosen byte (17282).
- Overwrite the result of the EXOR calculation into the chosen byte by selecting the pattern editor <REPLACE> mode.
- The parity checksum should now be zero, and as this corresponds to the B1 byte value, the pattern will run with no parity errors on STS-192 equipment.

Note that the B2 byte remains zero because the H pointer bytes, the rest of the line overhead and the payload of the STS-1s are all zero before scrambling.

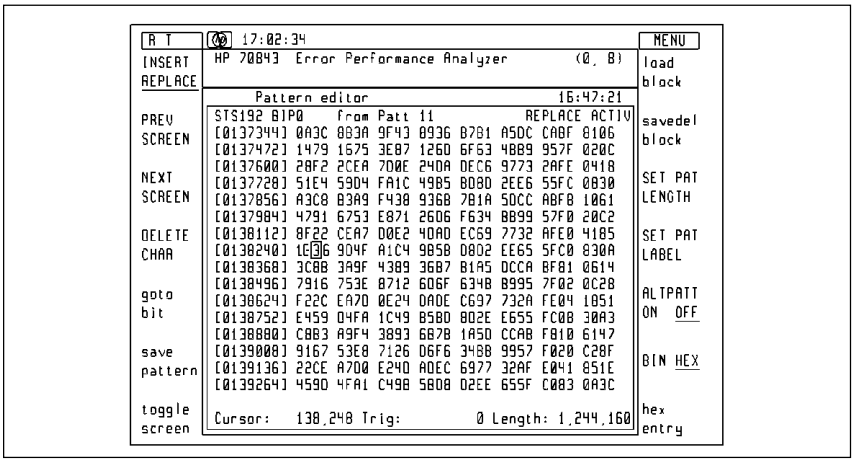

Figure 7. STS-192 frame with no parity errors

Figure 7 shows part of the STS-192 pattern described above with the cursor highlighting byte 17282 (bit 138,248) which has been overwritten with hexadecimal 36.

Pseudo-dynamic testing with alternating patterns

The 71612C analyzer can switch error free (hitlessly or synchronously) between two different user-programmable long patterns; these may be up to 4 Mbits long, but must be of identical length. Pattern selection is under the control of a front panel key, HP-IB or the auxiliary input port; changeover is synchronous with the end of a word. The length of the alternating patterns should be a multiple of 256 bits. The instrument will output one of two patterns (A or B) at the end of either pattern. The auxiliary input controls which pattern is output in one of two modes:

- Oneshot – a rising edge on the auxiliary input inserts a single version of pattern B into repetitions of pattern A.
- Alternate – the logic state of the signal at the auxiliary input determines which pattern is output. A logic 0 will output pattern A.

Note: The error detector is not affected by the pattern switching and is set to pattern A when alternate pattern is selected. In alternate pattern mode, a pattern trigger pulse output is provided; this occurs at bit 0 of the selected pattern.

The alternate pattern feature offers great potential for pseudo-dynamic testing of framing algorithms, failure states and alarms.

SONET/SDH systems test with user-programmable patterns

The framed pattern with no parity errors is suitable for jitter tolerance testing (with a suitable clock source) when the built-in parity error alarm of the LTE/STE is used to flag the onset of errors. The pattern has many additional uses as a basic framed STS-192 pattern. Real-time editing of this pattern may be used to confirm the operation of equipment parity error alarms.

The alternate pattern mode of pattern generation facilitates the construction of patterns that test failure states and algorithms.

- **Jitter testing with framed zero parity error pattern**
- **Failure states and maintenance signals**
  - **parity errors**
  - **loss of signal (LOS)**
  - **framing algorithm (LOF)(OOF)**
  - **alarm indicator signals (AIS)**
  - **loss of pointer (LOP)**
- **Block BER measurement**
  - **overhead bytes BER**
  - **payload BER**

Loss of signal (LOS) alarm may be tested by increasing the run of zeros in one pattern until the LOS state is entered; this should correspond to 100 ms or more of zeros (> 1,045,095 bits at STS-192). The LOS state should be exited after two valid frames are received. The LOS algorithm may be examined by alternating between a valid pattern and the pattern containing the run of zeros.

In SONET systems the out of frame (OOF) state is entered when four consecutive frames are received with errored framing patterns, and exited after two valid frames are received. The equipment loss of frame (LOF) signal is required to be activated by an STS-192 signal that is in the OOF state for 24 frames or more. The LOF alarm should therefore be activated after 28 or more consecutive frames have been received with errored framing patterns, and the equipment should frame-up after two valid frames are received. The operation of the alarms may be tested by using alternating patterns containing errored and valid framing bytes.

A single pattern to stress test the frame alignment system may also be constructed consisting of five STS-192 frames; two valid frames followed by three errored frames. The equipment should not enter an out-of-frame state when receiving this pattern.

The loss of pointer (LOP) failure state may be tested by switching between a framed pattern containing valid pointer bytes and one containing non-valid pointer bytes.

In SONET systems, major alarm conditions such as LOS, LOP, LOF cause the alarm indication signal (AIS) to be transmitted downstream. This signal may be simulated with a pattern consisting of valid section overhead bytes and a scrambled all ones pattern in the rest of the frame. This may be simply constructed on a PC, saved on a floppy disk and downloaded into the 71612C analyzer.

The failure state algorithms may be fully tested by selecting the patterns generated in alternate pattern mode by means of an external controller connected to the generator auxiliary input. The controller also counts the pulses received from the pattern generator trigger output. In this way it is possible to control the number of repetitions of each of the alternate patterns, and hence to select the number of frames transmitted. For example, this would allow the LOF failure mode to be fully tested with a sequence of 28 or more errored frames followed by the required number (8 to 24) of repetitions of valid framing patterns.

Error location analysis

In the past, bit error ratio test sets performed quantitative BER measurements that simply informed the user that his device under test had a certain error ratio. The results gave no indication of the possible cause of the errors. The next step was the introduction of simple diagnostics such as errored and error free interval measurement. In recent years the facility to independently measure the BER of errored ones and zeros has been added. This suite of features provided the user with some indication of the cause of errors.

The 71612C analyzer now introduces the next generation of error diagnostics, error location analysis (ELA). ELA helps the user to identify systematic errors.

Error location analysis functions only with RAM-based patterns. These include user-programmable patterns, and the PRBS-based patterns such as variable mark density and zero substitution that are generated from RAM in the 71612C analyzer.

Error location analysis consists of a suite of three measurements:

- Bit BER allows a user to specify any bit in a pattern and to perform BER measurements on that bit alone.

- Block BER allows BER measurements to be performed on a selected range of bits within a user-defined pattern. The range of bits must be a multiple of 32 with the block specified by a start location and block length. This feature is essential when trying to locate the cause of systematic errors which can affect a section of bits in a pattern – for example pattern-dependent errors in the section overhead bytes of an STS-192 frame.

- Error location capture allows the user to capture the actual position of errored bits in a user-defined pattern. After initiation of the measurement, the error detector locates the first (or next) errored bit in the pattern, displays the errored bit, and the sequence of bits either side of the errored bit. The error detector automatically measures the BER of the errored bit. If this BER remains significant over a period of time, it indicates the presence of a systematic or pattern-dependent error. This feature helps the user to differentiate between random and systematic errors, thus helping to identify the source of errors.

Figure 8 shows a block BER measurement being performed on the first 4608 bits of a 1,244,160 bits STS-192 pattern (block start address = 0, block length = 4608) The block error ratio is $7.056e^{-5}$. The block selected from the STS-192 pattern consists of the A1, A2 and C1 bytes from the section overhead.

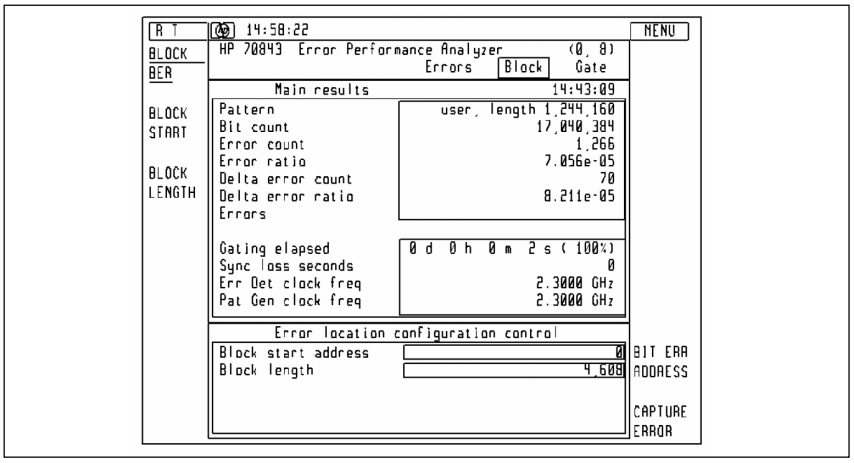

Figure 8. Example of STS-192 block BER measurement

Figure 9 shows the capture of bit 3,322 from a pattern of 1,244,160 bits. The 28 bits preceding the errored bit are displayed in the data window. The bit BER is $8.348e^{-7}$.

The pattern trigger output on the 71612C analyzer may be used to trigger an oscilloscope to automatically display the errored bits and adjacent parts of the pattern as they are captured.

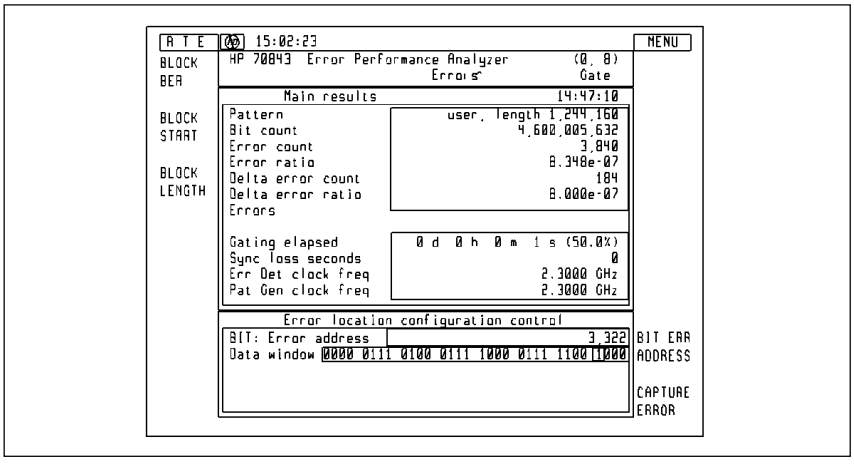

Figure 9. Example of error capture and bit BER

71612C 12.5 Gb/s error performance analyzer

Use the 71612C analyzer to measure bit error ratio (BER) and to verify thoroughly the performance and quality of your components and system hardware.

For more information on the 71612C 12.5 Gb/s error performance analyzer, contact your local Agilent sales office

Related literature

Reach tomorrow's marked today – accurately characterize your Gbit components fast	Brochure	5988-3281EN
Frequency agile jitter measurement system	Application Note (AN-1267)	5988-2749EN
Locating errors in Gigabit transmission systems and components	Product Note	5988-3321EN

Agilent Technologies manufactures the 71612C error performance analyzer under a quality system approved to the international standard ISO 9001 plus TickIT (BSI Registration Certificate No FM 10987).

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