The Agilent Technologies E2920 PCI/PCI-X Series

Application Note 5

Monitor how your device acts on the PCI/PCI-X Bus

Monitoring traffic on the PCI/PCI-X bus is done easily, but if you are designing PCI/PCI-X devices, you need to monitor the traffic relating to a particular device. This application allows you to debug your system quickly and effectively.

The Agilent PCI/PCI-X Analyzer, a combination of testcard and software, simplifies this task. By specifying trigger points, you can focus on a particular device on the bus.

Aims of this Application Note

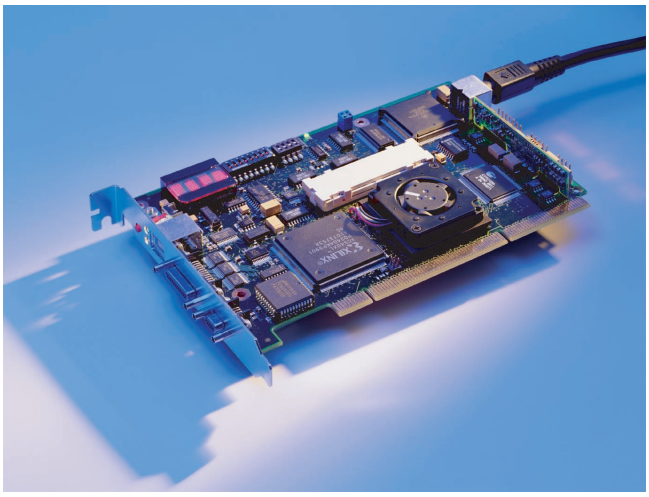
- To show a simple way of capturing traces of a particular device on the PCI/PCI-X bus in order to analyze functional problems.
- To introduce the trigger sequencer, which lets you perform more advanced measurements.

Questions that can be answered with the help of the PCI/PCI-X Analyzer

- How does data transfer to or from a particular device take place?
  Here the Analyzer can help you resolve performance problems. You can see whether the transfer consists mainly of byte transfers or single transfers, or if too many retries are taking place.
- During which bus transaction is data being incorrectly transferred?
- How do changes to the design of your device affect its behavior on the bus?

Benefits of the Agilent PCI/PCI-X Analyzer

- Provides three different display modes to view and evaluate the captured PCI/PCI-X traffic. You can set the modes so that the resulting views correlate with one another. This considerably eases the task of analyzing your device.
- Includes a programmable trigger sequencer.
  This sequencer implements a state machine that allows you to define individual trigger and storage qualifier conditions for each state.



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Setting Up the Test

Introduction

This application note is based around an example that shows you how the Agilent testcard can be used to capture traffic on a PCI or PCI-X bus. Differences between setups for PCI and PCI-X bus systems are explicitly stated.

The example shows you how to set up the testcard to trigger on a particular address range and capture bus traffic that occurs around this trigger point (both prior to and following it). The software offers two methods to let you set the trigger point:

- Single-Level Triggering (for simple measurements)
- The Trigger Sequencer (for more advanced measurements)

Single-Level Triggering

Here the aim is to set up the trigger and the storage qualifier for the Analyzer.
The trigger defines when the Analyzer starts capturing data. The trigger allows you to start capturing data when the programmed trigger event has occurred.
The storage qualification allows you to selectively capture only certain types of data.

Setting Up the Trigger

The following steps explain how to set up the trigger:

1. Open the Capture window. Use the Capture button in the icon bar of the main window, or choose Capture from the Analyzer menu.

2. Open the Pattern Editor dialog box:
- Select the Trigger tab.
- Choose trigger on Pattern.
- Click the Edit button next to the pattern term.

3. Set up the testcard to start capturing data when a single address phase occurs on the bus in the address range of 0xfb000000 to 0xfbffffff. The b_state signal gives an indication of the bus state. It is internally generated by the testcard and is used as a trigger source.
- Set the AD32 field in the Pattern Editor dialog box to FBxxxxxx\h.
- Click on the text field to the right of the signal b_state to open a Selection List dialog box.
- Highlight Addr and click the right-arrow button to place it in the right (Selected) box. Press OK.
- Use the left-arrow button to remove the "DON'T CARE" entry from the Selected list.

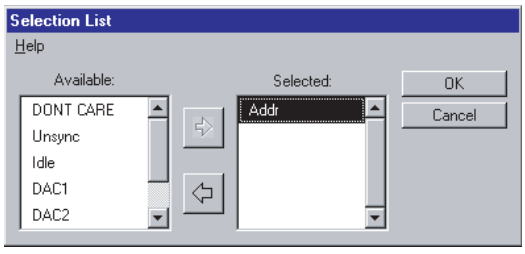


Figure 1.

4. In the Capture window (see below), you can select whether the Analyzer should trigger on the occurrence of the specified pattern on the bus, or on the absence of the pattern within a certain number of clocks.

In this example, you want the Analyzer to trigger immediately after the specified pattern has occurred on the bus. Click the Occurred Once radio button.

The Pattern editor window should now contain the following values:

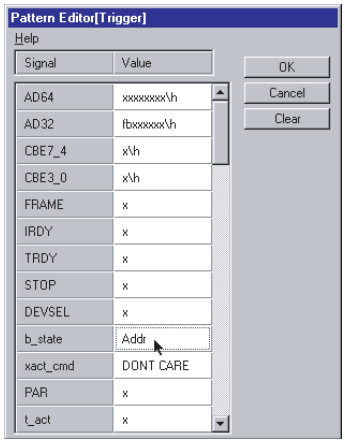


Figure 2.

5. Click OK.
The Capture window should now look like this. The default position for the trigger point slider is at 50%. That means that 50% pre-trigger history and 50% post-trigger history is stored.

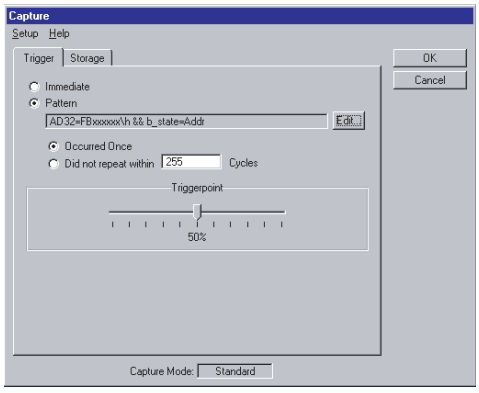


Figure 3.

Setting Up the Storage Qualifier

The Storage page of the Capture window allows you to define the storage qualifier.
The storage qualifier instructs the Analyzer to capture:

- Unconditionally one sample per clock.
- Only certain types of data.

Unconditionally Capturing One Sample per Clock

Use the default setting All.

Capturing Only Certain Types of Data

Choose Selected Transactions/States to suppress idle cycles between transactions and/or wait states during a transaction.
You can further restrict what is captured in the trace memory by storing only particular transaction types (for example, only memory writes).
Click the Edit... button and select the required storage restrictions from the Pattern Editor list.

Using the Trigger Sequencer

The following example highlights the advantages of using the trigger sequencer when setting up sophisticated trigger conditions. It also shows how the captured data can be viewed with the three display modes to analyze PCI behavior of the tested device.

The example shows how to set up the trigger to test a target device and a master device. The device under test (DUT) is a PCI graphics card.

Setting Up the Trigger Sequencer

The aim is to monitor only the traffic from or to a particular device. You therefore need to program the Analyzer to begin capturing data when access to this device starts and to stop capturing data as soon as access terminates.

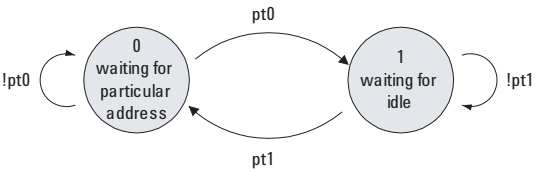
Setting up the trigger condition is simple: You have to provide the analyzer with the base address of your DUT and specify the associated sequence that is to be detected.

Defining a Sequence

The Analyzer has to act as follows:

1. It waits for the address phase of an access to a card, for example to the graphic card.
2. When the address phase is detected, it triggers and stores all the transfers.
3. It stops storing if an idle cycle occurs (it ignores the idle cycle).
4. It waits for the next access to a car, for example to the graphic card.

The trigger sequencer is a programmable state-machine.
The above sequence can be illustrated by a state diagram as shown below. The trigger conditions are determined by patterns pt0 and pt1.



where: pt0 = the address phase
pt1 = IDLE state

Figure 4.

Setting The Trigger Conditions

For this example, the Analyzer is set up to trigger on a PCI address phase with an address in the range between 0xfb000000 and 0xfbxxxxxx.

If you do not know the address of your device, use the Agilent testcard to perform a configuration scan of the PCI bus:

1. Plug the testcard into the primary PCI bus.
2. Open the Command Line Interface from the window menu.
3. Enter the commands cscan and then cscanprnt, (PCI only) each followed by the return key.

The CLI lists all devices found on the PCI bus including their address spaces.

Programming the Trigger Sequencer and the Trigger Conditions for a Target PCI Device

To use the trigger sequencer, the Analyzer must operate in the Sequencer Capture mode. Set the mode as shown in the following figure 5:

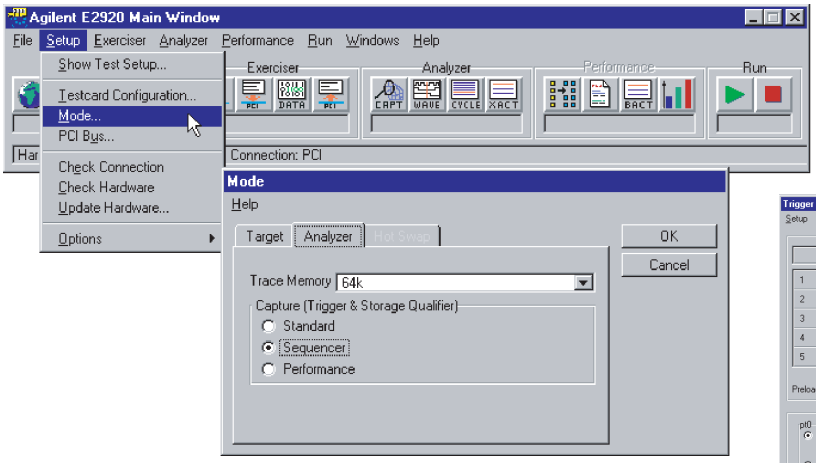


Figure 5.

After you have set the mode, you can set the sequence and the trigger conditions in the Trigger Sequencer dialog box. Open the dialog box by clicking the Capture button in the main window or by selecting Capture ... in the Analyzer menu.

1. Enter the sequence which you have specified previously in Defining a Sequence. In the following figure, the sequence settings have been entered in the Trigger Sequencer dialog box:

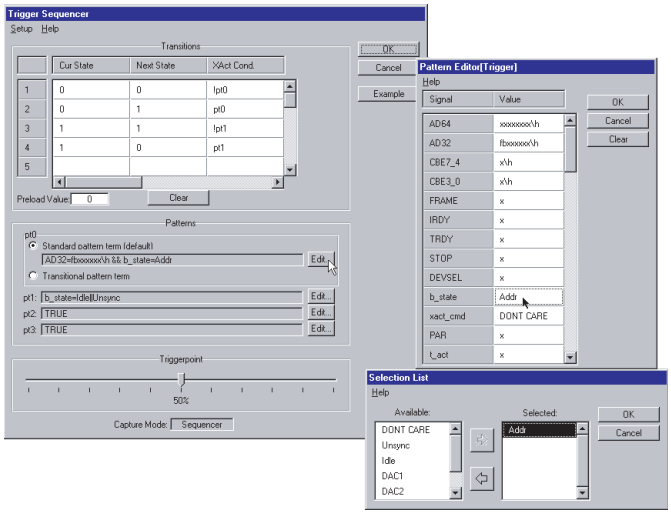


Figure 6.

2. Click the Edit ... button to open the Pattern Editor. Enter the trigger condition values.

3. Finally, assign the value Addr to the signal b_state by selecting it in the Selection List.

Setting the Trigger Condition to Monitor a Master PCI Device

In order to measure and evaluate PCI traffic initiated by particular master devices, you need to know when the master is active. For this purpose, the masters' GNT# (grant) lines must be made accessible to the Agilent testcard. These lines must be connected to the external trigger input pins of the testcard- if necessary, by soldering wires to them.

Defining a Sequence

The Analyzer has to act as follows:

1. It waits until the master becomes active (GNT# line is low) while the bus is idle (trigger0=0 && b_state=idle).

2. When these conditions are met, it triggers on the address phase (T=b_state=addr) and stores the transfers, except idle states (SQ=!(bstate=idle)).

3. It stops storing if an idle cycle occurs and the master's GNT# line is high. (trigger0=1 && b_state=idle).

4. It waits for the next transfer started by the master.

The following figure shows the state diagram of this sequence:

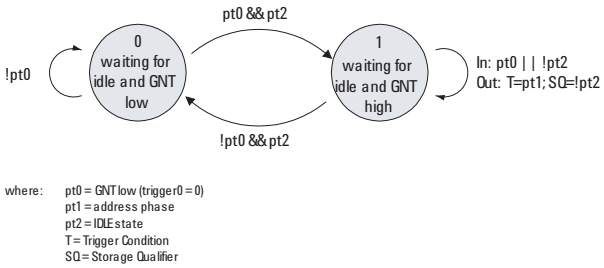


Figure 7.

In this example, the Master's GNT# line is connected to the external trigger input pin[0]. Enter the trigger conditions in the Trigger Sequencer dialog box as follows:

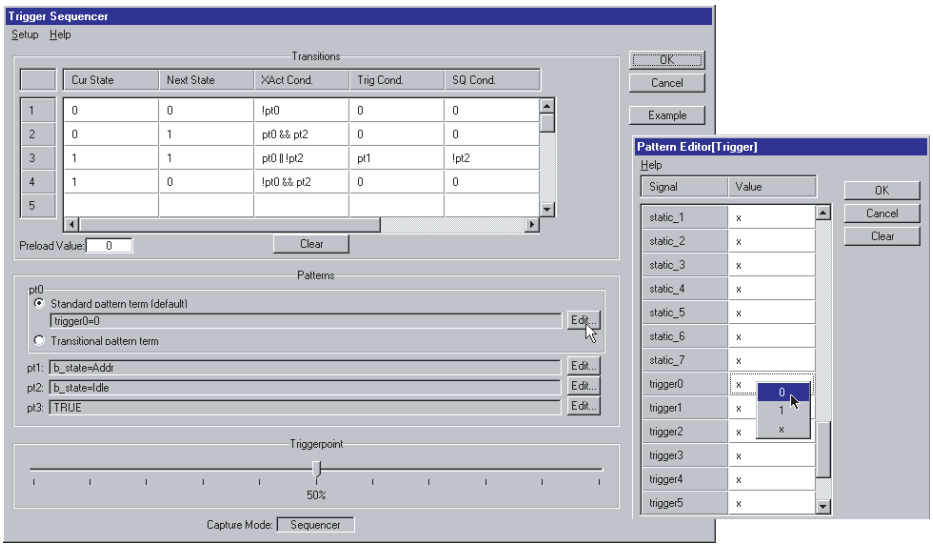


Figure 8.

Using the Trigger Sequencer for PCI-X Devices (valid only with Agilent E2920 PCI-X Series)

The following example shows how to set up the trigger to test a PCI-X graphics card.

Defining a Sequence

The PCI-X Analyzer has to act as follows:

1. It waits for the address phase of an access to a card, for example to the graphic card.

2. When the address phase is detected, it triggers and stores all the transfers.

3. It ignores any idle cycles.

4. It waits for the next access to the graphic card.

Setting the Trigger Conditions

With the PCI-X software, pattern terms are devided in bus and observer pattern terms. For this sequence, the following patterns need to be detected:

· bus0: addr_phase==1 && AD32==fbxxxxxx\h
Bus pattern term bus0 detects an address phase that addresses the range fb000000 ... fbffffff.

· obs0: xact_cmd==Mem_ReadDW && ri_act==1
Observer pattern term obs0 detects Memory Read DWord transfers executed by the requester-initiator.

· obs1: bstate==Idle
Observer pattern term obs1 detects idle cycles.

The following figure shows the state diagram of this sequence:

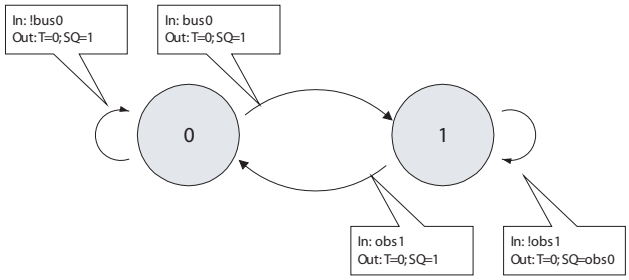


Figure 9.

Setting Up the Trigger Sequencer

Setting up the trigger sequencer for PCI-X devices is very similar to PCI devices:

1. To use the trigger sequencer, the PCI-X Analyzer must operate in the Sequencer Capture mode. To set this mode, check Trigger Sequencer under Options in the Setup menu:

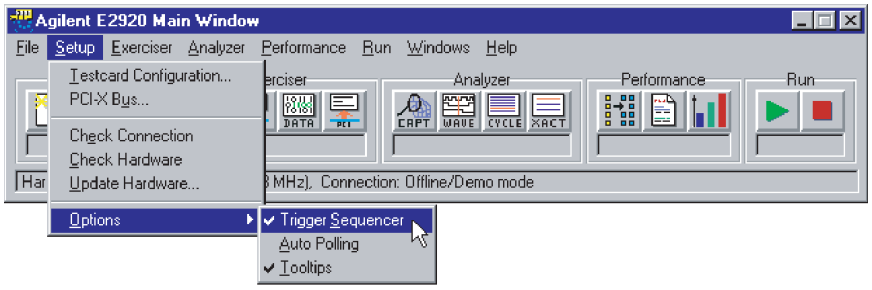


Figure 10.

2. After you have set the mode, you can set the sequence and the trigger conditions in the Trigger Sequencer dialog box. Open the dialog box by clicking the Capture button 

in the main window or by selecting Capture ... in the Analyzer menu.

3. Enter the sequence and the bus and observer pattern terms that you have previously specified. This can be done in the same way as for PCI devices.

In the following figure 11, the sequence settings and pattern terms have been entered in the Trigger Sequencer dialog box:

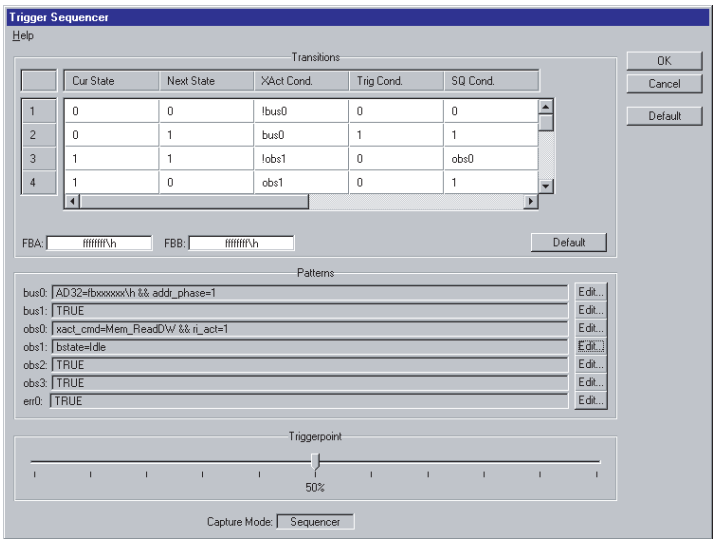


Figure 11.

Running the Test

To run the test, press the Run button in the main window or select Run in the Analyzer menu.

Viewing and Analyzing the Results

To help you analyze the captured data, three different display modes are available:

- Waveform Viewer to analyze captured waveforms
- Bus Cycle Lister to analyze bus cycles
- Transaction Lister to analyze transactions

Analyzing Captured Waveforms

The Waveform Viewer provides a detailed view of the signals on the bus. It is the appropriate display mode when analyzing single transactions or when checking the state of individual control signals.

Open the Waveform Viewer by clicking the Waveform Viewer button in the main window (or select the Waveform Lister item in the Analyzer menu).

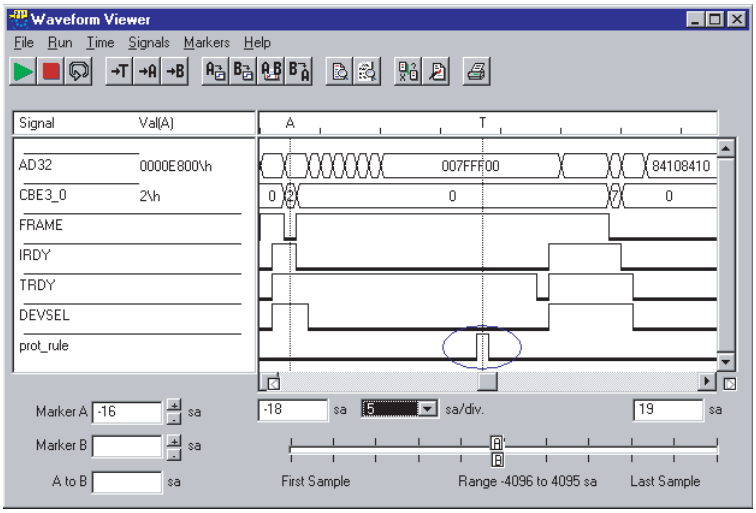


Figure 12.

Click the Trigger button to display data around the trigger point.

To view different signals, select them in the Arrange Signals dialog box. This is available in the Signals menu.

Analyzing Bus Cycles

The Cycle Lister provides a more compact view of the captured PCI transactions.
Open the Bus Cycle Lister by clicking the Bus Cycle Lister button in the main window (or select the Bus Cycle Lister item in the Analzer menu). Figure 13.

To view data around the trigger point, click the Trigger button

To examine the displayed cycles in more detail, click the Cross Reference button (highlighted in the above figure). The Waveform Viewer displays the data. (The Waveform Viewer must be active and not iconized.)

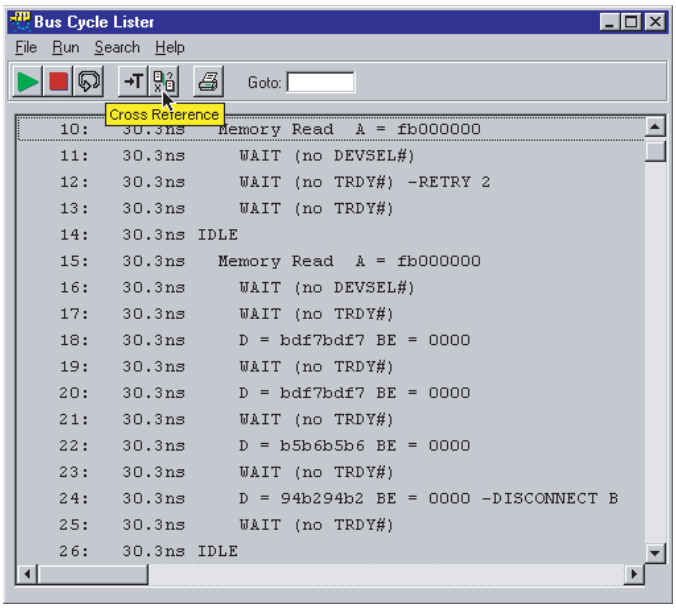


Figure 13.

Analyzing Captured Transactions

The Transaction Lister provides a compressed overview of the transactions that occurred on the bus. It removes idles from the display and summarizes the number of waits for each data phase, displaying only useful information such as address and data phases. Address reconstruction is also done during bursts.

Open the Transaction Lister by clicking the Transaction Lister button in the main window (or use the Transaction Lister item in the Analyzer menu).

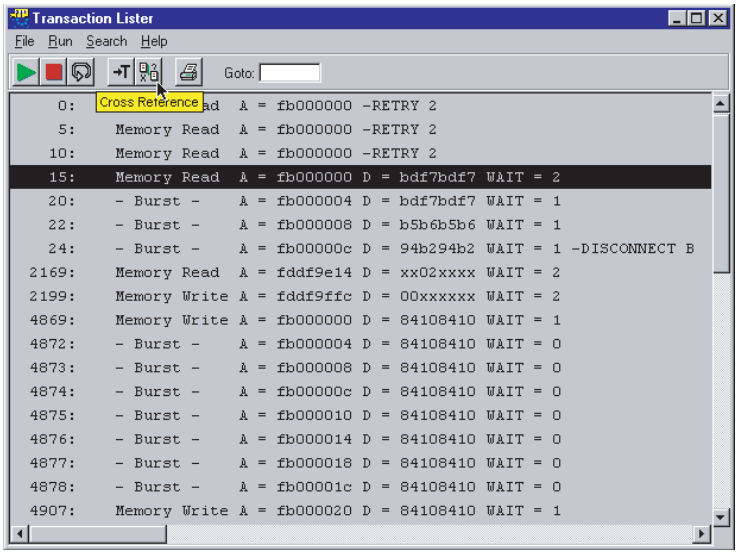


Figure 14.

Glossary

External Trigger	The testcard provides input lines to be used as trigger input and output. As input, they can be used in pattern terms, just like PCI/PCI-X signals. As output, they can be used to trigger other devices.
Pattern Term	The pattern terms can be programmed to recognize bus events (signal patterns on the bus). They are part of the testcard's Analyzer. The output of pattern terms (always 1 or 0) can be used in Analyzer functions, for example, to trigger trace memory or to count bus events.
PCI Analyzer	The testcard's Analyzer queries the PCI bus for information, such as the state of the Exerciser, or the external trigger inputs, so that it can check timing and protocol rules, capture traffic, and measure performance.
PCI-X Analyzer	The testcard's Analyzer queries the PCI-X bus for information, such as the state of the Exerciser, or the external trigger inputs, so that it can check capture traffic.
Sequencer	The sequencers of the testcard recognize sequences of patterns on the PCI bus. They are used by the testcard's Analyzer. A sequencer can be programmed to change between internal states with the occurrence of certain patterns. On each state change, it can issue certain output signals. To recognize these patterns, pattern terms are used.
Storage Qualifier	Storage qualifiers are used by the Analyzer when storing samples in the trace memory. The trace memory stores samples of bus states for post-processed analysis. To exclude unnecessary samples from being stored, the Analyzer provides storage qualifiers.
Trace Memory	The trace memory is part of the testcard's Analyzer. It stores all PCI/PCI-X signals along with extensive bus state and Exerciser state information. All this information is aligned.
Trace Memory Trigger	The trace memory trigger is part of the Analyzer. The trace memory stores samples of bus states for post-processed analysis. To control the start of the sampling, the Analyzer provides the trace memory trigger.

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Related Agilent Literature

- Agilent E2925B 32bit, 33 MHz, Agilent E2926B 32/64bit, 33 MHz PCI Exerciser & Analyzer, technical specifications, p/n 5968-3501E
- Agilent E2928A 32/64bit, 66 MHz, PCI Exerciser & Analyzer, technical specifications, p/n 5968-3506E
- Agilent E2929A PCI Exerciser & Analyzer, technical specifications, P/n 5968-8984E
- Agilent E2922A PCI-X Master Target Card, technical overview, p/n 5968-9577E
- Agilent E2940A CompactPCI Exerciser & Analyzer, technical overview, P/n 5968-1915E
- Agilent E2976A System Validation Pack, Agilent E2977A System Test Library, technical overview, p/n 5968-3500E
- Agilent E2920 Computer Verification Tools, PCI Series, brochure, p/n 5968-9694E
- Intel discusses basic concepts of PCI performance and efficient use of PCI with the Agilent E2920 series, case study, p/n 5988-0448ENDE
- HP NSD stabilizes server designs quickly and completely with the Agilent E2920 PCI Series, case study, p/n 5968-6948E
- HP HSTC speeds high-end server testing and reduces engineering costs with the Agilent E2920 PCI Series, case study, p/n 5968-6949E
- Agilent E2920 Verification Tools, PCI Series gives Altera Corporation competitive Advantage, case study, p/n 5968-4191E
- **5 Measurements of Agilent E2920 PCI/PCI-X Series p/n5988-3395EN**

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