Designing High-Speed Digital Systems for Logic Analyzer Probing

Application Note

Purpose and Scope

When probing high-speed digital signals with a logic analyzer, you must take the electrical characteristics of the probe into consideration in the design of the target system. The input to the probe, including the probe connector, becomes a part of the circuit of the target system. The purposes of this application note are:

- To identify the issues that are critical when designing a target system that includes probes for logic analyzers.
- To provide information about the electrical models of the probes available for Agilent logic analyzers, with special emphasis on the Agilent 16760A, 1.25 Gb/s, differential logic analyzer, and guidelines for how to use that information most effectively.
- To provide design recommendations and examples for layout of target systems incorporating logic analyzer probing connectors.
- To help ensure that your design will operate correctly with the logic analyzer connected.

This application note is limited to probing with multiple-channel probing connectors that are designed into the target system. Many of the general principles described herein also apply to probing with individual flying leads.

All the examples in this application note refer to the Agilent E5378A and E5379A probes, which are compatible with the Agilent 16760A, 1.25 Gb/s, differential-input logic analyzer. The general principles and procedures described in the examples may be applied to designing in other probes for other logic analyzers. To do this, you will need to know the parameters of the specific probe and logic analyzer, specifically:

- Minimum input amplitude
- Setup and hold time
- Equivalent probe load

These can be found in the Agilent reference documents listed in "Recommended Reading."

The requirements for probing are fundamentally different from the design requirements of a connection system to transmit signals within a controlled - impedance environment.

Guidelines and recommendations in this application note apply only to the design of the logic analyzer probes in a digital system.

Contents

Agilent Technologies

Selecting the Optimum Probe and Connector

Probe	Usable with Agilent Logic Analyzers	Maximum State Acquisition Speed
E5346A	All except 16760A	400 Mb/s
E5385A	All except 16760A	400 Mb/s
E5378A	16760A	1250 Mb/s
E5379A	16760A	1250 Mb/s
E5380A	16760A	600 Mb/s

Table 1. Agilent logic analyzer probes that incorporate isolation networks

Agilent recommends the E5378A, E5379A, or E5385A for new designs. These probes provide lower input capacitance, lower inductance, and better isolation between adjacent signals compared to the E5346A and E5380A. The mating connector for these probes does not require through-holes in the PC board under the connector, thus greatly alleviating restrictions on signal routing.
For compatibility with preexisting target systems that were designed with the 38-pin mating connector, Agilent provides the E5380A probe for the 16760A logic analyzer.
Figure 1 compares the impedance of the E5346A, E5378A, E5379A, E5380A, and E5385A. As you can see, the E5346A and E5380A have resonances at lower frequencies, and the resonances dip to a lower impedance compared to the E5378A, E5379A, and E5385A probes.

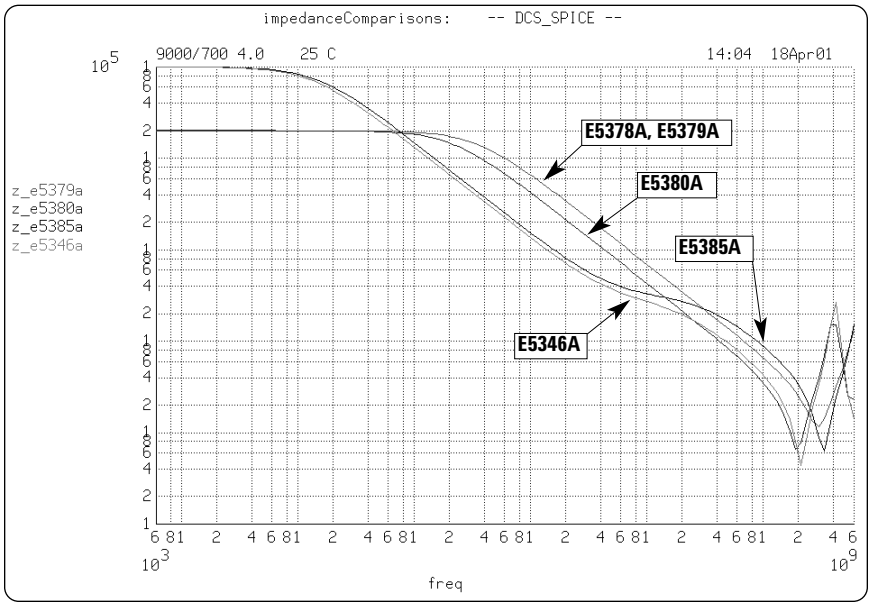

Figure 1. Impedance comparisons

Probe Load Models

The probe load models shown in this application note and in the other Agilent documents listed in the section “Agilent Reference Documents” are intended to represent the effective load of the probe and connector. They are not intended to be literal or complete models of the entire probe and logic analyzer front end. The models are designed to be inserted into the Spice model of the target system.

These models are realistic, in that they include a typical PC board pad and solder, not just the connector and probe. Note that the models published by connector manufacturers typically are “free-space” models; they do not incorporate the effects of any PC board mounting. They also do not include the loading effects of the circuits inside the logic analyzer probe.

The models were developed to provide both accuracy and simplicity. Accuracy is important to ensure that the effects of the probe are correctly accounted for. Simplicity is important to avoid long simulation times and an unnecessarily large number of elements in the models.

Models for E5378A, E5379A

Figures 2 and 3 are the equivalent probe load models for any one input channel on both the Agilent E5378A single-ended probe and the E5379A differential probe for the Agilent 16760A logic analyzer. Figure 2 represents the input to the probe–including the PC board pads, solder blob, and connector–as a short transmission line. In figure 3, the input to the probe is represented as a 3-segment lumped LC network. As you can see from figure 4, the two models agree well, and both agree well with the measured impedance. The model in figure 3 is desirable for Spice simulations because it will generally simulate faster.

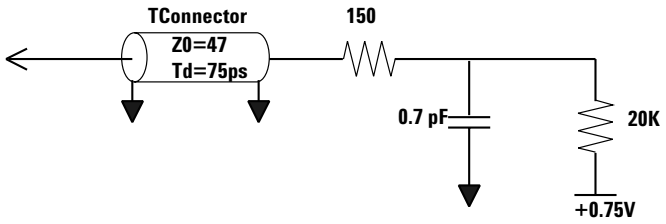

Figure 2. Transmission line segment model for E5378A, E5379A

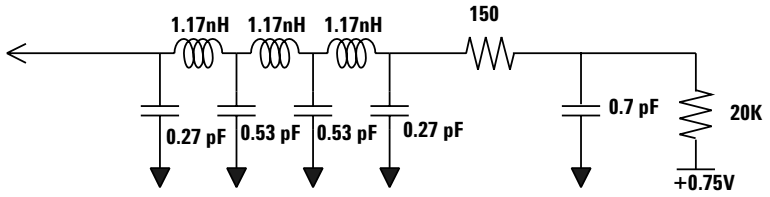

Figure 3. Lumped LC model for E5378A, E5379A

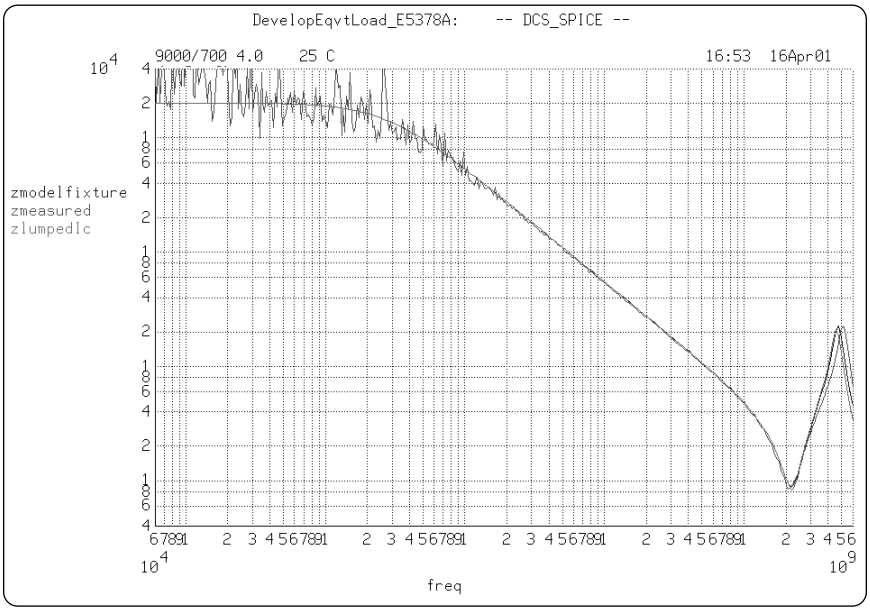

Figure 4. Measured vs model impedance for E5378A, E5379A

Figure 4 illustrates the comparison between the simulated impedance for the models shown in figures 2 and 3, and the actual measured impedance of the probe and connector mounted on a PC board, including the mounting pad.

Models for E5346A, E5385A and E5338A

Figures 5, 6, and 7 are the equivalent probe load models for the E5346A, E5385A, and E5380A. The impedances for these probes are illustrated in figure 1.

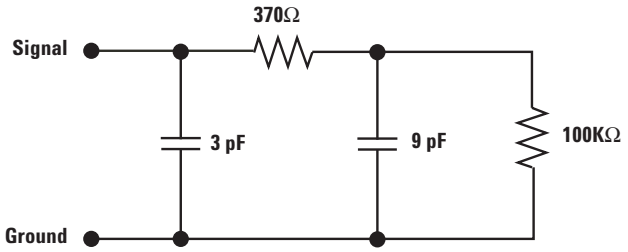

Figure 5. Equivalent probe load model for E5346A

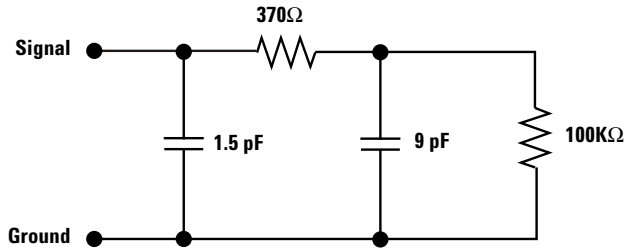

Figure 6. Equivalent probe load for E5385A

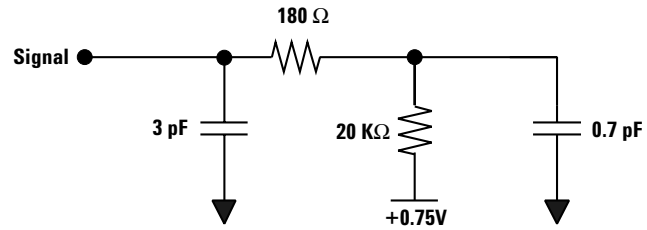

Figure 7. Equivalent probe load for E5380A

Differential Signals and Transmission Lines

All the examples in this application note refer to single signals carried on a single conductor. The examples are valid either for single-ended signals, or for individual signals within a differential pair.

For differential signals, the minimum signal amplitude at the probe input of the 16760A is 200 mV p-p. This refers to the difference between the positive and complement of a differential pair.

Extra care must be taken in routing differential signals to avoid skew between the positive and complement signals in a differential pair. As illustrated in figure 10, if the skew between the two sides of a differential signal is on the order of the rise and fall time or greater, the difference signal will suffer from a "shelf". Worse yet, this shelf will be at a difference signal of zero volts. In differential operation, the 16760A discriminates below a high and a low input based on the crossover where the positive and negative inputs are equal. The resulting "shelf" will therefore cause a period of uncertainty in determining where the 16760A will detect a change from a high to a low.

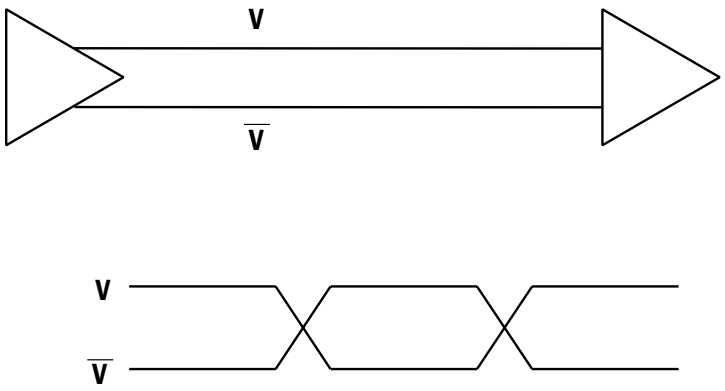

Figure 8. A differential transmission system

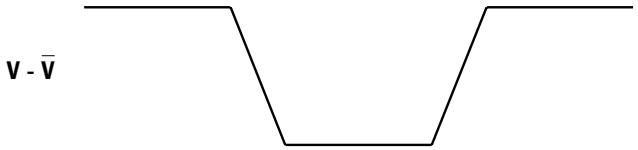

Figure 9. For a differential signal, V – $\overline{V}$ must be >= 200 mV

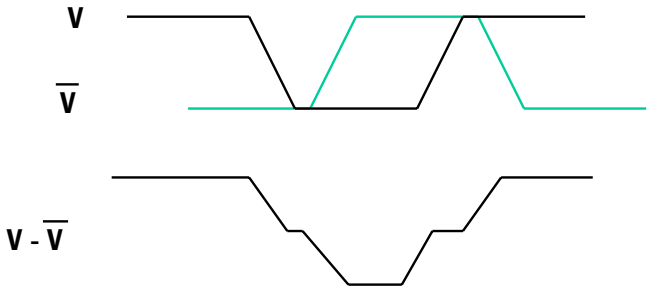

Figure 10. Excessive skew between the two components of a differential signal, resulting in a distortion of the rising and falling edges of the difference signal

Design Examples

Damped Stub

At high frequencies, PC board traces must be considered as transmission lines. A reasonable rule of thumb is that if the propagation delay of a trace exceeds 20 percent of the signal rise time, it should be modeled as a transmission line. A stub is defined as an unterminated branch of a transmission line. When a signal propagating on a transmission line encounters a branch, a portion of the signal energy will propagate along each branch and, due to the impedance mismatch caused by the branch, a portion of the energy will be reflected back toward the source. The point of the branch will appear as a step function decrease in impedance, resulting in a mismatch.

If you are not familiar with transmission line fundamentals and theory, we strongly recommend reading one of the reference works listed in the recommended reading. An introduction to transmission line behavior and theory is beyond the scope of this application note.

One decades-old solution for connecting a target bus to a logic analyzer probe connector has been to use a stub. A stub allows the connector to be placed at a convenient location away from congestion commonly surrounding target driver and receiver devices. The target bus is tapped with the stub trace over to the logic analyzer connector, sometimes as far as 6 inches away. For many years, that has been an acceptable solution for routing to logic analyzer probe connectors.

Until recently most systems (and logic analyzers) were running at < 100 MHz clock rates. Only in the last few years have general-purpose logic analyzers been available to capture buses at higher frequencies. System designers have attempted to use the old stub methodology to connect a target to a logic analyzer, but it has become increasingly difficult to maintain system bandwidth and provide adequate signal bandwidth at the probe tip.

For the 16760A running at 1250 Mb/s clock rates, the stub method of connecting to the logic analyzer probe is all but impossible. As simulations will readily reveal, even a short trace stub length represents a substantial portion of the load on the target, and will noticeably degrade the signals provided to the logic analyzer probe. Long trace stubs will dominate the total load seen by the target, and will be more of a problem than the probe load. The laws of physics are colliding with the need for system speed.

Consider for a moment a trace stub that is 0.2 inch of a 50 Ω microstrip. This seemingly innocuous short trace will result in an additional 0.6 pF of capacitive load, bringing the total capacitive load of the stub plus probe load to 2.2 pF. If that same trace stub were increased from 0.2 to 1.0 inch, the capacitance of the stub would be 3.0 pF, which has well surpassed the capacitance of the probe load. As you can see, stubs can significantly and adversely affect the load on the target bus.

To illustrate this point, the following analysis of a stub connection from a target bus to a logic analyzer may prove useful in understanding why a stub can be such a detriment to high-speed systems. Note that a stub is not necessarily unfeasible in all cases. For some applications, even for the 16760A, short damped stubs may be an acceptable solution that gives adequate system performance as well as adequate logic analyzer performance.

For illustration purposes, consider the hypothetical layout of a simple target driver, receiver, and probe connector for a single trace in figure 11. The traces are assumed to be surface microstrip construction, yielding 50 Ω transmission line impedance with 150 ps/inch propagation velocity.The traces are annotated for length, impedance, and propagation delay.

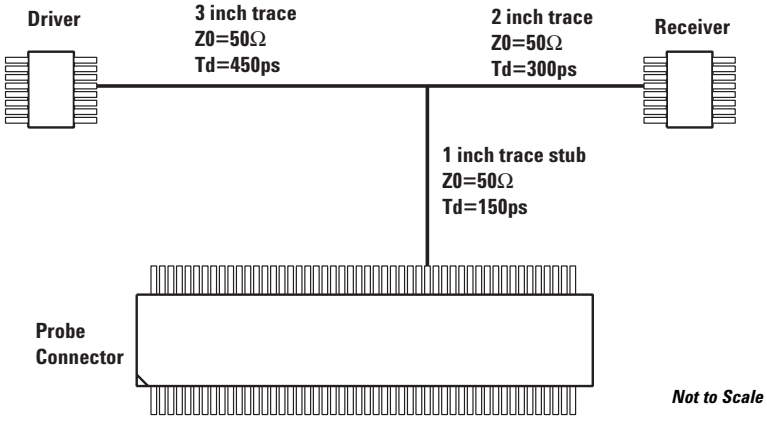

Figure 11. Stub connection to logic analyzer (hypothetical trace stub layout)

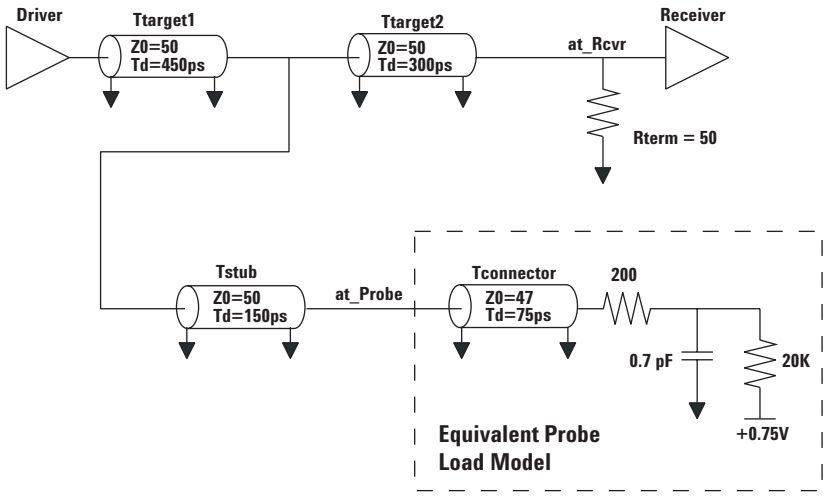

Figure 12. Schematic representation of stub connection to logic analyzer (hypothetical load-terminated bus with 1 inch stub to connector)

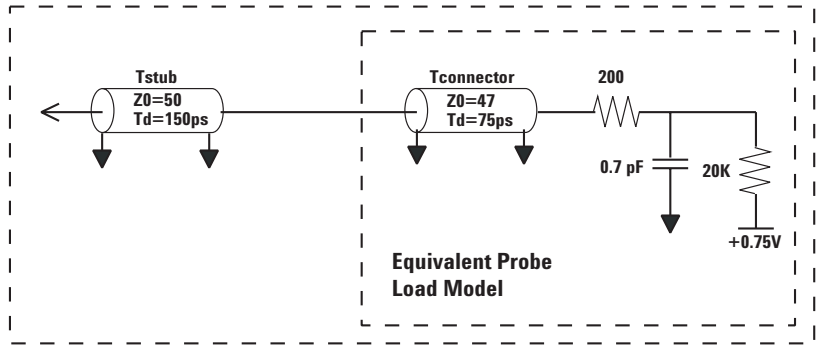

Figure 13. Total load on target bus with trace stub

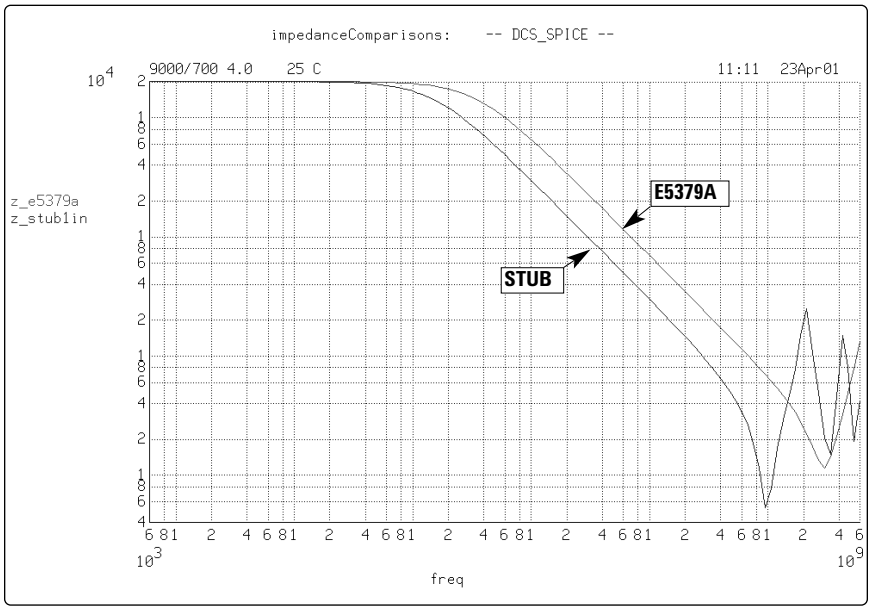

Figure 14. Impedance of total load on target including stub

The schematic representation of this hypothetical layout is shown in figure 12. The nodes “at_Rcvr” and “at_Probe” are indicated for referencing simulation results.

Determining Total Equivalent Load On Target Bus

The total load on the target bus for the layout example above is no longer adequately represented by the E5379A equivalent probe load model. To determine the true total equivalent load on the target, you must include the trace stub to the connector. The schematic representation of the total load is shown in figure 13, which shows both the stub and the equivalent probe load model.

The trace stub is significant. For the layout example above, the additional capacitive load presented by the 1 inch trace stub is another 3 pF, bringing the total capacitive load to 4.6 pF. The load from the 1 inch stub has dwarfed the probe load. This can be observed in the impedance plot in figure 14. Compare the original E5379A probe load model in figure 5 to the new total load model in figure 14.

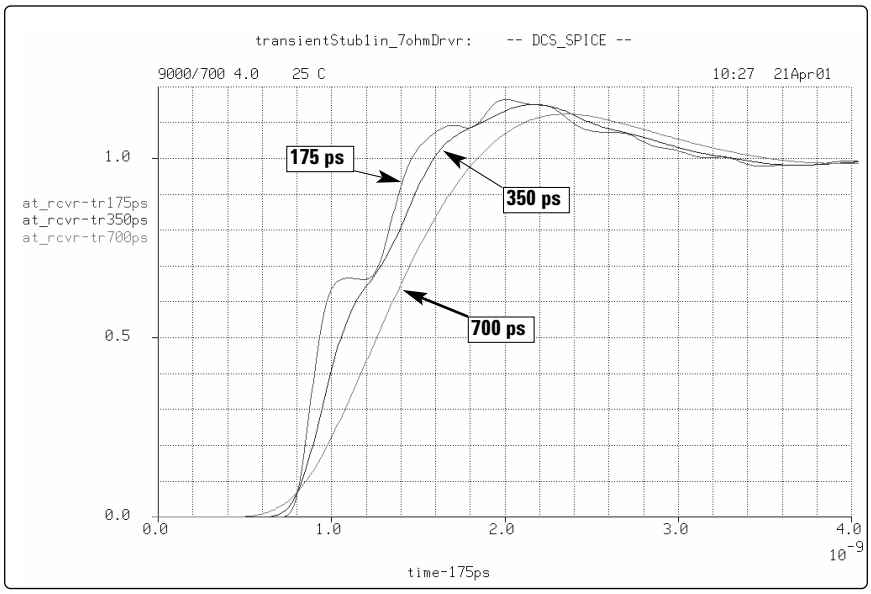

Figure 15. Effect on target waveform at the receiver for a 1 inch stub

Determinating the Effect on the Target Bus

Probe load models are useful for understanding the potential effect on the target bus. But the real determination of goodness is what the signal looks like at the receiver. A transient analysis of the signal reveals that, depending on the target rise time, the 1 inch stub may be a problem. The simulations in figure 15 show the effect of the total probe load at the receiver for rise times of 175 ps, 350 ps, and 700 ps. For systems running 350 to 700 ps rise times, a 1 inch stub length is borderline. For sub-350 ps rise times, the 1 inch stub is probably unacceptable.

"Rules of thumb" abound for maximum stub lengths. Usually a ratio of the stub electrical length to the system rise time is applied, with ratios of 1/3 to 1/10 widely used. A 1/5 ratio of stub length to rise time is usually acceptable, but as in any general rule of thumb, can't be relied upon as the standard for determining maximum stub length. System margins may allow for more relaxed ratios or require much more stringent ratios.

The simulated rise times at the receiver are 550 ps, 700 ps, and 800 ps. respectively. The reduction in rise time is directly related to the capacitive load of the combined stub and probe load. If the ratio of stub electrical length to driver rise time is less than 0.2, an estimate of the rise time at the receiver (Trcvr) can be made with the following equations:

Cload = Cstub + Cconnector
Zdrive = Ztarget
Tfilter = 2.2 x Zdrive x Cload
Trcvr = SQRT ($Trise^2$ + $Tfilter^2$)

For this example:

Cload = Cstub (1 inch) + Cconnector
= 3.0 pF + 1.6 pF = 4.6 pF
Zdrive = 1/2 Ztarget = 25 Ω
Tfilter = 2.2 x Zdrive x Cload
= 2.2 x 25 Ω x 4.6 pF
= 253 ps

For the 700 ps driver, the receiver would see an estimated rise time of SQRT(700 ps^2 + 253 ps^2) = 744 ps

For the 350 ps driver, the receiver would see an estimated rise time of SQRT(350 ps^2 + 253 ps^2) = 431 ps

For the 175 ps driver, the receiver would see an estimated rise time of SQRT(175 ps^2 + 253 ps^2) = 308 ps

This equation does not estimate rise time well as rise time gets faster. The stub electrical length is too high compared to the driver rise time to make a reasonable estimate.

Determining the Effect at the Analyzer Probe Tip

Figure 16 shows the simulated waveforms at the probe tip for the 1 inch stub example. The ringing at the probe tip is due to reflections and re-reflections on the unterminated stub. These reflections will cause data-dependent jitter at the probe tip, collapsing the eye by reducing both voltage and time margin to the analyzer. If the eye is at least 250 mVp-p (for the E5378A single-ended probe) tall and 500 ps wide for all data stream patterns and conditions, then the design solution is acceptable.

A typical question is whether or not it is good practice to insert a damping resistor (Rdamp) between the target bus and the connector stub, thereby isolating the effects of the stub and connector from the target bus. In general, this can be a good idea for small values of Rdamp, which will be explained in the following section. Figure 17 shows the previous example layout and schematic of the same stub routing to the connector with the addition of Rdamp. Figure 18 is the schematic representation of this change.

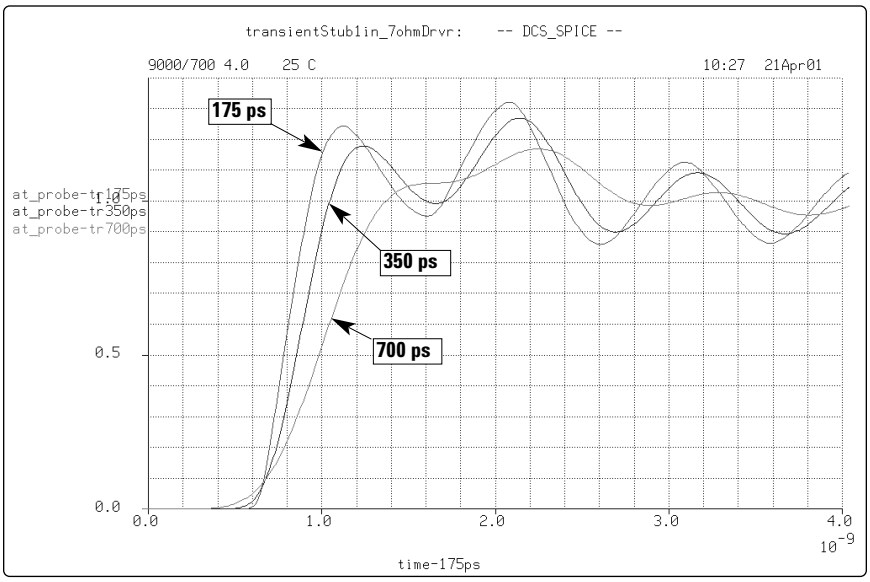

Figure 16. Waveforms at logic analyzer probe tip for 1 inch stub example

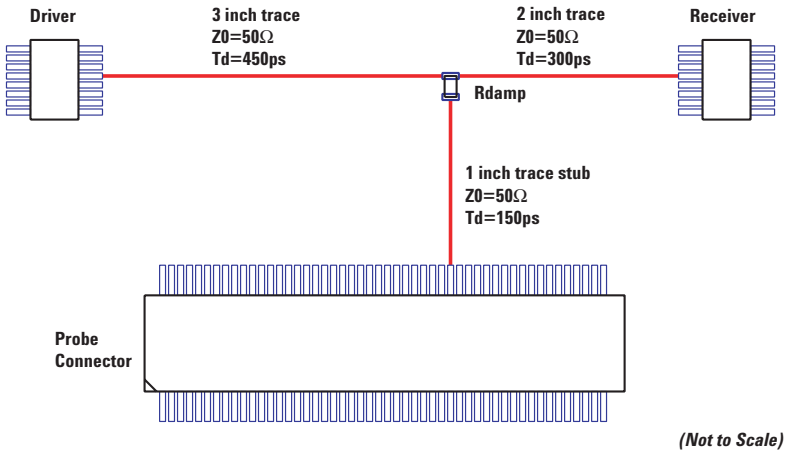

Figure 17. Addition of damping resistor (hypothetical trace stub layout with Rdamp)

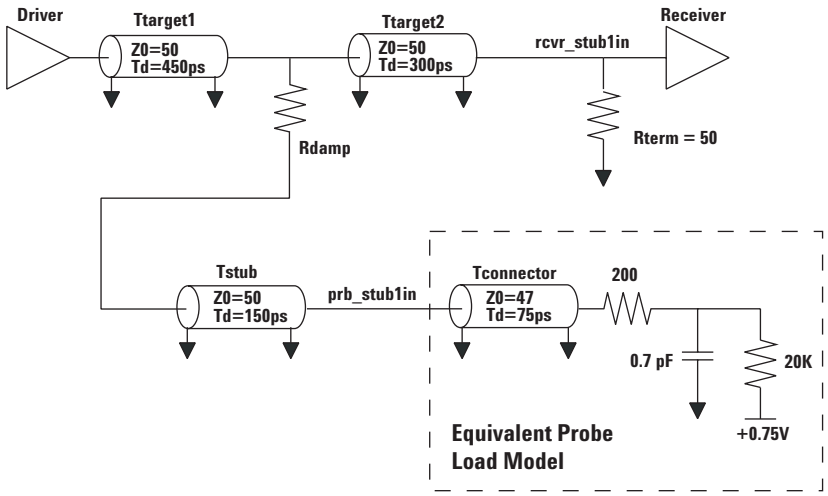

Figure 18. Schematic showing addition of Rdamp (hypothetical load-terminated bus with Rdamp isolating 1 inch stub to connector)

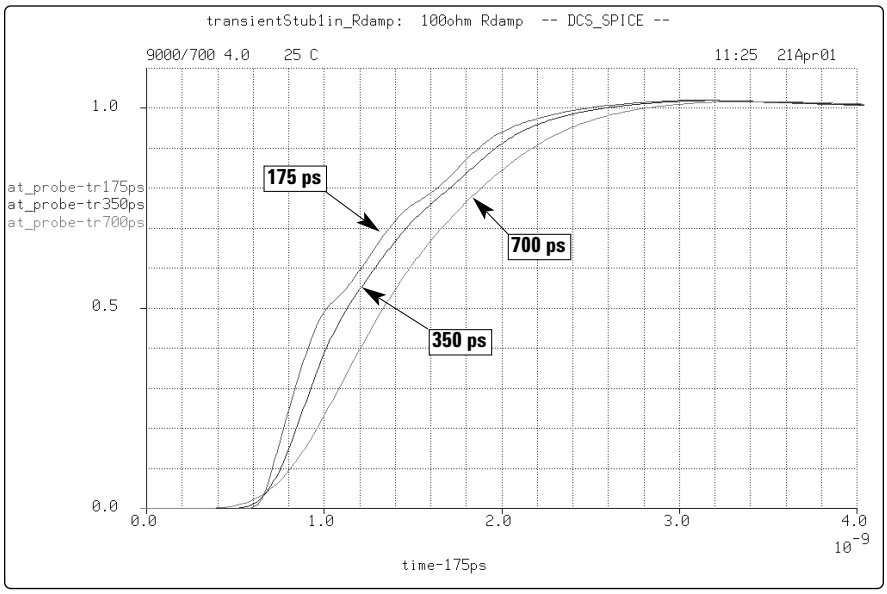

Figure 19. Effect of 100 Ω damping resistor on waveforms at logic analyzer probe input

Determining the Value of Rdamp

There is a critical value of Rdamp that improves the isolation on the target bus and improves the response at the probe. As a rule, Rdamp ≥ Zstub – 1/2 Ztarget. The minimum value of Rdamp can be chosen such that Rdamp acts like a source-terminating resistor, eliminating the ringing on the stub. However, be careful of setting Rdamp too large. If Rdamp is too large, the performance of the logic analyzer will be severely limited by the low-pass filter effect of an impedance driving a capacitive load. The low-pass filter driving impedance is set by Rdamp plus 1/2 Ztarget. The total C is set by the trace stub and the connector.

Consider the effect of a 100 Ω value of Rdamp in our current example. The driving impedance into the stub is Rdamp 100 Ω + 1/2 Ztarget = 125 Ω. The total capacitance of the 1 inch trace stub and the connector is roughly 4.6 pF. Therefore, the cutoff frequency of the low-pass filter created by Rdamp is calculated to be 1/(2 x pi x Rtot x Ctot), or roughly 300 MHz. A sinewave at 300 MHz will be attenuated 3 dB, or 30 percent, in amplitude.

In a digital system, the target is generating a series of pulses of varying width, not sinewaves of continuous frequency. A rough approximation of the maximum usable clock rate then is that a pulse cannot be narrower than 2 x rise time. Even at 2 x rise time, the signal is not reaching full amplitude and may violate the logic analyzer specifications. A rough approximation of the rise time using the same variables in the paragraph above would be 2.2 x Rtot x Ctot = 1.26 ns. From the simulations in figure 19, you can see that the rise time is indeed roughly 1.25 ns. Because the low pass filter rise time is significantly larger than the original rise time, the low pass filter will set the rise time seen by the probe regardless of the original rise time of the target driver.

For lower-speed target systems (2.5 ns minimum pulse widths), this solution still may have adequate bandwidth to capture the bus reliably with the logic analyzer. For higher-speed systems, though, this low-pass filter effect will probably prevent the analyzer from properly capturing data on the bus. The analysis needs to be performed for the specifics of the target bus. Keep in mind that the signal at the probe connector must meet the specifications of the logic analyzer to ensure reliable capture of data.

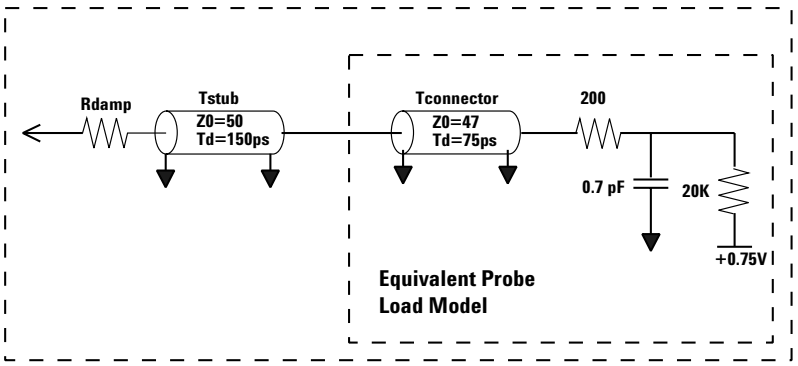

Figure 20. Model of damped stub for analysis

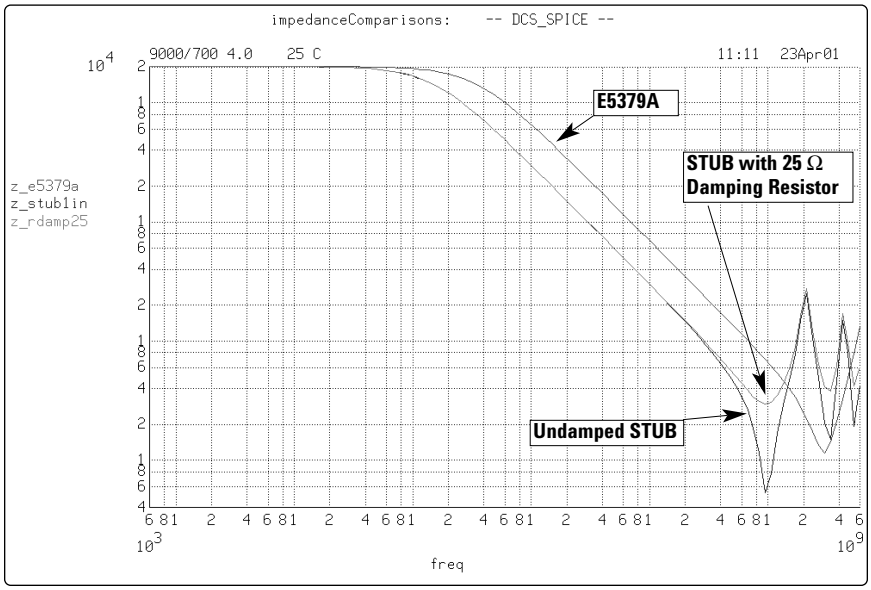

Figure 21. Impedance of stub with 25 Ω damping resistor

Critically Damped Example

Now let's analyze the effects of a critically damped stub. For the example we've been using, the critical value of Rdamp would be Zstub – 1/2 Ztarget = 25 Ω. This may not seem like much. Indeed, it makes only a slight improvement on the response seen by the target receiver, but it makes a substantial difference in the signal seen by the probe. The 25 Ω also substantially reduces the resonance in the equivalent load, as can be seen in the simulation results in figure 21.

Looking at the impedance plot in figure 21, the 25 Ω damping resistor does have an effect on the resonant impedance, limiting the impedance to 25 Ω or so. This is helpful, but probably not enough to regain the system bandwidth.

The effect on the signal as seen by the target receiver is subtle. The transition times seen by the receiver are improved slightly. For the fastest rise time simulated, the flat "step" from the stub reflecting back into the target bus has been improved, moving from 65 percent with no damping to 75 percent with a 25 Ω Rdamp (critically damped). However, compared to the non-isolated stub, no significant improvement in the rise time (as seen by the receiver) is observed (figure 22).

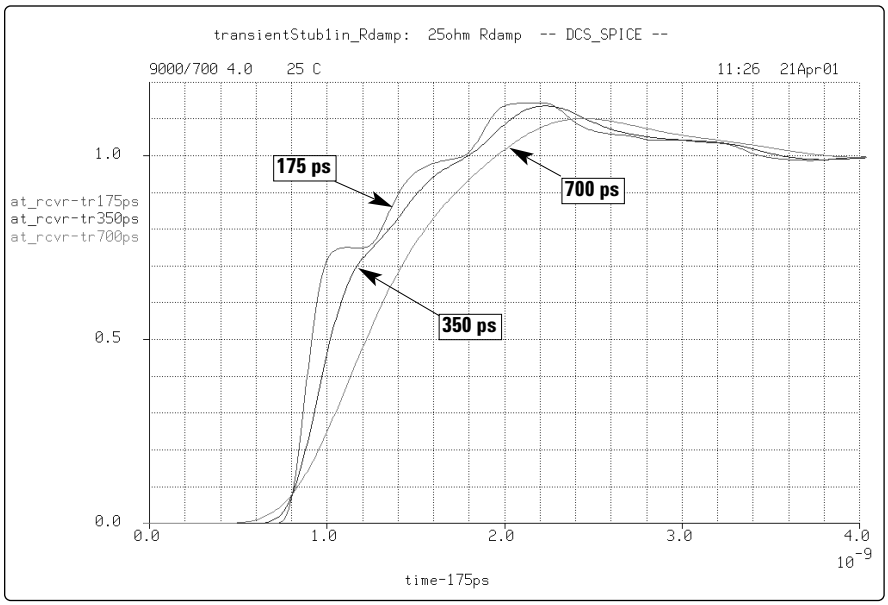

Figure 22. Signal at receiver, 25 Ω damping resistor

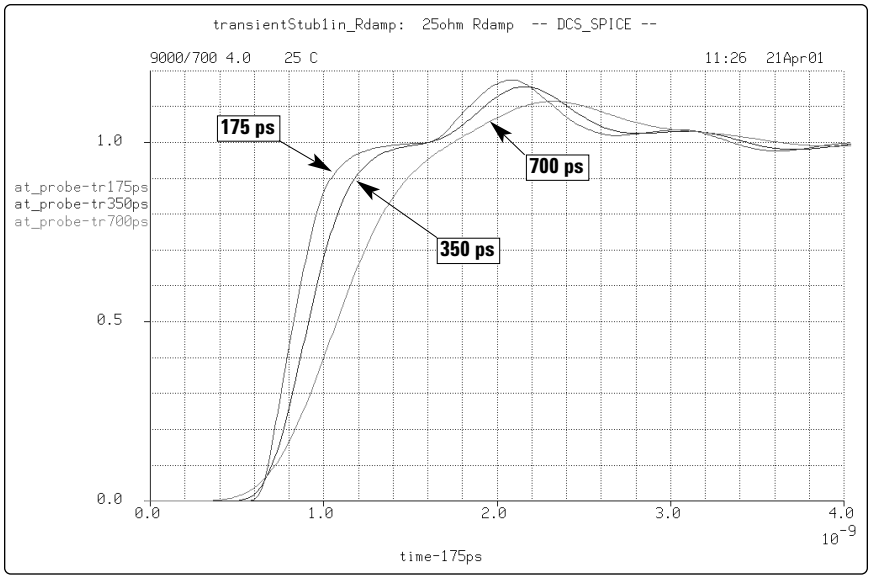

Figure 23. Signal at logic analyzer probe input, 25 Ω damping resistor

Notice that the signal seen by the logic analyzer is improved (figure 23). The ringing is eliminated, with little effect on rise time. In fact, for this example, the rise time seen at the logic analyzer probe tip is cleaner and faster than the rise time seen by the target receiver. Some optimization may be desired to balance the bandwidth at the target receiver with the bandwidth at the logic analyzer probe.

What about Longer Tab Stubs?

Realizing that for some systems a 1 inch stub is too short to be of any value, we can lengthen the stub in our example to show the effects of longer stubs. However, it ought to be clear by now that the performance degradation caused by adding a 1 inch stub is going to get worse as we increase the length of the stub. For illustration purposes, let's assume that the stub length is increased from 1 to 5 inches and re-run some of the analyses.

First, the schematic needs to be modified for a 5 inch stub length (Td=750 ps) (figure 24).

The minimum critical value of Rdamp = Zstub – 1/2 Ztarget = 25 Ω still applies, regardless of trace length. However, as the equivalent impedance plots will show, the total equivalent load is now extremely capacitive at 16 pF. A 25 Ω value for Rdamp will do little to hide the effect of such a large capacitive load on the target bus.

To effectively isolate the bus, Rdamp would have to approach 150 Ω or more. But such a large value of Rdamp would result in unacceptable bandwidth at the logic analyzer probe. Referring back to the equations used before, the 3 dB bandwidth of the signal at the probe tip would be approximately 1/(2 x pi x Rtot x Ctot) = 1/(2 x pi x 150 Ω x 16 pF), or 66 MHz. The rise time also could be approximated at 2.2 x R x C = 5.3 ns. Neither of these metrics is even close to approaching the signal bandwidth required for the logic analyzer to view the target bus, unless the bus is operating at a fairly slow clock speed.

In short, the rest of this illustration will demonstrate that long stub lengths are unacceptable as a probing solution for high frequency applications. While this method has been successfully used over the years for what used to be considered state-of-the-art designs, it will yield unsatisfactory results for the speeds at which the 16760A was designed to run.

To continue with the analysis of the 5 inch stub, figure 25 shows the load representation on the target bus.

The simulations in figure 26 show the equivalent impedance relative to a 1 inch stub and no stub for the E5379A probe.

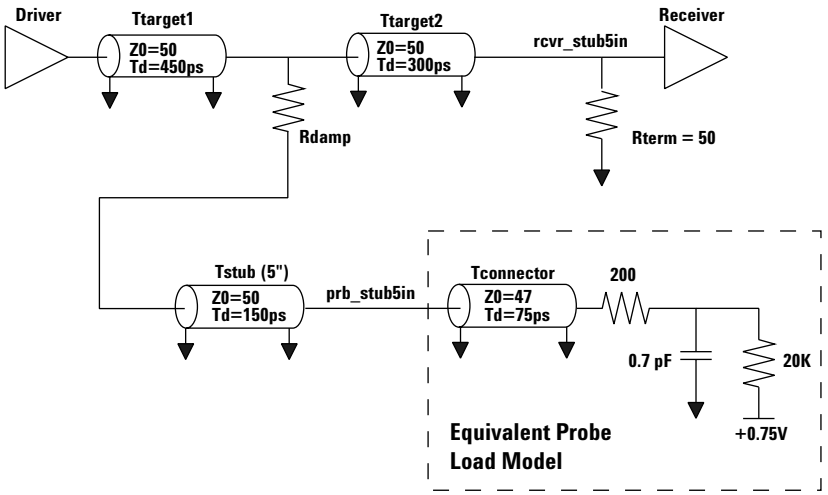

Figure 24. Schematic for hypothetical load-terminated bus with Rdamp isolating 5 inch stub to connector

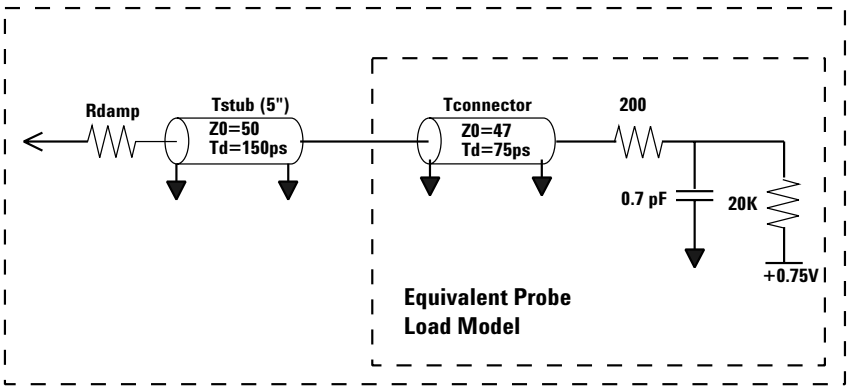

Figure 25. Simplified schematic showing effective load on target bus, 5 inch stub with 25 Ω damping resistor

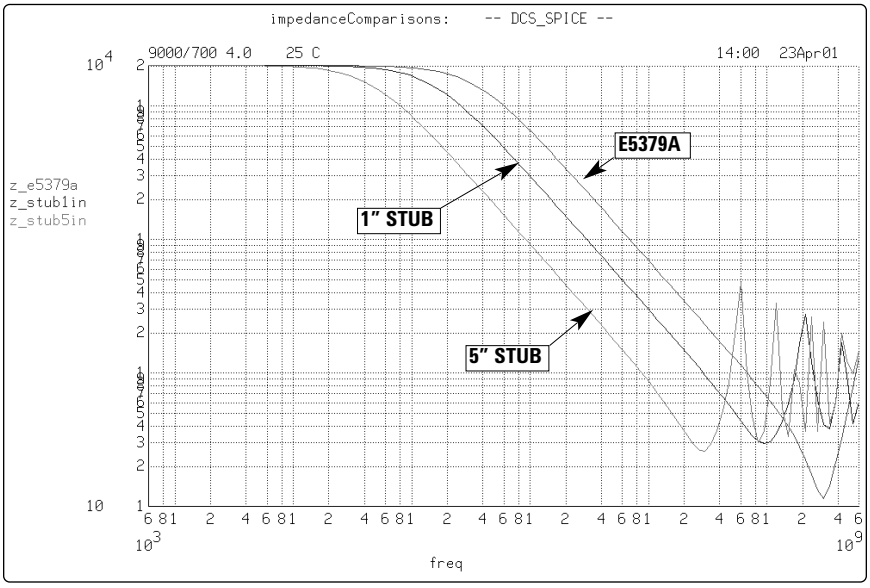

Figure 26. Impedance of load on target for 5 inch stub with 25 Ω damping resistor

The equivalent load of a 5 inch stub looks far worse than the 1 inch stub. This will significantly impact the performance of both the target receiver and the logic analyzer probe.

The signal at the target receiver (figure 27) is grossly distorted, even for the 700 ps rise time. The steps in the rise time are due to reflections from the stub bouncing back and forth on the target bus.

The signal at the probe (figure 28) doesn't look quite as bad. Some optimization is possible to improve the signal quality at the receiver at the expense of the signal quality at the probe, but it is unlikely to achieve the desired performance.

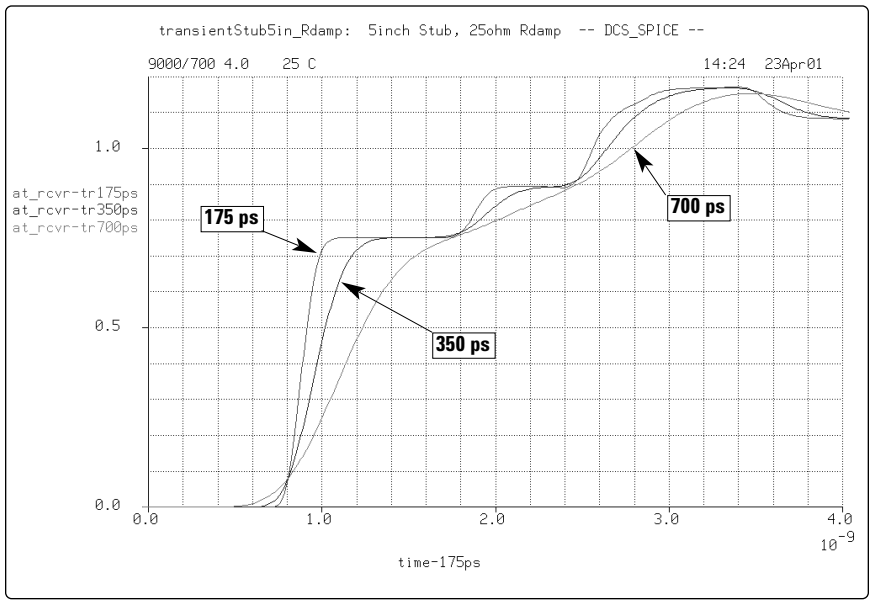

Figure 27. Signal at receiver for 5 inch critically damped stub

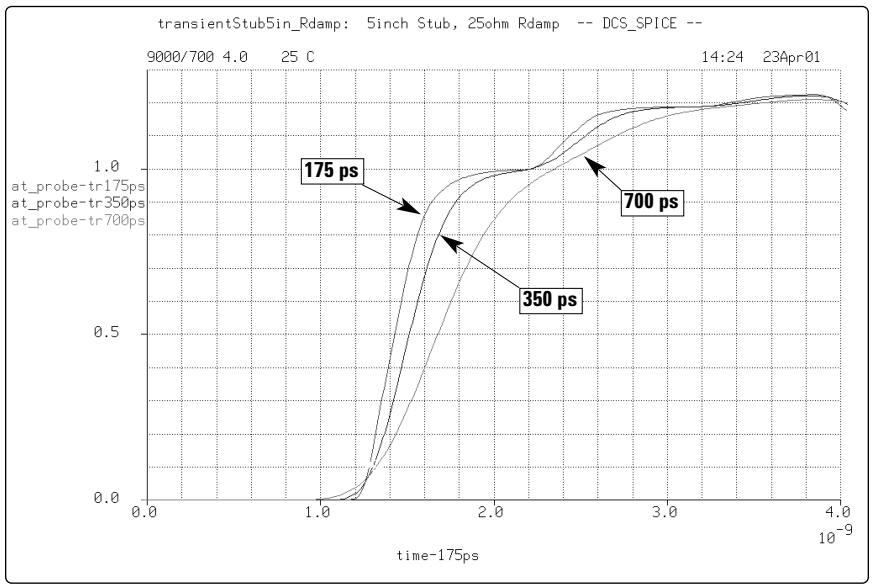

Figure 28. Signal at logic analyzer probe input for 5 inch critically damped stub

Summary of Damped Stub Connection

A stub is not an ideal method of tapping off the target bus for logic analyzer probing. The stub significantly adds to the total equivalent probe load. Even seemingly short stub lengths can dominate the total equivalent probe load. For systems with fast rise times, the total load introduces reflections and steps on edges that can cause the target system to malfunction. Therefore, other probing alternatives are recommended. However, if a stub connection to the probe connector is the only probing solution available, then some optimization can improve the likelihood of successfully probing the target.

One of the few attractive features of a damped stub is that the stubs can be disconnected in the target by simply removing the damping resistor. Here are a few things to keep in mind:

Trace Stub

- Keep the stub length as short as possible.
- Start with a rule of thumb: Tstub ≤ 1/5 system risetime.
- Keep the stub trace impedance as high as possible.
- Make the stub impedance higher than the target impedance.

Rdamp

- Damp the stub with at least the minimum critical damping R = Zstub – 1/2 Ztarget, regardless of stub length.
- Optimize Rdamp using system rise time,stub impedance, and stub length.
- Use simulation to optimize Rdamp to balance the transition times between the probed signal and the receiver signal. Don't over-damp the stub, or the probed signal won't have enough bandwidth to be useful for probing.

Performance

- The "eye" at the probe tip must meet the logic analyzer specs
- Rise time at the probe tip can be estimated as 2.2 x (Rdamp + 1/2 Ztarget) x (Cstub + Cconnector)
- Bandwidth can be estimated as 1/(2 x pi x (Rdamp + 1/2 Ztarget) x (Cstub+Cconnector))
- For stubs that are shorter than 1/5 of the signal rise time, an estimate of the rise time seen by the receiver can be made using

Cload = Cstub + Cconnector
Zdrive = 1/2 Ztarget
Tfilter = 2.2 x Zdrive x Cload
Trcvr = SQRT ($Trise^2$ + $Tfilter^2$)

Resistive Divider

An alternative to using a damped stub is to turn the stub into a portion of a resistive divider with a transmission line segment. By terminating the stub at the connector end into the stub's characteristic impedance, the capacitive load effects are replaced by a DC load that is virtually flat over frequency. At first glance, this may appear to have some undesirable consequences. But before dismissing the idea, consider some of the following points.

- A resistive divider connection can have extremely high bandwidth. This solution is similar in bandwidth and probe load to a scope resistive divider probe, such as an Agilent 54006A 6 GHz oscilloscope probe.
- The 16760A logic analyzer is much more sensitive than other logic analyzers. With 250 mVp-p (200 mV differential) minimum input swing at the logic analyzer probe tip, a system using 1V ECL signals can be divided down 4:1 and the logic analyzer would still acquire data reliably.
- In low-impedance load terminated systems, a constant resistive load may be a much better solution than the capacitive load of trace stubs and the probe connector.
- The load presented to the target system is almost purely resistive, therefore non-reactive. Consequently, the disturbance to the signals in the target system will be less frequency-dependent.
- There are no trace-length limits to worry about. All trace lengths behave the same, with the exception of skin-effect and dielectric losses on extremely long traces (greater than 6 inches).
- This is perhaps the best method to use for both load-terminated and source-terminated target buses.

To use a resistive divider connection to the analyzer probe, two basic conditions must be met. First, the target must be capable of sustaining a resistive load (DC) in the neighborhood of 200 to 400 Ω. Second, the target signal swing must be of large enough amplitude to be divided down to the probe and still meet the logic analyzer specs. If these two conditions are met, then a resistive divider connection may be a superior alternative to a damped stub.

In general, the following guidelines apply:

1. Design the connector stub trace impedance to be as high as possible (higher than target bus is desired).
2. Terminate the stub trace with Rterm at or after the connector such that Rterm = Z0, the characteristic impedance of the stub trace.
3. Determine the maximum divider ratio so that at least a 250 mV signal swing appears at the probe tip (200 mV if differential).
4. Calculate the tap resistor value = N x Rterm, where N = Divider Ratio - 1.

Advantages of a resistive divider over a damped stub:

- Rtap can be a substantially higher value in the resistive divider connection compared to Rdamp in a damped stub.
- The length of the line between the bus and the connector can be much longer than for a damped stub.
- Rterm terminates the stub line and substantially reduces the capacitive load effects of the probe. There is no reflection from the end of the stub.

Disadvantages of a resistive divider connection:

- Signal to probe is attenuated, may not be enough signal swing. This solution is not usable unless the signal amplitude in the target is at least 500 mV (for the 16760A).
- DC load attenuates signal amplitude at receiver somewhat (depends on driving impedance).

Example Layout of a Resistive Divider Connection

For illustration purposes, consider the following hypothetical layout of a simple driver, receiver, and probe connector for a single trace (figure 29). The target bus traces are assumed to be surface microstrip construction, yielding a 50 Ω transmission line impedance with 150 ps/inch propagation velocity.

Furthermore, it is assumed that the target PC board material, processes, and design rules can support a 75 Ω trace impedance to the probe connector. For simplicity, the Rterm resistor is shown adjacent to the pin. Ideally, the resistor Rterm would be placed as close as possible after the connector pin to minimize stubs from the termination to the probe connector.

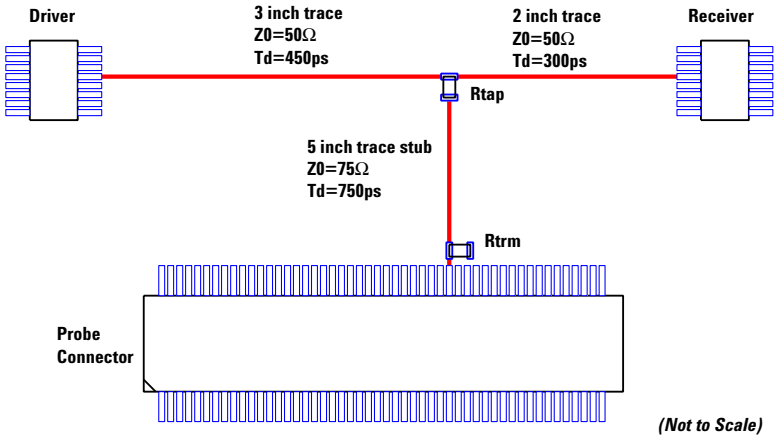

Figure 29. Hypothetical layout with divider connection to probe

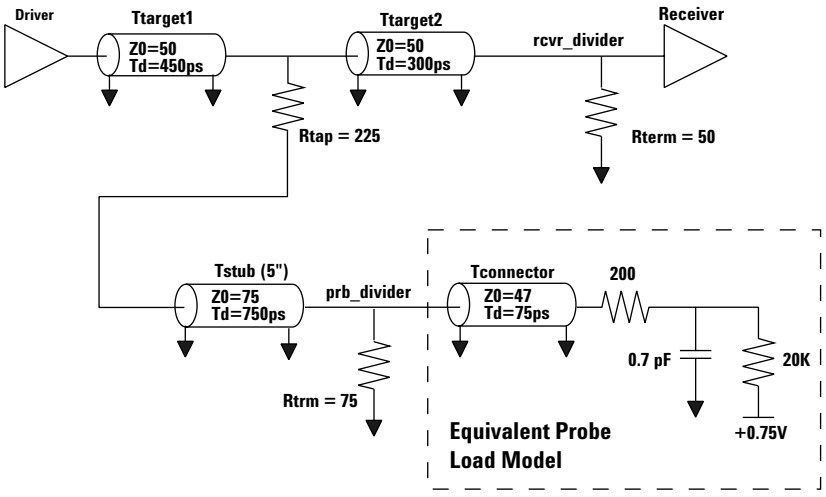

Figure 30. Schematic of the resistive divider solution in figure 29 (hypothetical load-terminated bus with resistive-divider connection to probe)

Determining Total Equivalent Load on Target Bus

The total load on the target bus is no longer dependent on the E5379A equivalent probe load model. Instead, the impedance on the target will behave largely like a DC value. To illustrate this point, the total probing solution as a load is shown in figure 31.

As expected, the equivalent load of the resistive divider connection looks like a resistor at all frequencies (figure 32). The capacitance of the E5379A equivalent load is effectively isolated by this approach.

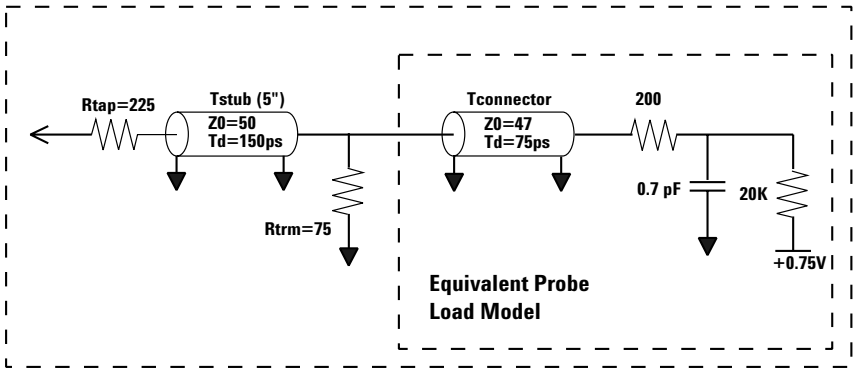

Figure 31. Total load on target bus 4:1 5 inch resistive divider connection

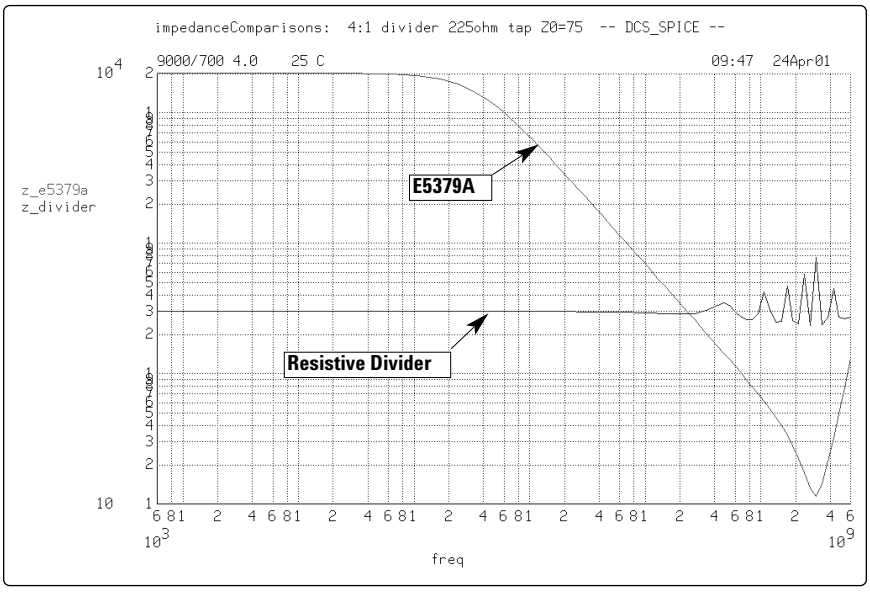

Figure 32. Impedance of resistive divider load on target bus compared to E5379A probe

Determining the Effect on the Target Bus

Using several different driver rise times, the effect of this load on the target can seen in the simulation results in figure 33. The shelf – or flat spot – between 1 and 2 ns is caused by a slight mismatch in impedance where the resistive divider probe taps off. For this simulation, the driver impedance is assumed to be 7 Ω. A small reflection is created at the resistive divider tap, which travels back down towards the receiver, and re-reflects off the receiver because the receiver isn't terminated into Z0 of the target. That re-reflection off the driver has to travel down the trace called Target1 and back, so it shows up at the receiver 2 x 450 ps = 900 ps after the initial edge. For the 700 ps rise time example, this round-trip reflection is too short to show up as a shelf.

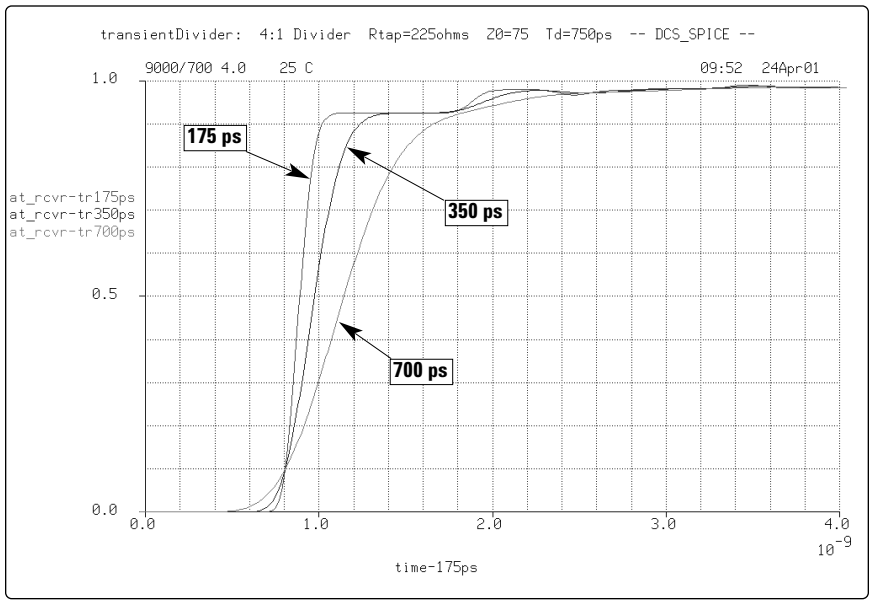

Figure 33. Signal at receiver, resistive divider solution

This is a much better looking signal at the receiver than any of the damped-stub methods could provide. The rise times of the system are preserved, and the distortion on the signal is less than 10 percent of the total amplitude. The distortion is due to the impedance mismatch caused by the resistive divider tap. For this example, the resistive divider tap is a 300 Ω impedance, in parallel with the target bus of 50 Ω, resulting in a 43 Ω impedance in a 50 Ω system. For other implementations, the discontinuity might be smaller or larger, depending on the target bus impedance, the divider ratio, and the divider trace impedance.

Any reflections internal to the resistive divider trace are attenuated by the ratio of Rtap to 1/2 Ztarget. For this example, the reflections are attenuated by 225 Ω into 25 Ω, which is 10:1, or 10 percent. So, a 10 percent reflection on the divider trace will be manifested as a 1 percent perturbation on the target bus.

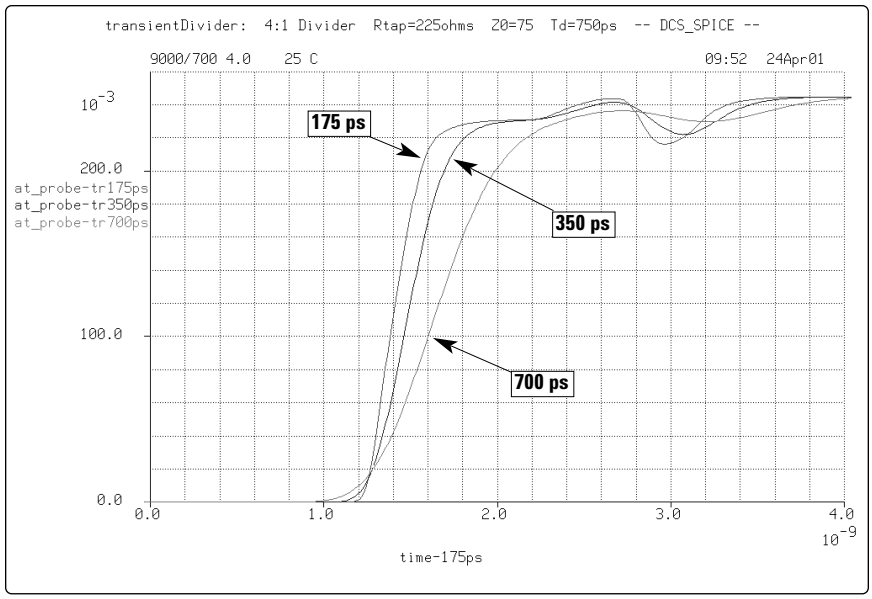

Figure 34. Signal at logic analyzer probe input for resistive divider

Determining the Effect at the Analyzer Probe Tip

The signal at the logic analyzer probe tip suffers from some distortions. The capacitance of the connector causes a reflection on the divider trace. This reflection re-reflects off the 225 Ω Rtap resistor at the target bus, and shows up 2 prop delays of the divider trace later at the probe tip (see figure 34).

Optimizing for Load Terminated Buses

Option 1: Move the resistive divider tap as close to the driver as possible (figure 35), thereby minimizing or eliminating the reflections from the impedance discontinuity caused by the resistive divider connection.

The signal at the receiver (figure 36) is flattened, with no “shelf” or “step” caused by the impedance discontinuity. However, there is still a slight attenuation of the signal amplitude, which may or may not be a problem.

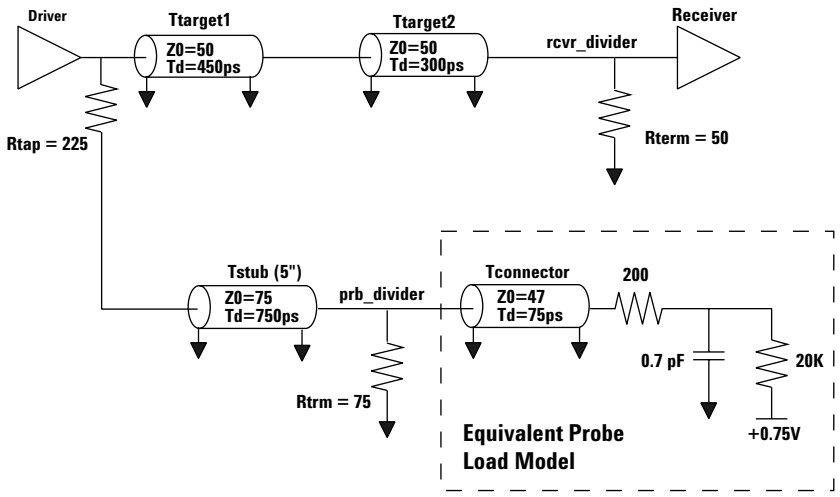

Figure 35. Schematic of a load-terminated bus with resistive divider tap at the driver

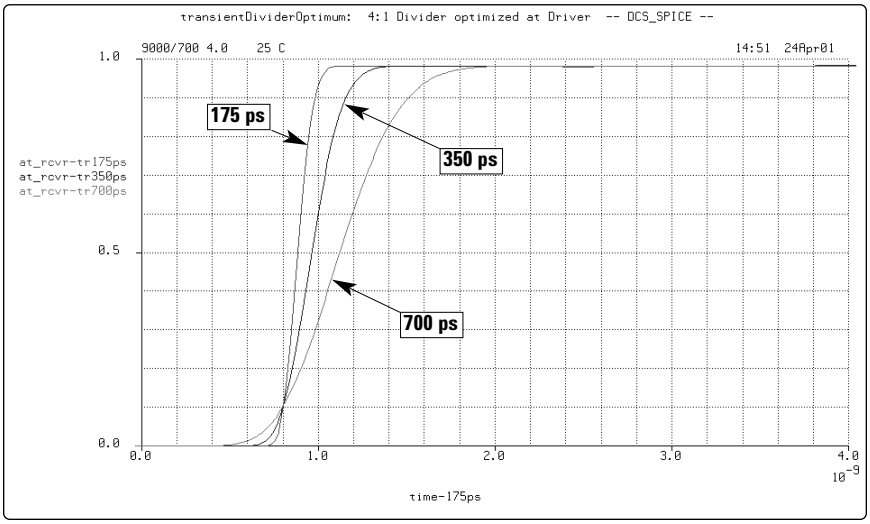

Figure 36. Simulation results of signal at receiver for resistive divider, tap connected at driver

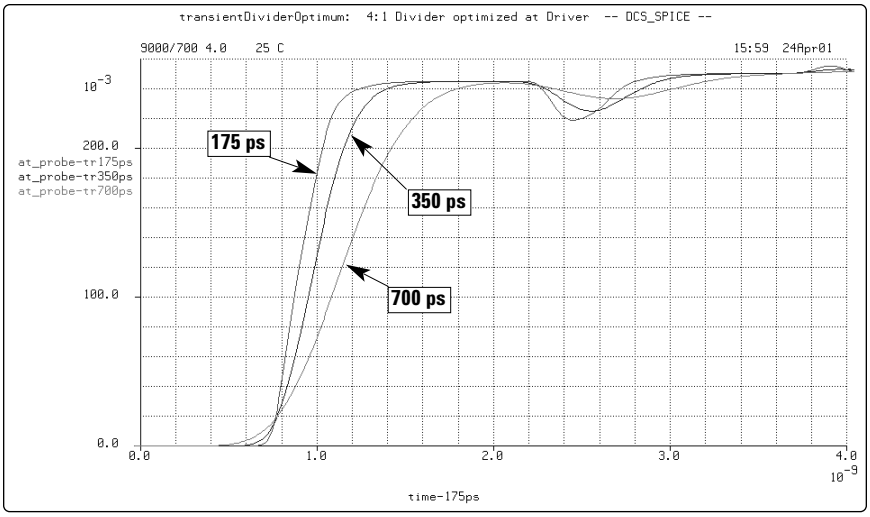

Figure 37. Simulation results of signal at logic analyzer probe input for resistive divider, tap connected at driver

Option 2: Move the resistive divider tap as close to the receiver as possible (figure 38). Then adjust Rterm, the target termination, so that Rterm in parallel with (Rtap+Zdivider) = Ztarget. For the example underway, this change to the target is shown in figure 40.

This option not only minimizes or eliminates the reflections from impedance discontinuities, but it also eliminates the voltage attenuation. The big drawback to this solution is that the target must be modified. On the other hand, the parallel combination of the new Rterm and the resistive divider matches the target Z0, so it is conceivable that the resistive divider could become a permanent part of the design.

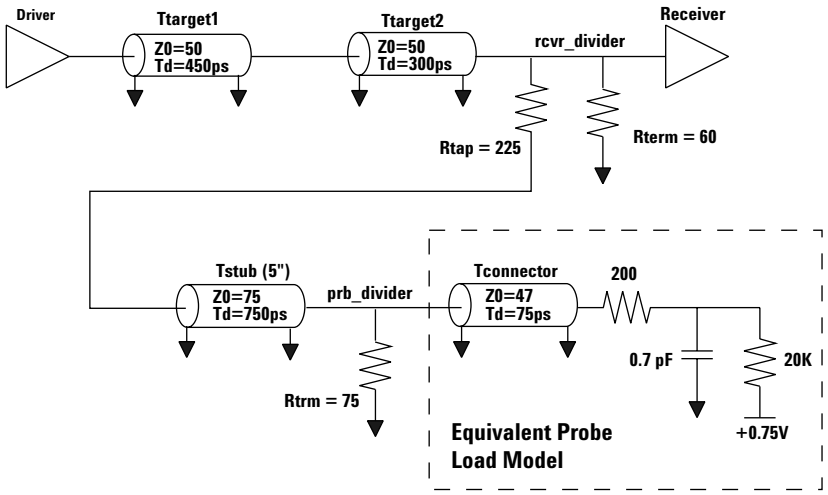

Figure 38. Load-terminated bus with resistive divider tap located at the receiver

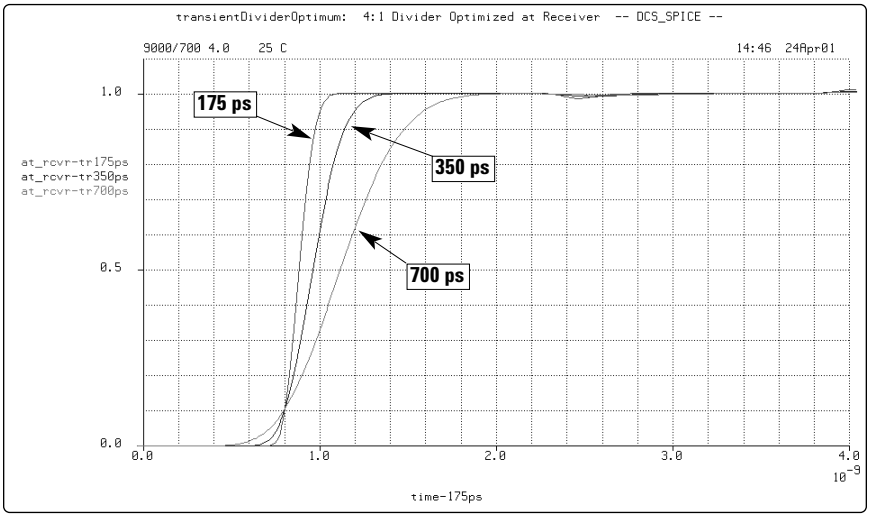

Figure 39. Simulation results, signal at the receiver, load-terminated bus, resistive divider tap located at the receiver

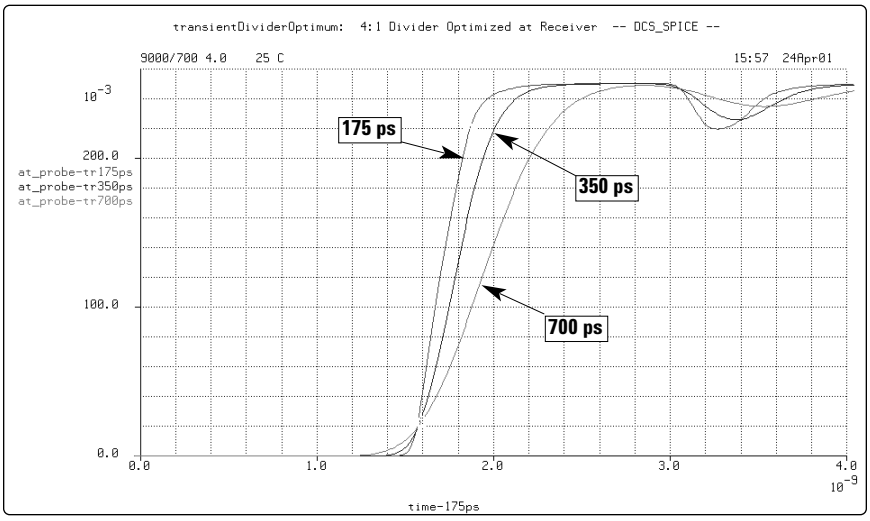

Figure 40. Simulation results, signal at the logic analyzer probe input, load-terminated bus, resistive divider tap located at the receiver

Optimizing for Source-Terminated Buses

Not all high-speed systems are designed with load-terminated buses. A resistive divider probe connection is one of the few alternatives for connecting to a source-terminated bus. To evaluate the resistive divider probe, consider a slight modification to the example schematic (figure 41). Instead of terminating the target bus at the receiver, the bus is source-terminated at the driver. In this case, Rtap MUST be placed as close to the receiver end of the bus as possible. See the section "Source-Terminated Buses" on page 30.

The equivalent probe load on the target is the same as for the load-terminated bus. However, the signal at the receiver and probe tip needs to be re-evaluated.

Note: Always probe as near as possible to the receiver end of the line for source-terminated buses! Attenuation is more severe on the source-terminated bus because the source impedance is 50 Ω instead of 7 Ω for the example given for load-terminated buses. However, the signals are clean and flat at the receiver, and have enough bandwidth at the probe to be useable.

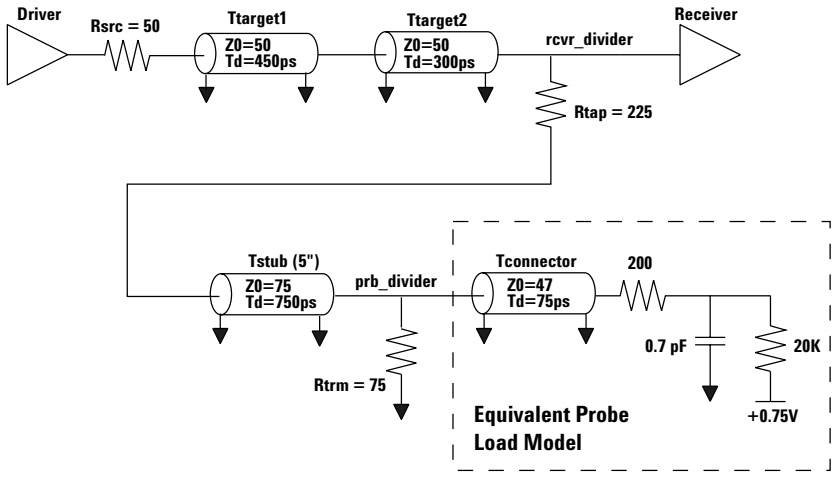

Figure 41. Schematic of a source-terminated bus, resistive divider tap located near the receiver

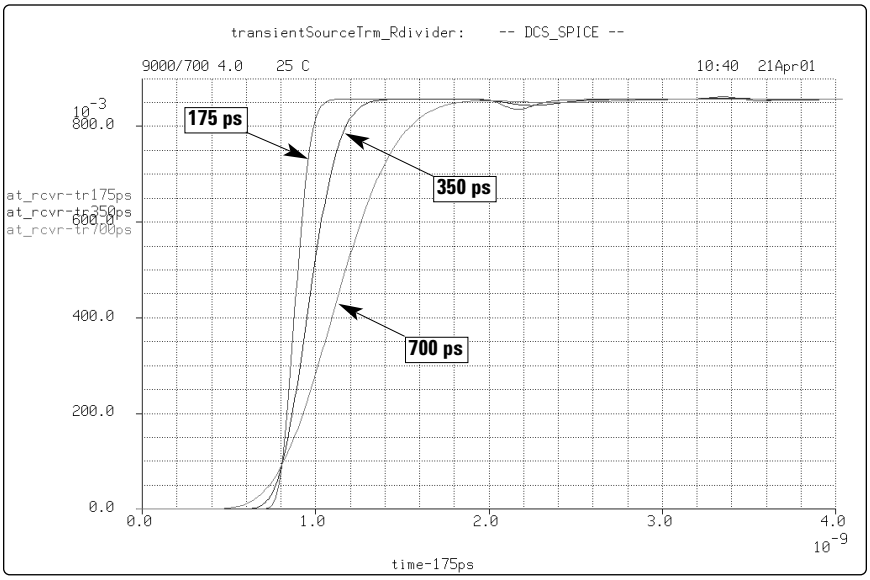

Figure 42. Simulation results, signals at the receiver, source-terminated bus, resistive divider solution with tap located at the receiver

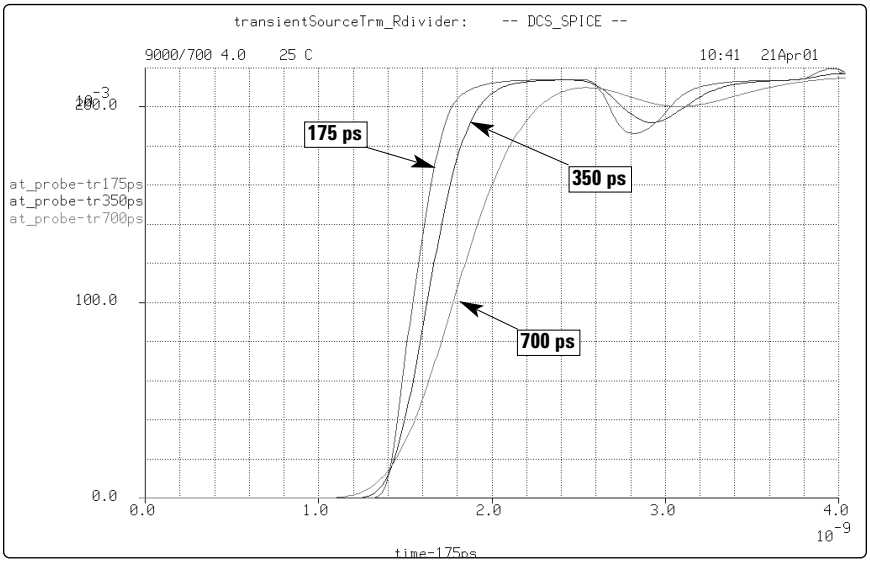

Figure 43. Simulation results, signals at the logic analyzer probe input, source-terminated bus, resistive divider solution with tap located close to the receiver

Summary of Resistive Divider Connection

Requirements to use a resistive divider connection:

1. The target must have enough signal amplitude to allow a resistive divider connection to attenuate the signal to the probe and still meet the logic analyzer specs.
2. The target must have enough tolerance in the amplitude specs of the receiver to tolerate the attenuation of the signal on the bus. (Note: it may not be necessary to give up any signal amplitude on the target bus if the tap resistor can be designed as part of the termination for the transmission line.)

Resistive divider connection design:

1. Design the divider-tap trace to be as high impedance as possible.
2. Terminate the divider trace Tdivider into its characteristic impedance at the probe connector.
3. Select as high a divider ratio as possible that still meets the logic analyzer minimum signal swing specs.
4. Rtap = (Divider Ratio - 1) x Zdivider

Placement of Rtap on the target bus:

1. For load-terminated buses, tap off at the driver, or as close to the driver as possible.
2. For source-terminated buses, tap off at the receiver, or as close to the receiver as possible.
3. For source-AND-load terminated buses, it really doesn't matter. Signal fidelity is the same everywhere.

Benefits of using a resistive divider connection:

1. Maximum bandwidth on target bus with probe in place (least distortion on rise/fall times)
2. Flattest signal response at target receiver
3. System performance is nearly unaffected with or without probe attached
4. Production can ship with design in place, or simply no-load the tap resistors

Thevenin Equivalent Resistive Divider

An interesting variation on the resistive divider approach is to modify the target load termination such that the resistive divider becomes part of the target termination. The basic approach is to adjust the target load termination and/or set the resistive divider elements such that the two in parallel make a Thevenin equivalent impedance that properly terminates the target bus.

This approach only works for load or source/load terminated systems, and requires modifications to either the target load termination or the target trace impedance. However, when utilized, this approach minimizes the probe load on the target, thus maximizing the target bandwidth. It also substantially reduces reflections on both the signal seen at the target receiver and the signal seen at the probe tip. This approach has the additional benefit of potentially providing a larger signal to the probe tip, depending on the values chosen for the resistive divider. Remember that whatever resistive divider ratio is chosen it must provide a signal at the probe tip that meets the logic analyzer specifications.

All of the resistive divider benefits still apply, that is to say that a resistive divider probe has high bandwidth, the length of the trace used for the resistive divider can be arbitrarily long, and the load on the target is non-reactive. If the target system has the flexibility to adjust either the target load termination or the target trace impedance, and the resistive divider probe is attached at the load termination, then the Thevenin equivalent approach is a better approach than a simple resistive divider probe.

However, note that the divider probe tap must always be loaded, even in production boards, to maintain a proper termination. The probe connector itself does not need to be loaded, but the resistive divider tap does because it has become an integral part of the target system.

In general, the following design guidelines apply:

Case 1: Target load termination is adjusted to match a fixed target trace impedance.

1. Determine the target trace impedance Z0
2. Determine the probe divider trace impedance Zdivider
3. Determine N, the maximum divider ratio that still meets spec for the logic analyzer
4. Rtap for the divider = (N-1) x Zdivider
5. Rterm for the divider trace = Zdivider
6. Calculate Rload of the target = 1/[1/Z0 - 1/(N x Zdivider)]
7. Set Rload of target to be 2 x Z0 of trace
8. Place logic analyzer probe at or near Rterm

Example

Suppose Z0 = 50 Ω, and Zdivider = 50 Ω.

Furthermore, the maximum divider ratio N=2.

Therefore, Rtap = 50, Rterm = 50, and Rload = 100.

You now have the values for a target with a 50 Ω trace impedance that is terminated into 50 Ω, with a 2:1 resistive divider probe at the load termination.

This example will be evaluated in the discussion on the following pages.

Case 2: Target trace impedance is adjusted to match a fixed target load in parallel with Zdivider.

1. Determine Rload, the load termination for the target bus
2. Determine Zdivider, the probe divider trace impedance. Higher impedance is probably desirable
3. Determine N, the maximum divider ratio that still meets spec for the logic analyzer
4. Rtap = (N-1) x Zdivider
5. Rterm for the divider trace = Zdivider
6. Calculate the desired target bus impedance = 1/[1/Rload + 1/(N x Zdivider)]
7. Place logic analyzer probe at or near Rterm

Example

Suppose Rload=50, and Zdivider = 75. Furthermore, the maximum divider ratio N=4.

Therefore, Rtap=225, Rterm =75, and Z0 calculates out to roughly 43 Ω.

Layout of a Thevenin Equivalent Resistive Divider Connection (Case 1)

For illustration purposes, consider the hypothetical layout in figure 44 of a simple driver, receiver, and probe connector for a single trace. The target bus traces are assumed to be surface microstrip construction, yielding a 50 Ω transmission line impedance with 150 ps/inch propagation velocity. Furthermore, it is assumed that the divider trace is also 50 Ω impedance. For simplicity, the Rterm resistor is shown adjacent to the pin. Ideally, the resistor Rterm would be placed after the connector pin to minimize stubs from the termination to the probe connector.

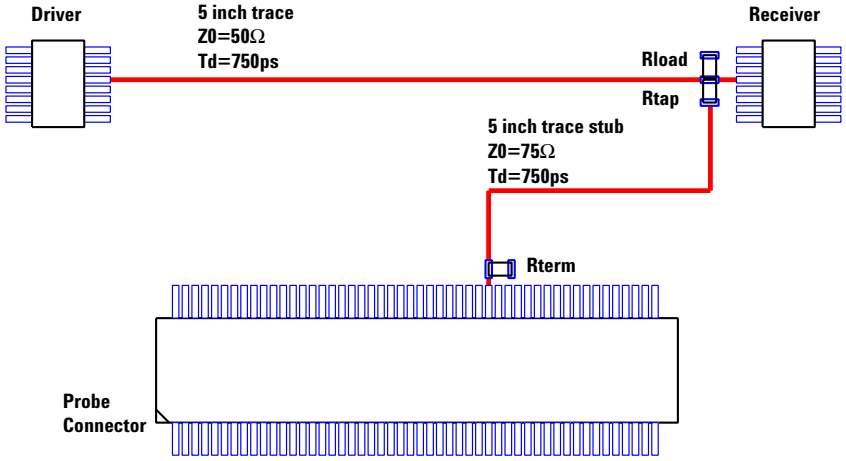

Figure 44. Layout of a Thevenin equivalent resistive divider connection

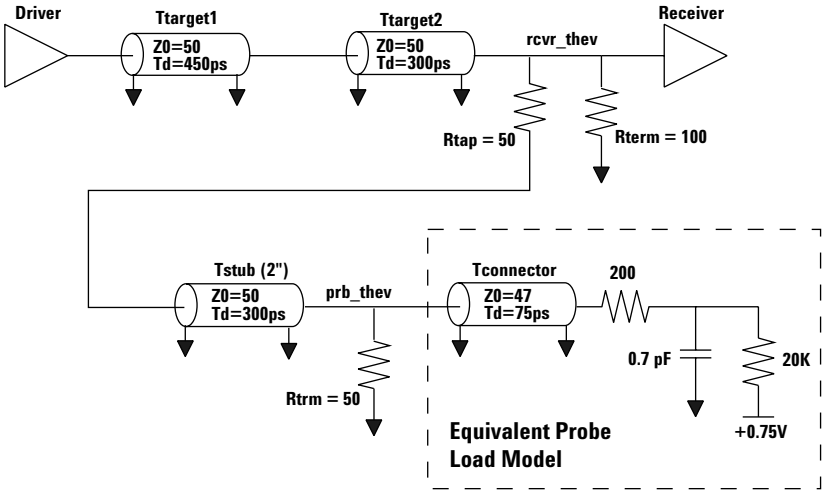

Figure 45. Schematic of a Thevenin equivalent resistive divider connection

Determining Total Equivalent Load on Target Bus

The comparison to be made is between an ideal 50 Ω load and the new Thevenin equivalent divider load. The Thevenin equivalent resistive divider load includes the new value for Rload. Hopefully, this would look just like an ideal 50 Ω termination on the bus.

As expected, the equivalent load termination using the Thevenin equivalent resistive divider approach looks like a resistor at all frequencies. The capacitance of the E5379A equivalent load is effectively isolated by this approach.

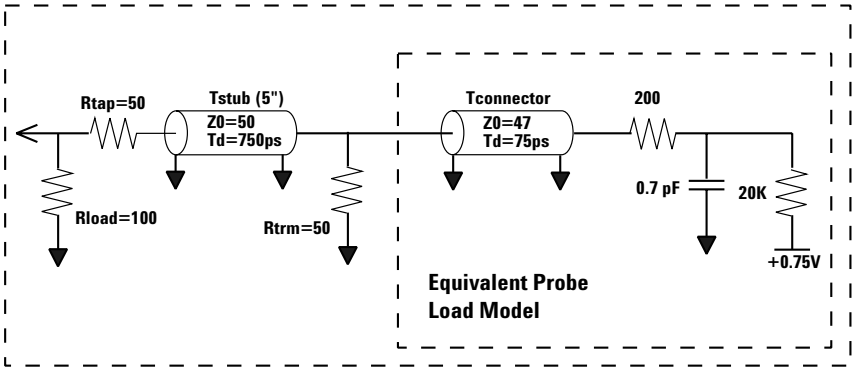

Figure 46. Simplified schematic showing the equivalent load on the target bus for a Thevenin equivalent resistive divider connection

Determining the Effect on theTarget Bus

Using several different driver rise times, the effect of this load on the target is seen in the simulation results in figure 48. Note that there is virtually no degradation in rise times, and that the effect of the probe load is isolated such that for this 2:1 divider example, the reflections are ≤ 5 percent.

This yields a much better looking signal at the receiver than would be realized with either a damped stub method or by placing the probe load directly on the bus. Even compared to a resistive divider approach using a 5 inch stub, the signal is improved.

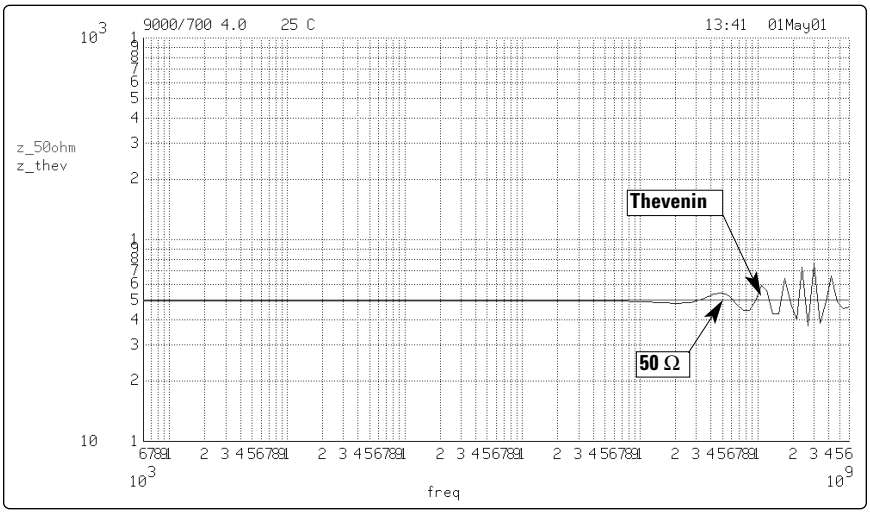

Figure 47. Impedance of equivalent load on target bus, Thevenin equivalent resistive divider connection

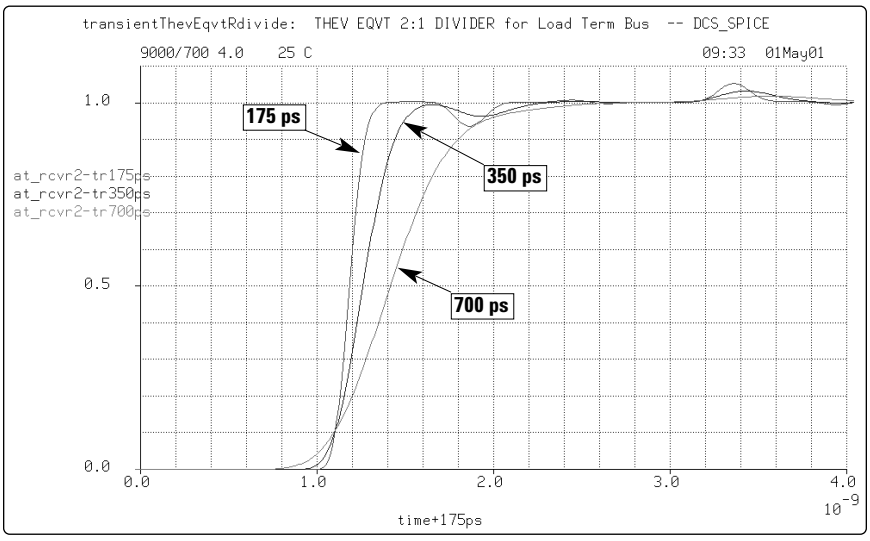

Figure 48. Signals at receiver for different rise times, Thevenin equivalent resistive divider connection

Determining the Effect at the Analyzer Probe Tip

The signal at the logic analyzer probe tip, figure 49, manifests some distortions. The capacitance of the connector causes a reflection on the divider trace. This reflection re-reflects off the 50 Ω Rtap resistor at the target bus, and shows up 2 prop delays of the divider trace later at the probe tip.

Still, the signal integrity at the probe tip is greatly improved compared to other approaches. Again, compared against a resistive divider connection with a 5 inch trace, the signal on the Thevenin equivalent approach is improved. It has larger amplitude, faster rise times, and smaller reflections.

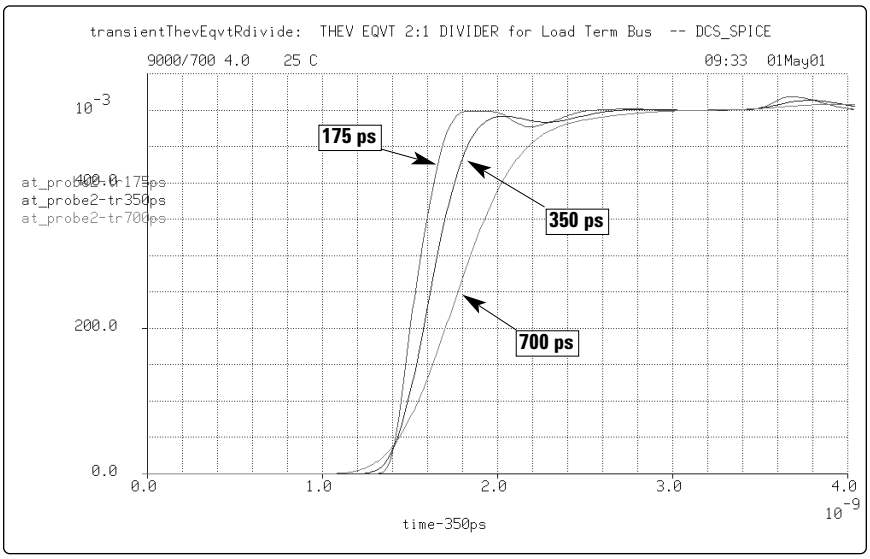

Figure 49. Signals at logic analyzer probe input, Thevenin equivalent divider connection

Probing Location

Load-Terminated Buses

A hypothetical load-terminated transmission line system is illustrated in figure 50. Three potential probing points have been indicated, for probing at the driver, somewhere in the middle of the trace, or at the receiver. Each of these cases has been simulated with the E5379A equivalent load model inserted at the indicated places. To illustrate what it means to add the probe load, figure 50 shows the probe load inserted at the driver.

There are two nodes of concern for this simulation. The first, always on the mind of the designer, is what effect the probe load has on the signal at the target receiver. The second, easily overlooked, is the signal at the probe tip. If the signal at the probe tip does not meet the minimum logic analyzer specs, there is little or no point in connecting to a logic analyzer. Therefore, these simulations will evaluate the effect of probe position on the signal at both the receiver and the probe tip.

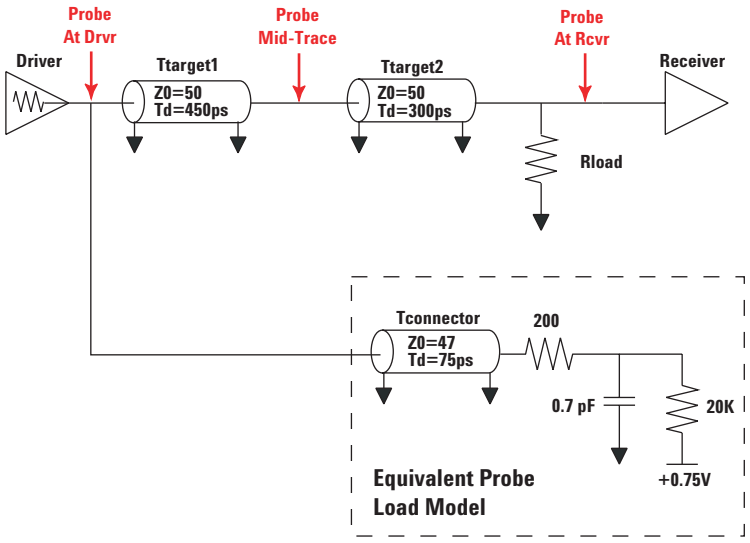

Figure 50. Schematic of a load-terminated system showing various probing locations

Load-Terminated Bus Summary

The probe load, no matter how it is implemented, will cause an impedance mismatch in the target system at the tap point for the probe. For load-terminated systems, the effects of the probe load can be minimized by locating the probe tap at the target driver. If the connector is placed directly on the bus, a damping resistor may be used in series with the probe connector to reduce the reflections on the target bus.

Load-Terminated Bus, Probed at the Driver

The simulation results for a load-terminated target system, probed with a logic analyzer at the driver, show that the signal at both the target receiver and the probe tip are identical except for the absolute time when the bus transitions occur. There is little or no degradation of the rise times. The step responses are flat, with no reflections on the bus.

Thus we can conclude that as close as possible to the driver is the ideal location to probe a load-terminated bus in terms of signal fidelity. It may be difficult to physically position the probe connector at the target driver output. Damped stub connections or resistive divider connections may make this more feasible. As the connector moves farther from the driver, reflections from impedance discontinuities (or mismatches) caused by the probe load will become more apparent.

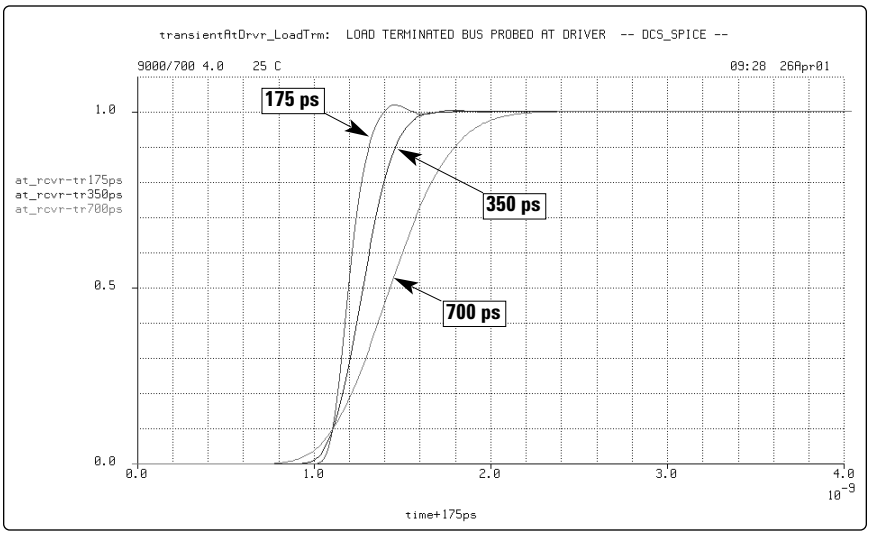

Figure 51. Signals at the receiver, load-terminated bus probed at the driver

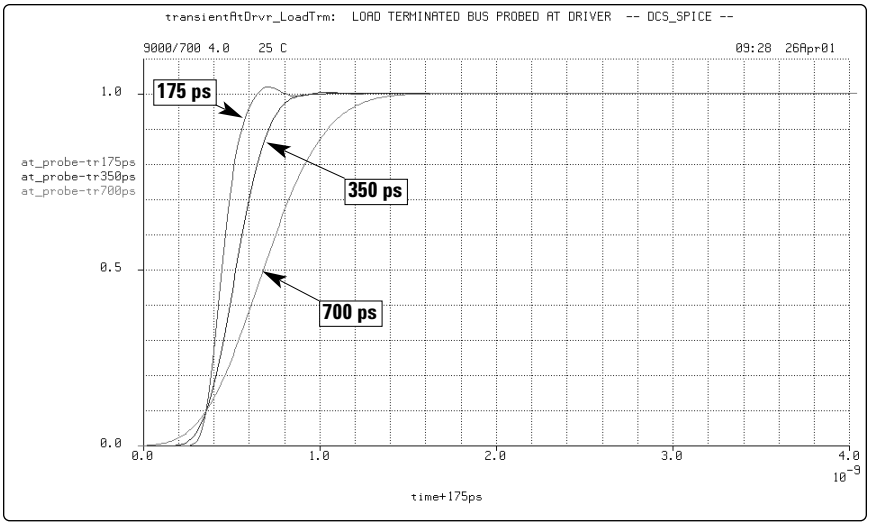

Figure 52. Signals at the logic analyzer probe input, load-terminated bus probed at the driver

Load-Terminated Bus, Probed in the Middle of the Target Trace

The reflections in this simulation are due to the impedance discontinuity caused by the probe load. The impedance discontinuity causes a reflection to travel back toward the driver. Because the driver impedance is not matched to the transmission line impedance, the driver re-reflects the signal back toward the receiver. A smaller secondary reflection is generated at the probe load from the first re-reflection. This mode of reflection and re-reflection continues with diminishing amplitude until the reflections effectively die out. The time interval between incident edge and the first reflection is set by the electrical length of the trace between the target driver and the probe load, Td1. The reflection must travel down the trace segment Target1 and back, so the reflection shows up 2 x Td1 after the incident edge, which in this example is 900 ps later. All subsequent re-reflections show up at 900 ps intervals.

Note that if the probe load were placed close enough to the driver, the reflection would show up in the rise time of the signal, and possibly cause the rising edge to have a flat spot in it, or at least appear as a slower rise time.

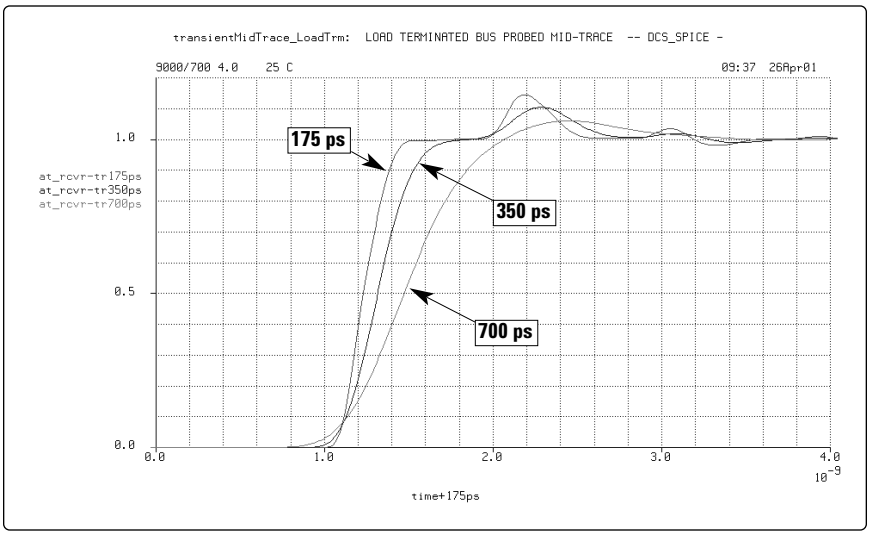

Figure 53. Signals at the receiver, load-terminated bus probed in the middle of the target trace

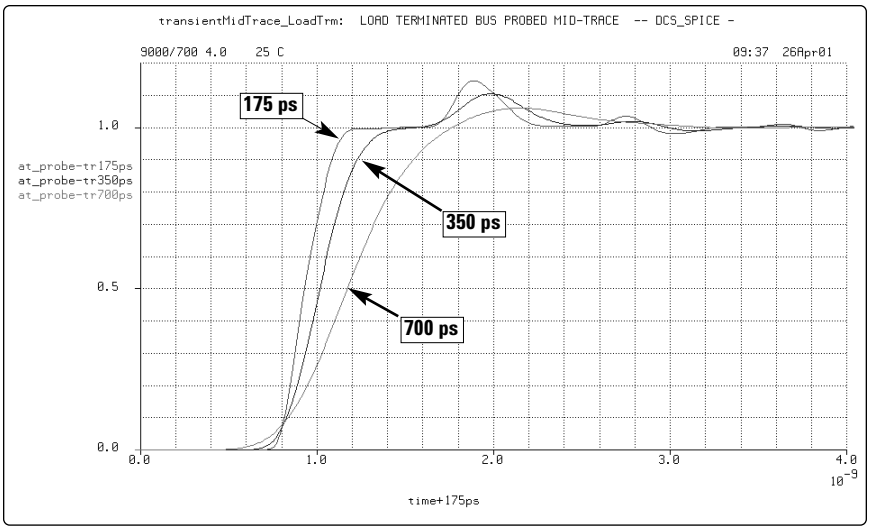

Figure 54. Signals at the logic analyzer probe input, load-terminated bus probed in the middle of the target trace

Load-Terminated Bus, Probed at the Receiver

Here again the probe load has introduced an impedance discontinuity, sending a reflection back toward the driver. The time interval between incident edge and reflection is now set by the total length of the target bus. The total length of the example target bus was 450 ps + 300 ps = 750 ps. Therefore, reflections (and subsequent re-reflections, which are not shown on the simulation plots) occur at 1.5 ns intervals.

The primary advantage of probing directly at the receiver is that both the probe and the receiver see identical waveforms, both in time and voltage.

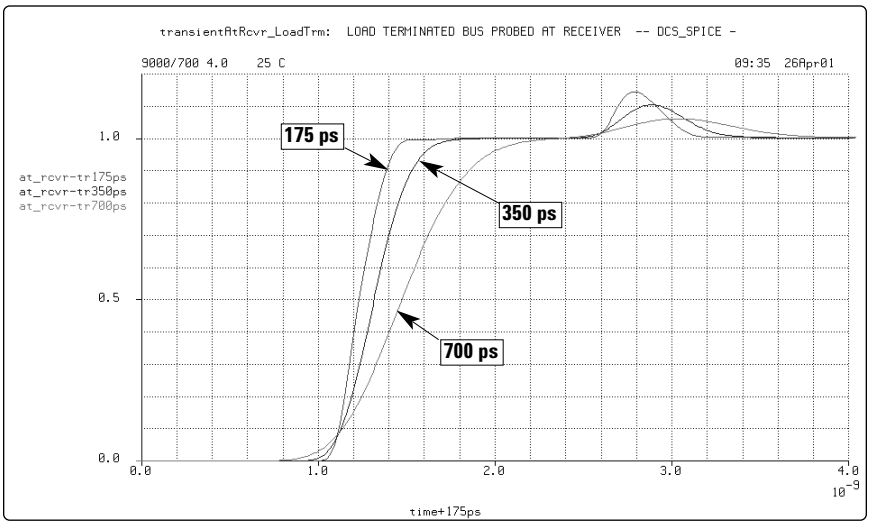

Figure 55. Signal at the receiver, load-terminated bus, probed at the receiver

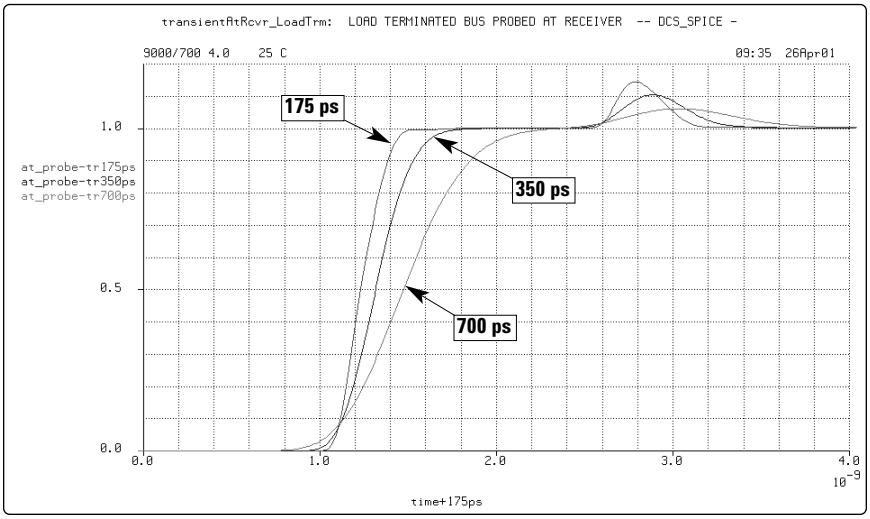

Figure 56. Signal at the logic analyzer probe input, load-terminated bus, probed at the receiver

Load-Terminated Bus, Probed After the Receiver

In this example, the target bus is extended by an additional 300 ps beyond the receiver. The probe load is at the end of this extension, and the target load-termination has also been moved to the end of the trace. This may not be possible for all systems because some receiver devices have bus terminations integrated on-chip.

Now, for the first time, the receiver device is seeing the reflection off the probe load before it is re-reflected. Because the probe load looks capacitive, and thus a lower impedance than the target trace, the reflection is in the opposite direction of the incident edge. When the reflection encounters the driver, it too is a lower impedance than the target trace, so the re-reflection polarity is again reversed. Both the initial reflection back toward the driver and the re-reflection off the driver are shown for the signal at the receiver.

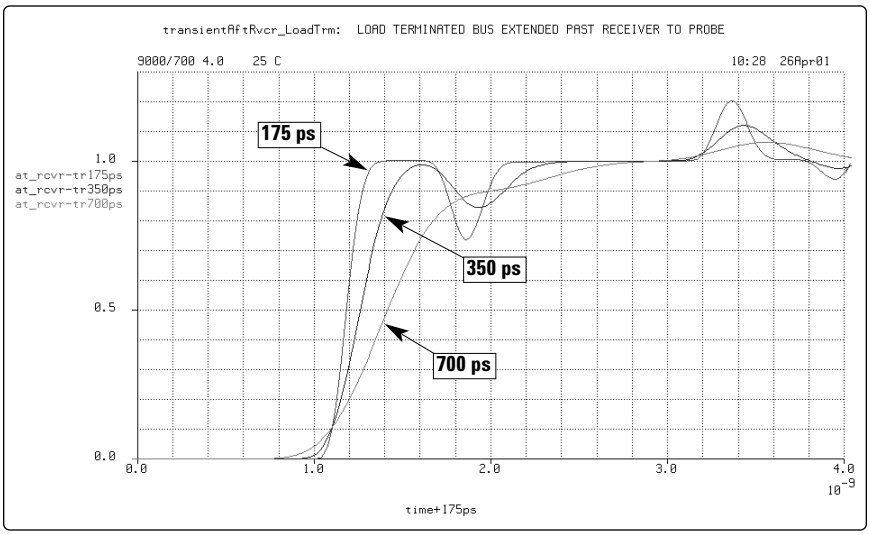

Figure 57. Signal at the receiver, load-terminated bus, probed after the receiver

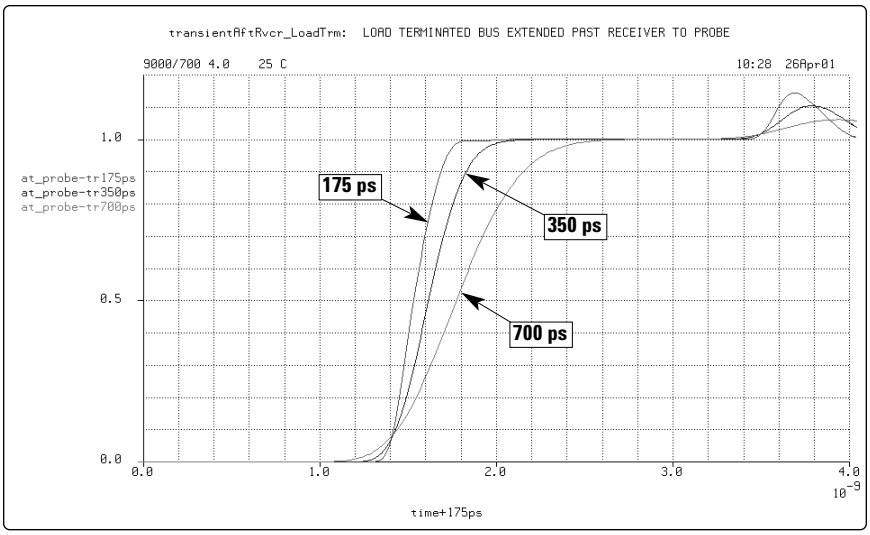

Figure 58. Signal at the logic analyzer probe input, load-terminated bus, probed after the receiver

Source-Terminated Buses

A hypothetical source-terminated transmission line system is illustrated in figure 59. Three potential probing points have been indicated, for probing at the driver, somewhere in the middle of the trace, or at the receiver.

Each of these cases has been simulated with the E5379A equivalent load model inserted at the indicated places. Figure 59 shows the probe load inserted at the driver.

A source-terminated bus is the hardest to probe because the restraints on effective probing solutions don't allow many alternatives. It is undesirable to degrade the signal integrity on the target system, yet the signal at the logic analyzer probe tip must have enough signal integrity to meet the logic analyzer specs. Fortunately, many source-terminated buses also tend to operate at slower clock rate, so some degradation of the signal at the probe tip might be tolerable.

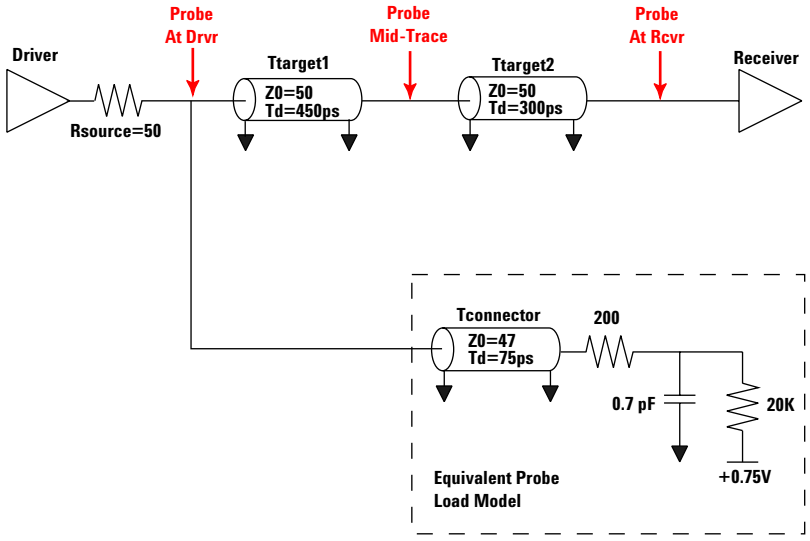

Figure 59. Schematic of a source-terminated bus with various probing points indicated

Source-Terminated Bus Summary

The only place a source-terminated bus can effectively be probed is at or very near the receiver. The following simulations of the probe points mentioned above will illustrate why. As the simulations will show, any substantial deviation from this location results in a severely degraded rise time at either the probe or the receiver or both. Realizing that placing a probe connector right at the target receiver might be physically impossible, a resistive divider approach may be preferable for connecting the probe to the target bus.

Note: No matter how the probe connection is made, the connection to a source-terminated bus MUST be made at or very near the target receiver.

Source-Terminated Bus, Probed at the Driver

The simulation results (figures 60 and 61) for a source-terminated target system, probed with a logic analyzer at the driver, show that the signal at the target receiver is acceptable, but that the signal at the probe tip is not. The “step” at 1 ns and 500 mV in the simulation results is due to the nature of a source-terminated transmission line. A source-terminated transmission line initially reaches half-amplitude on the incident edge, and reaches full-amplitude after the incident edge has reflected from the end of the line and traveled back down the line. The “step” width is simply 2 x Td, the electrical length from the point of observation to the end of the transmission line. As the point of observation is moved closer to the end of the line, the “step” width becomes narrower, until at the receiver end of the line there is no step.

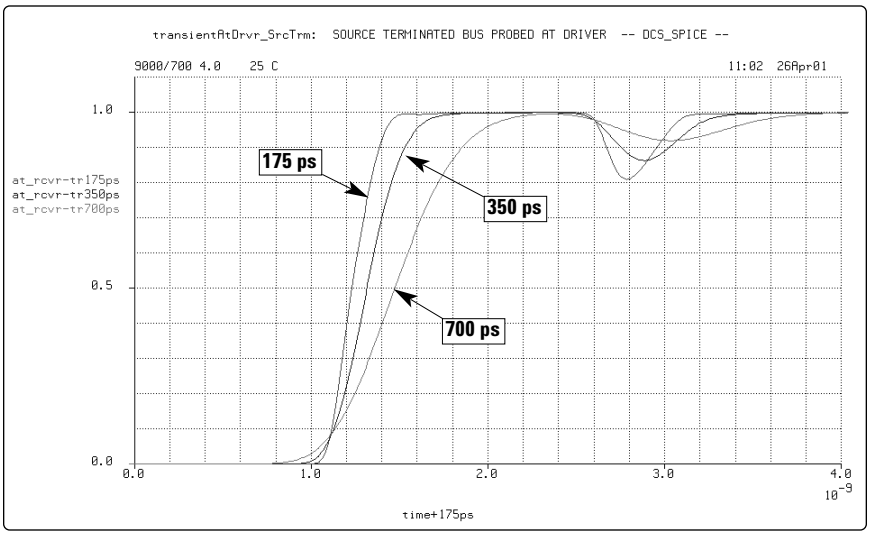

Figure 60. Signal at the receiver, source-terminated bus, probed at the driver

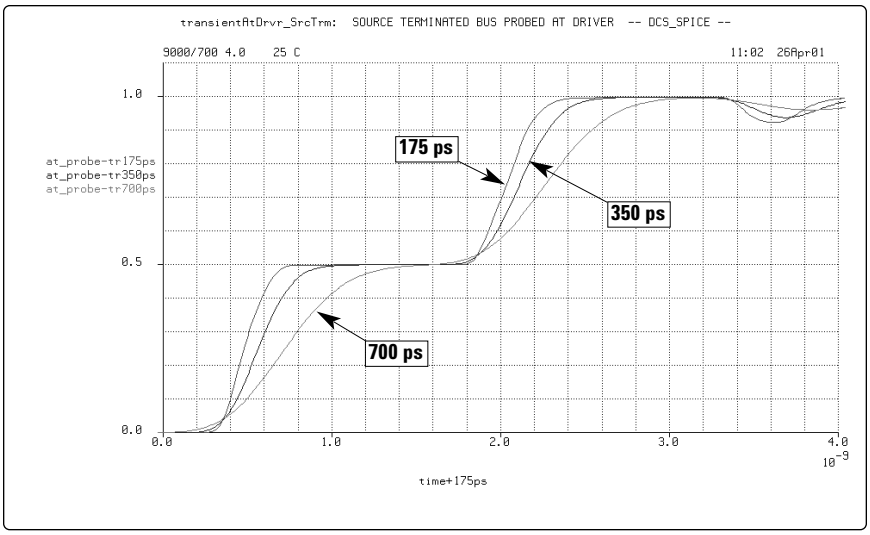

Figure 61. Signal at the logic analyzer probe input, source-terminated bus, probed at the driver

Source-Terminated Bus, Probed in the Middle of the Target Trace

Moving the probe location closer to the end of the transmission line reduces the width of the “step” observed at the probe tip. The “step” may be short enough in time to be absorbed in the risetime. Such is the case for the 700 ps risetime above – instead of seeing a step, the risetime is slower. A “step”, especially on the clock signals, is generally an unacceptable signal at the probe tip. If the “step”is near the threshold, it may cause spurious transitions in the analyzer. However, a slower risetime with a clean transition through the threshold region may be acceptable as long as the timing specs of the logic analyzer are met.

In the simulation in figure 63, the 175 ps trace at the probe tip is still unacceptable as a clock signal, because the time spent dwelling near threshold may very well create a spurious clock as seen by the logic analyzer. The 350 ps trace is marginal, but probably acceptable. The 700 ps trace is fine.

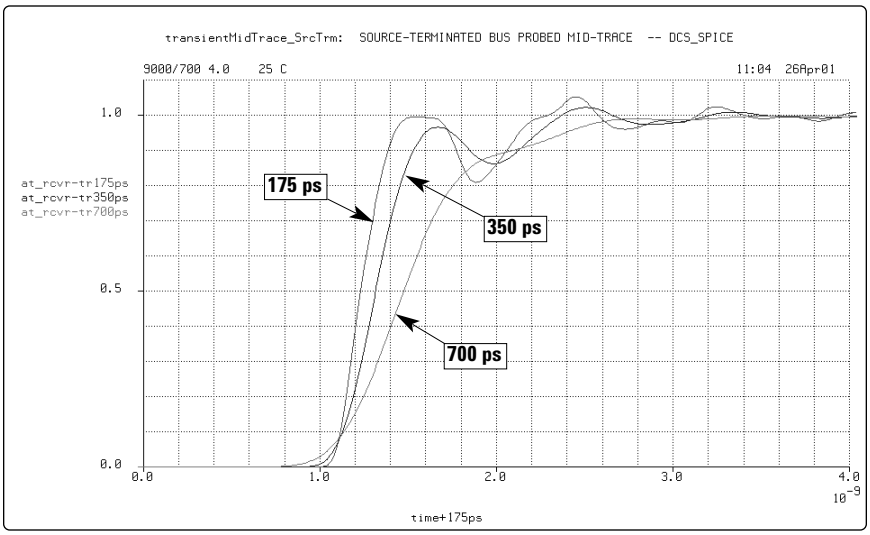

Figure 62 Signal at the receiver, source-terminated bus, probed in the middle of the target trace

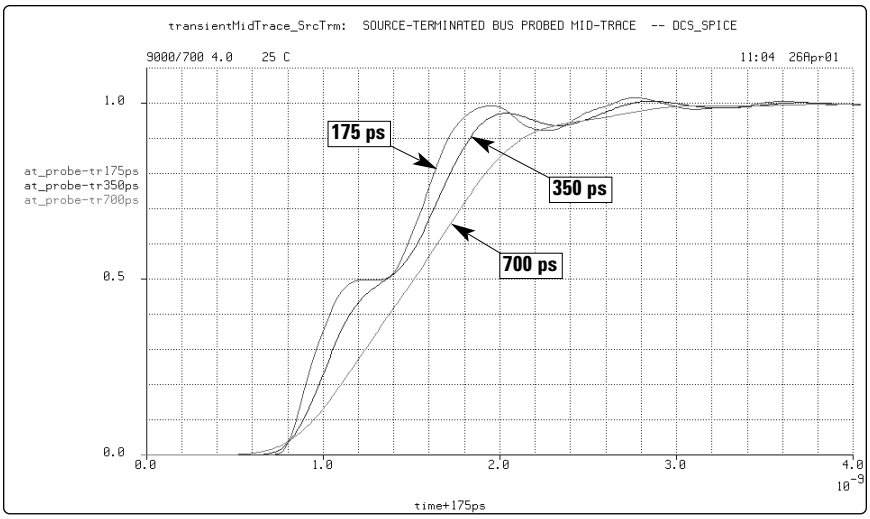

Figure 63 Signal at the logic analyzer probe input, source-terminated bus, probed in the middle of the target trace

Source-Terminated Bus, Probed at the Receiver

This solution best achieves the goal for probing a source-terminated bus. By probing at the receiver, the signal fidelity at both the receiver and the probe tip is as good as it gets. However, physically speaking, it is not always possible to probe at the receiver. Physical space constraints may preclude the placement of the probe tip at the receiver, or even near enough to the receiver to be valuable for probing. A resistive divider probe connection, with the tap made at or as close to the receiver as possible, may be the best solution.

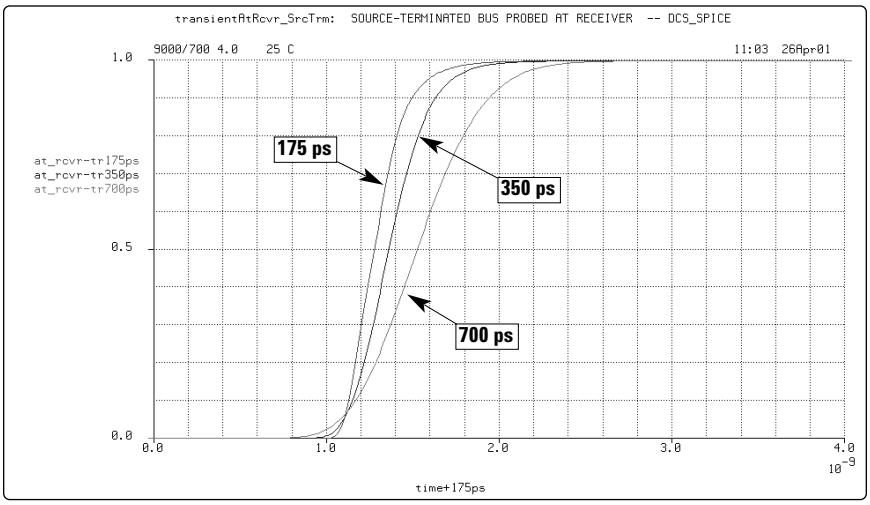

Figure 64. Signal at the receiver, source-terminated bus, probed at the receiver

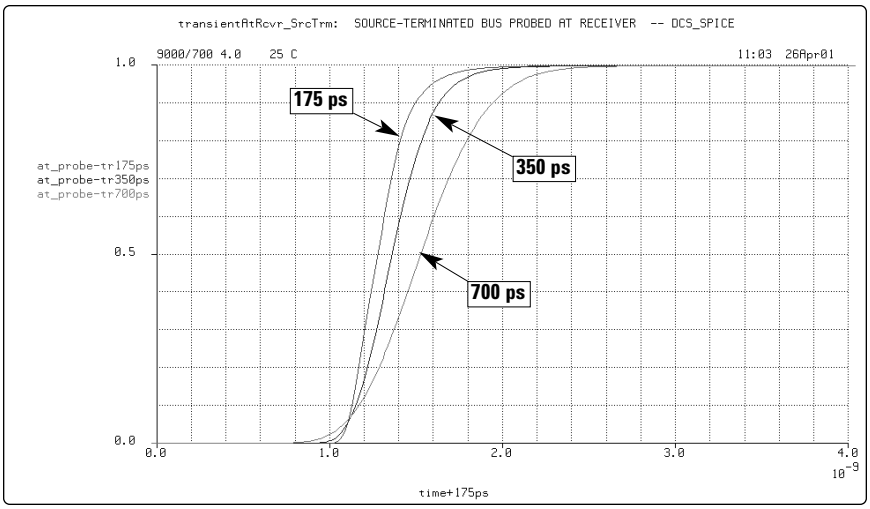

Figure 65. Signal at the logic analyzer probe input, source-terminated bus, probed at the receiver

Source-Terminated Bus, Probed After the Receiver

In this example, the target bus is extended by an additional 300 ps beyond the receiver. The probe load is at the end of this extension. This solution is undesirable for the target for the same reasons that probing in the middle of the bus is an undesirable solution for the probe. Because the transmission line has been extended past the receiver, the receiver doesn't see full amplitude until the incident edge has reflected off the end of the transmission line, now moved 300 ps away. Hence, the signal at the target receiver has a "step", which is just as objectionable to the system design as a "step" is to the logic analyzer, for the same reasons.

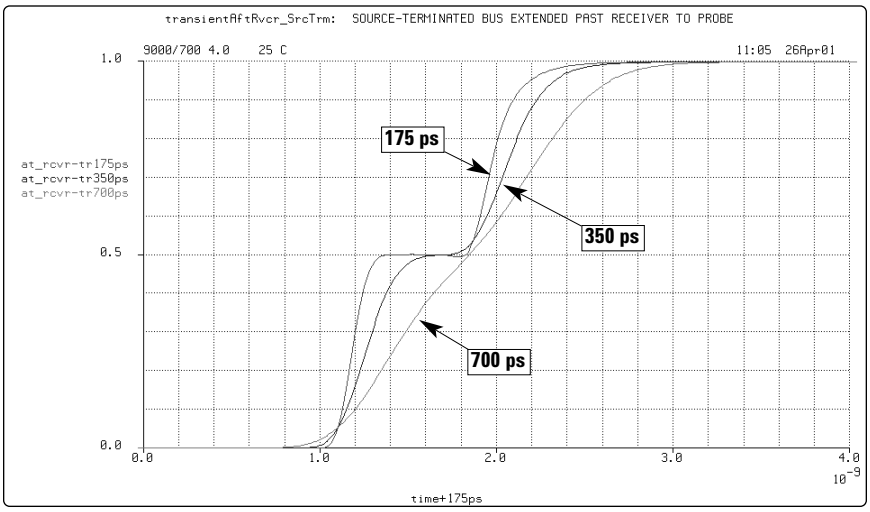

Figure 66. Signal at the receiver, source-terminated bus, probed after the receiver

Source-Terminated Bus, Resistive Divider Solution

The best solution to space constraints for source-terminated systems is to use a resistive divider connection (figure 68). The resistive divider solution taps off the target bus at the receiver through a divider resistor into a transmission line segment. This new transmission line segment is terminated into its characteristic impedance. The result is a slight attenuation on the signal at the receiver, and a significant attenuation at the probe tip. However, the signals all have clean edges. If the target signal has large enough amplitude to allow the signal to the probe to be attenuated and still meet the logic analyzer's input amplitude specifications, this may be the best probing solution.

The resistive divider solution for a source-terminated system may sometimes be possible using a 16760A logic analyzer. The 16760A logic analyzer only requires 250 mV signal swing (on the E5378A single-ended probe) to meet spec. The sensitivity of the 16760A allows solutions that may not be possible with other logic analyzers.

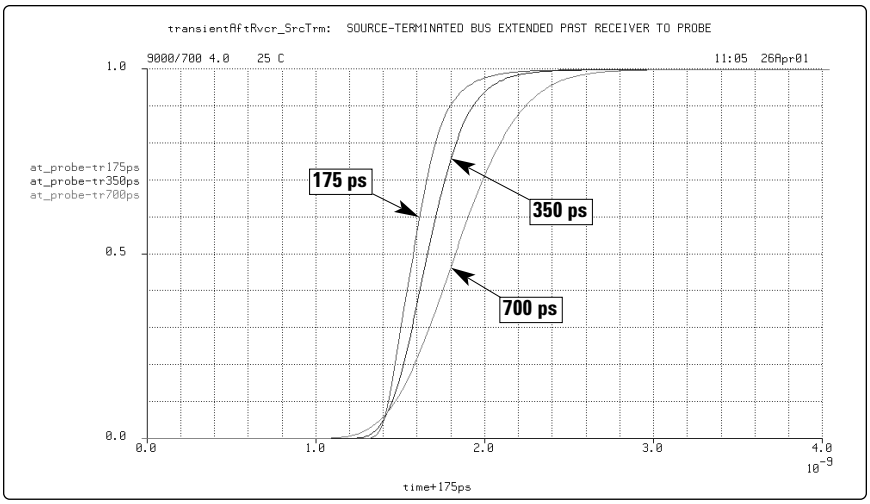

Figure 67. Signal at the logic analyzer probe input, source-terminated bus, probed after the receiver

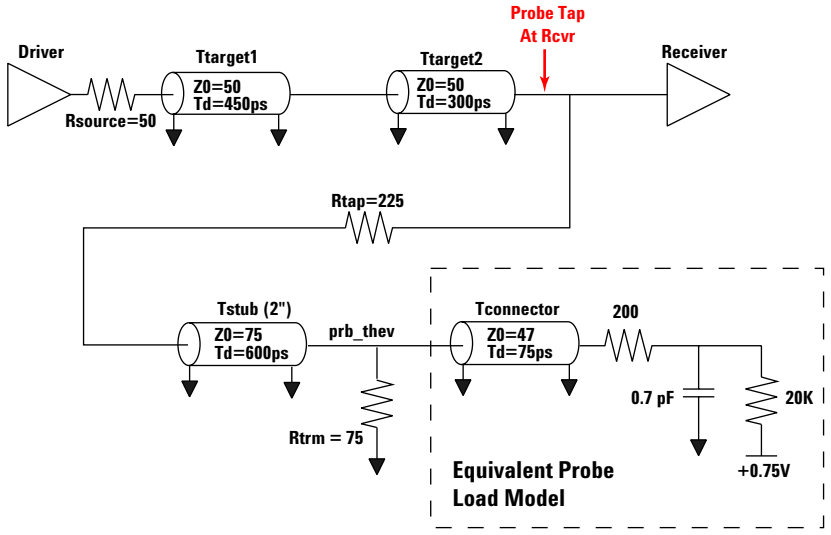

Figure 68. Resistive divider connection for a source-terminated bus, probed at the receiver

Source- and Load-Terminated Buses

A hypothetical source/load-terminated transmission line system is illustrated in figure 71. Three potential probing points have been indicated for probing at the driver, somewhere in the middle of the trace, or at the receiver. Each of these cases has been simulated with the E5379A equivalent load model inserted at the indicated places. To illustrate what it means to add the probe load, figure 71 shows the probe load inserted at the driver.

A system that is both source- and load-terminated is the most forgiving of all termination schemes. Any reflections from impedance discontinuities are absorbed at either the driving or receiving end of the transmission line, eliminating any re-reflections that may have been observed in a purely load-terminated system or a purely source-terminated system. Thus it is much easier to probe a source/load-terminated system with minimal impact on the target, regardless of where the probe is located in the system.

The only drawback to probing a source/load-terminated system is that the signal swings are typically reduced, which might make certain probing techniques unfeasible. However, the target is nearly immune to virtually all probe techniques. Even though the target is immune, the probe technique still needs to be evaluated for adequate signal integrity at the probe.

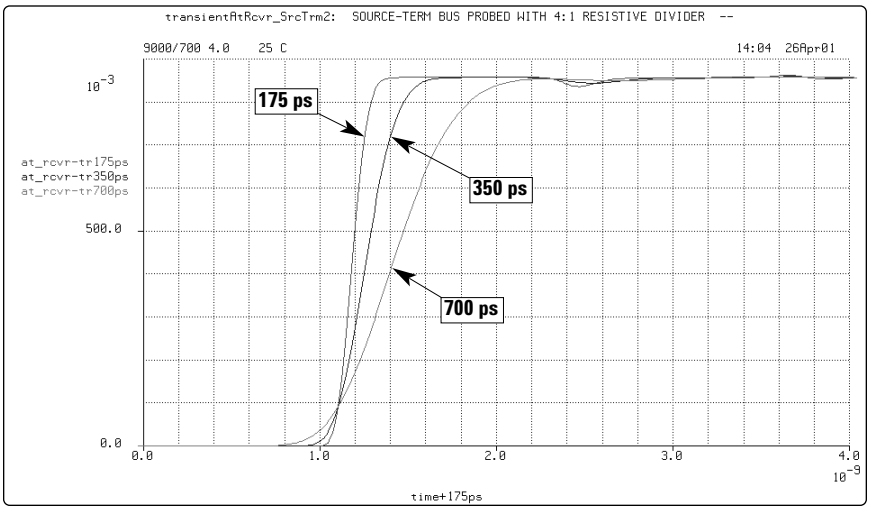

Figure 69. Signal at the receiver, source-terminated bus with resistive divider connection, probed at the receiver

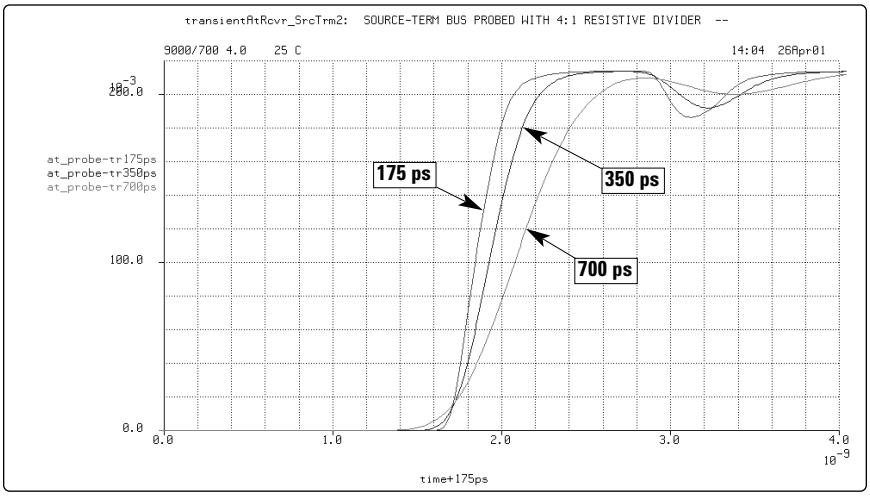

Figure 70. Signal at the logic analyzer probe input, source-terminated bus with resistive divider connection, probed at the receiver

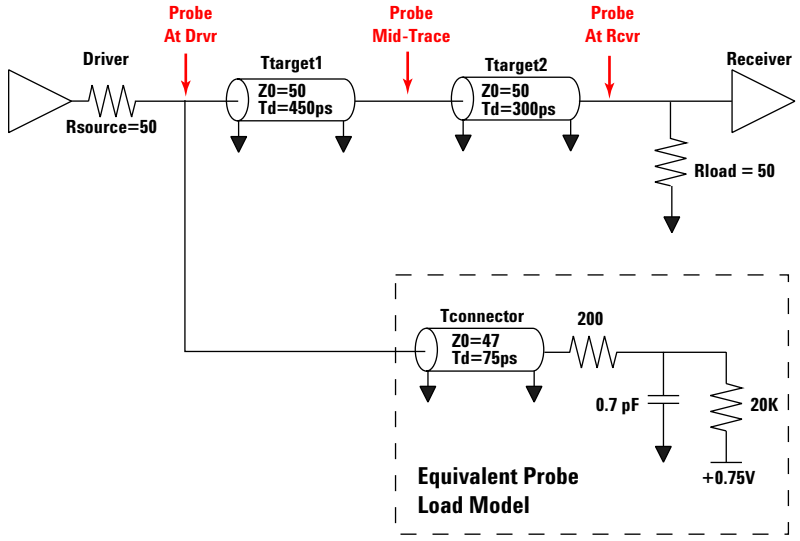

Figure 71. A schematic of a source- and load-terminated system

Source- and Load-Terminated Bus, Probed at the Driver

It will become obvious when reviewing the simulations for source/load terminated systems that it doesn't appear to matter where the logic analyzer probes the target bus. About the only difference in the different probe locations is the timing relationship between the probe and the target receiver.

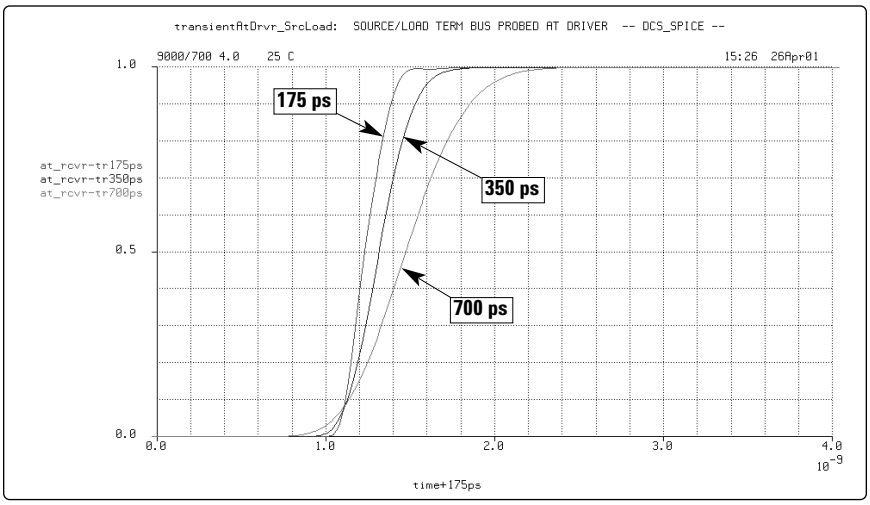

Figure 72. Signal at the receiver, source- and load-terminated system, probed at the driver

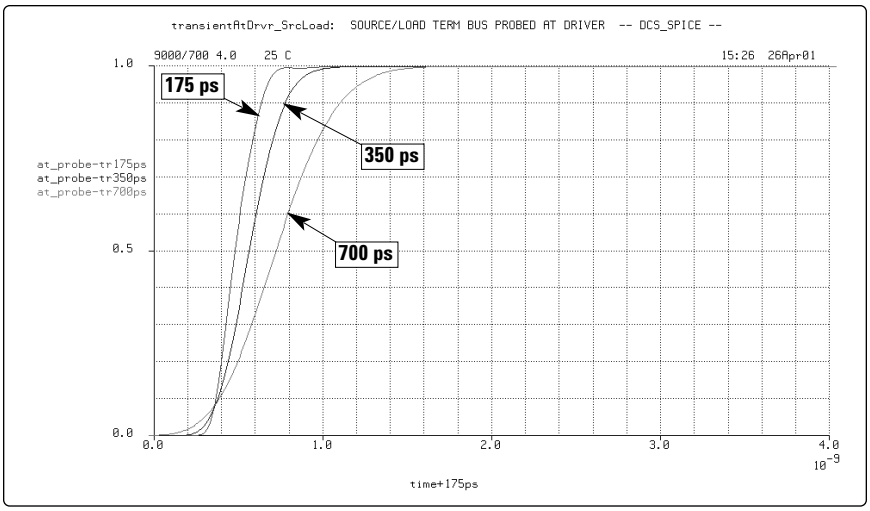

Figure 73. Signal at the logic analyzer probe input, source- and load-terminated system probed at the driver

Source- and Load-Terminated Bus, Probed in the Middle of the Target Trace

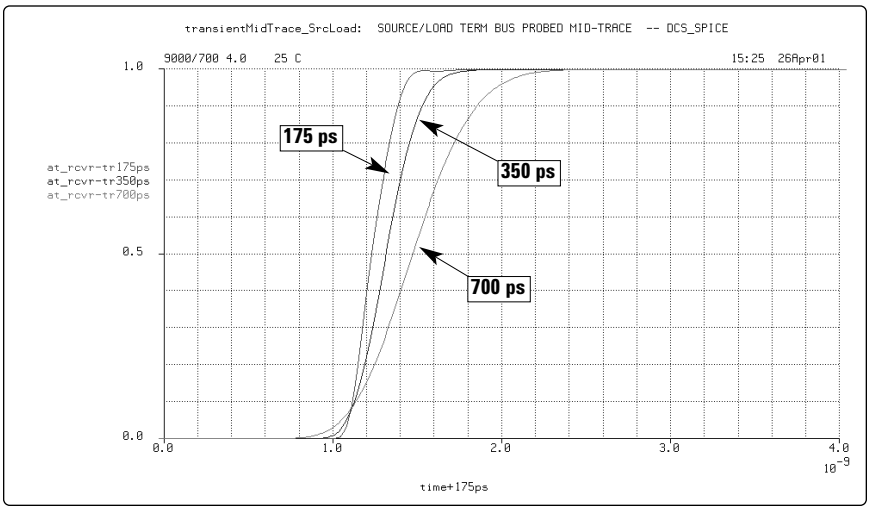

Figure 74. Signal at the receiver, source- and load-terminated bus probed in the middle of the target trace

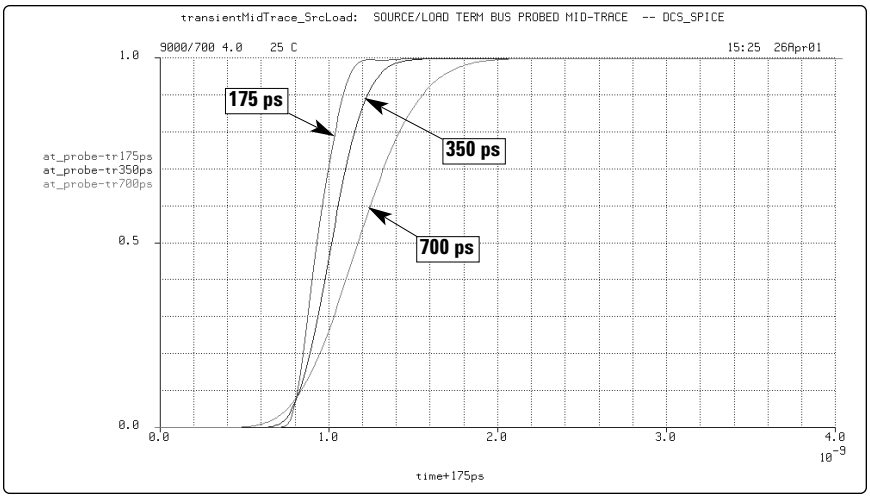

Figure 75. Signal at the logic analyzer probe input, source- and load-terminated bus, probed in the middle of the target trace

Source- and Load-Terminated Bus, Probed at the Receiver

As can be seen by the simulations, it makes virtually no difference where the signal is probed, in terms of signal fidelity at the probe and signal fidelity at the target receiver. Source/load terminated systems allow the most flexibility in probe placement, and have very little impact on the target.

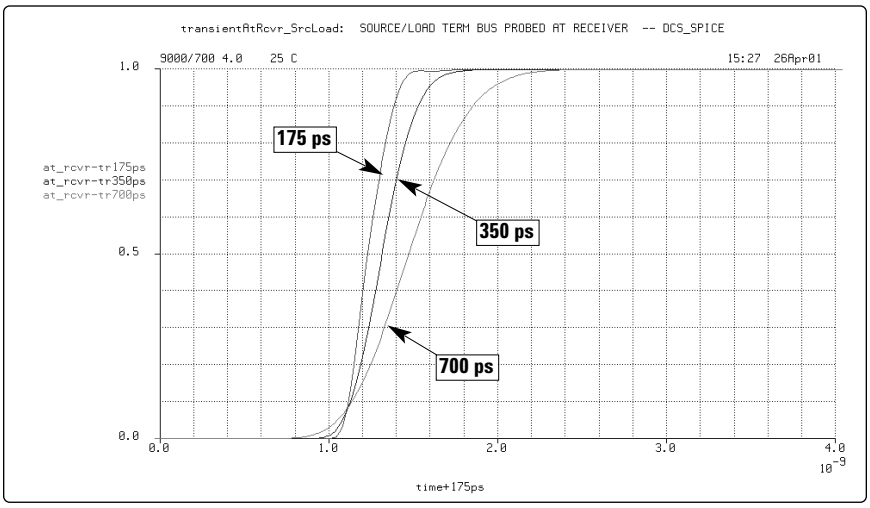

Figure 76. Signal at the receiver, source- and load-terminated system, probed at the receiver

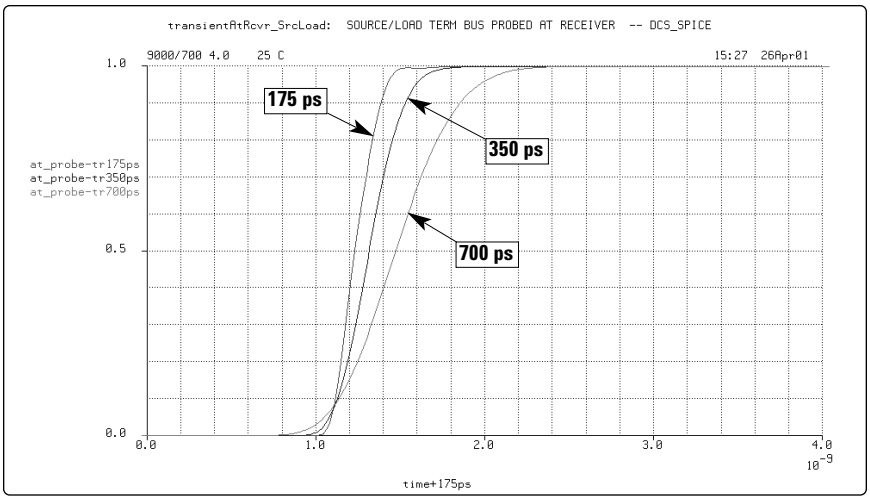

Figure 77. Signal at the logic analyzer probe input, source- and load-terminated system, probed at the receiver

Source- and Load-Terminated Bus, Probed After the Receiver

The only probe location that degrades the signal fidelity at the target receiver is when the target bus is extended PAST the receiver and terminated at the probe. In this example, the target bus is extended by an additional 300 ps beyond the receiver. The probe load is at the end of this extension, and the target load-termination has also been moved to the end of the trace. This may not be possible for all systems because some receiver devices have bus terminations integrated on-chip.

The receiver sees the reflection from the probe load traveling back down the trace toward the receiver. However, there is no re-reflection because the source termination absorbs all the reflection.

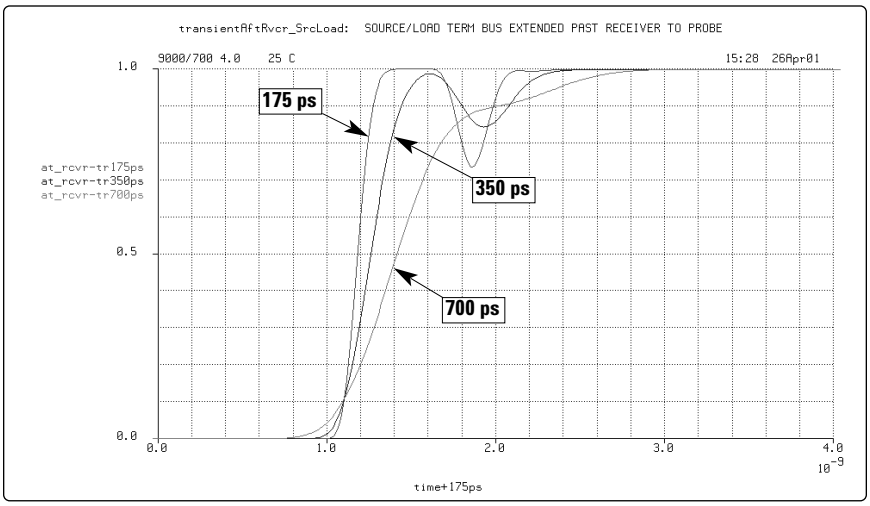

Figure 78. Signal at the receiver, source and load-terminated bus, probed after the receiver

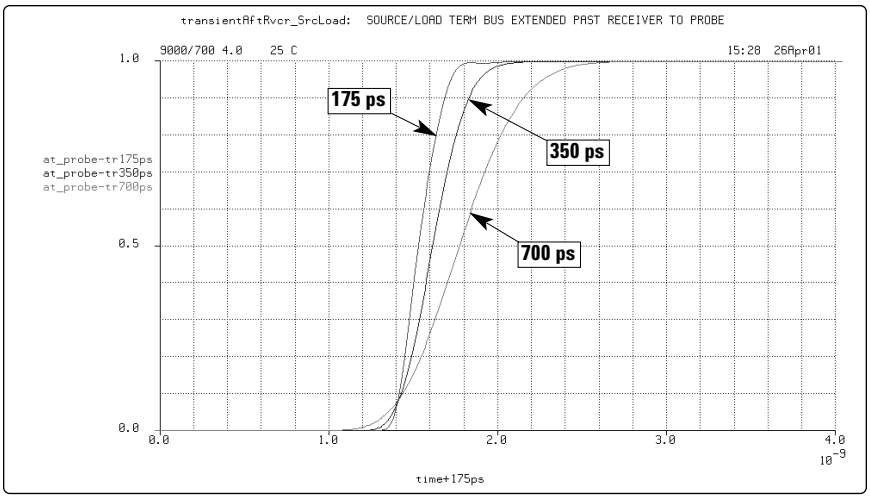

Figure 79. Signal at the logic analyzer probe input, source- and load- terminated bus, probed after the receiver

Suggested Board Layouts

- Figures 80 through 83 illustrate possible board layouts for the probe connector. The assumed design rules are:
- Figures 80-81: Signal traces on 0.0398" (1 mm) centers. Width determined by target design
- Figures 82-83: Trace widths and spacings equalized to minimize crosstalk where necked down between connector pins
- Ground traces are 0.013 inch (0.33 mm) wide, on 0.0398 inch (1 mm) centers
- Vias are on 0.0398 inch (1.0 mm) centers
- Vias are 0.010 inch (0.254 mm) finished hole size size, 0.023 inch (0.584 mm) signal pad size, with 0.033 inch (0.838 mm) clearance pads

Figures 80 and 81 are for the case where the signal traces end at the connector pins, with signal pairs broken out to alternating sides. Figures 82 and 83 are for the case where the signal traces continue on past the connector pins, with the signal traces crossing from one side of the connector to the other.

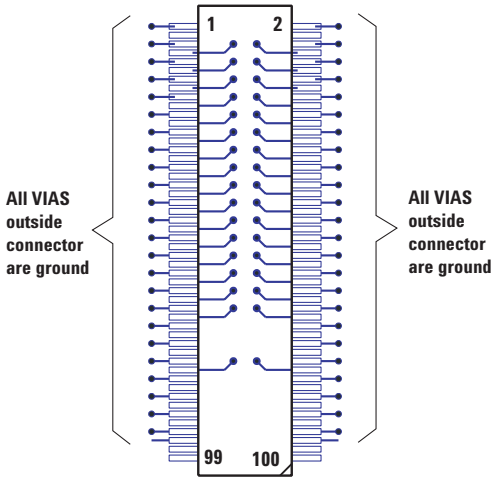

Figure 80. Surface layer, signals end at connector pins, signal pairs broken out to alternating sides of connector

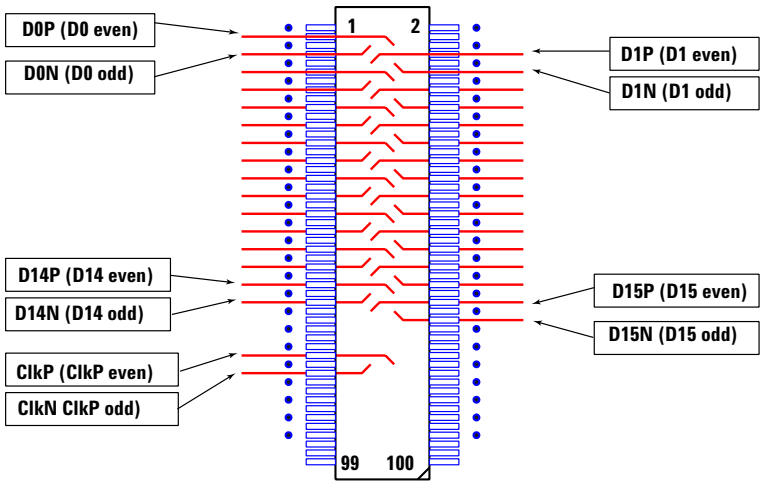

Figure 81. Signal layer 2, signals end at connector pins, signal pairs broken out to alternating sides of connector. Signal callouts in parentheses are for single-ended signals (E5378A probe)

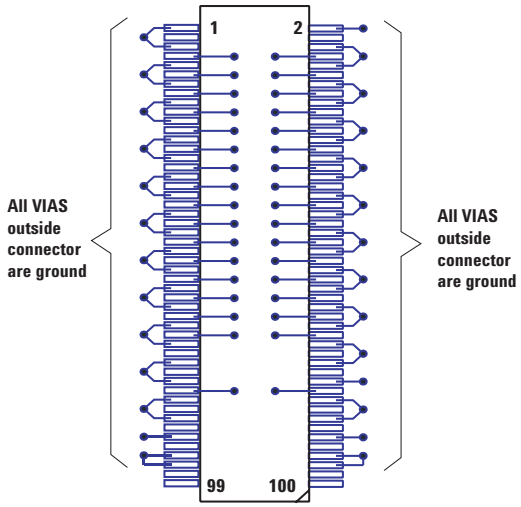

Figure 82. Surface layer, flow-through routing

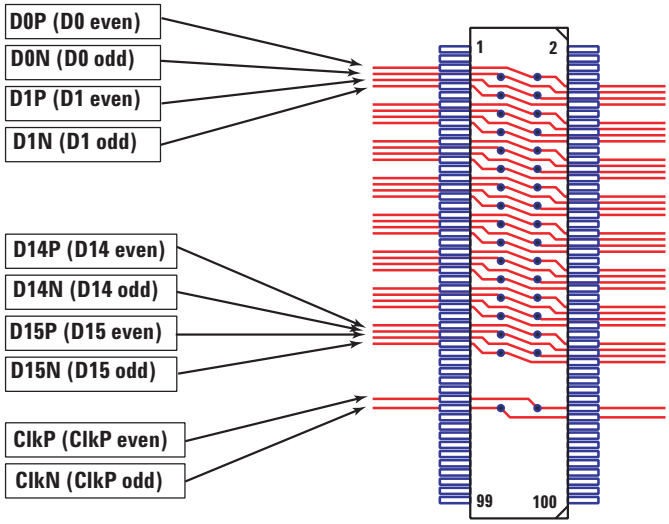

Figure 83. Signal layer 2, flow-through routing. Signal callouts in parentheses are for single-ended signals (E5378A probe)

Selecting a Connector for a New Logic Analyzer Probing System

As Agilent logic analyzers have increased in state speed above 400 MHz, a connector is needed that can handle this challenge. Some of the features of the connector must include:

- Minimized capacitive load on the target circuit
- Minimized crosstalk between adjacent signals at high frequencies
- Minimized resonances at high frequencies
- Mechanical robustness
- High connection density
- Surface mount capability

Minimizing Capacitance

Not only does the 100-pin connector used with the E5378A, E5379A, and the E5385A have inherently low capacitance between adjacent pins, but the layout of the pins is fortuitous in enabling Agilent to route the signals inside the probe tip to further reduce capacitance and crosstalk.

Signal Isolation and Crosstalk Reduction

Interleaving ground pins with signal pins enables a major improvement in isolation and reduction in crosstalk. The increased density of the 100-pin connector makes it possible to interleave signal and ground pins. For differential signals, isolation between adjacent pins is doubly important. Signals switching in opposite directions on adjacent pins can result in a doubling of the effective capacitive load.

Resonances

The pin inside the mated pair of connectors behaves like a short transmission line. This transmission line will resonate at some frequency. The longer the transmission line, the greater the resonance effects, and the lower the resonant frequency. The effective pin length of the 100-pin connector is quite short, so the resonance appears at a high frequency and its effect is minimized. A glance at figure 1 reveals the difference.

Mechanical Robustness

Probes are connected and disconnected frequently during their lifetime. You have to count on the connectors on your test equipment to make reliable connection. The connector must be selected to be mechanically robust. Other connectors with similar or in some cases superior electrical attributes to the 100-pin connector were considered, but the 100-pin connector is far more robust.

Agilent strongly recommends the use of support shrouds, Agilent part number 16760-02302 (for PC boards up to 0.062 inch thick) or 16760-02303 (for PC boards up to 0.120 inch thick). The shrouds aid significantly in protecting the connectors and extending their life. The shrouds also help avoid inadvertently dislodging the connector due to tugs on the probe cable when the target is moved, etc.

Connection Density

Connectors for logic analyzer probes consume valuable space on the target system. It was desirable to select a connector with high density. The high density of the 100-pin connector also allowed Agilent to interleave signal and ground pins, thereby greatly improving crosstalk and isolation, while at the same minimizing the space consumed by the connector.

Surface Mount Capability

The 100-pin connector does not require any through-holes in the area under the connector, which reduces the restrictions on routing signals under the connector. This may be very desirable for a logic analyzer probe connection. Through-holes are required for the recommended support shrouds, but these holes fall outside the connector area.

Recommended Reading

Blood, William R. Jr., "MECL System Design Handbook," 4th edition, 1988, published by Motorola. This handbook can be obtained from ON Semiconductor on the web. Go to <http://onsemi.com>. Click on "Online ordering" under "Documentation." Click on the link "General search." Type in "HB205" in the "Document number" field. Click "Submit." To view the document online, click on "PDF" in the right-hand column titled "PDF MFAX." You can also order a printed copy of the handbook on-line.

Johnson, Howard W., and Martin Graham, "High-speed Digital Design," Prentice-Hall, 1993, ISBN 0-13-395724-1

Agilent Reference Documents	Publication Number
Agilent Technologies 16700 Series Logic Analysis System, Product Overview,	5968-9661E
Probing Solutions for Agilent Logic Analysis Systems, Product Overview,	5968-4632E
User Guide, Agilent Technologies E5378A, E5379A, and E5380A Probes for the 16760A Logic Analyzer, User Guide	16760-97004
Agilent Technologies E5346A 38-pin Probe and E5351A 38-pin Adapter Cable, Installation Note	E5346-92014
Agilent Technologies E5385A 100-pin Probe, Installation Note	E5385-92000

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