Agilent E2920

PCI Timing Check using the Agilent E2920 PCI Series Exerciser/Analyzer

Application Note

Introduction

Until now, verifying that timing in 33 MHz 64-bit PCI designs met the setup and hold specification, required either very tedious measurements of all signals with a digital storage oscilloscope (DSO) or a very high speed logic analyzer, which is very costly. The timing check feature of the E2920 PCI Series Exerciser/Analyzer simultaneously monitors ***all*** 87 synchronous bused PCI signals for both setup and hold timing violations and identifies suspect individual signals. It works with your DSO to speed up the timing verification process not only by quickly telling you ***which signals*** are violating timing, but also triggering your scope ***when*** a timing violation occurs.

PCI Timing parameters

The PCI electrical specifications call for very tight AC timing characteristics. Even though the devices that are used in your design meet the PCI specifications, system design problems such as crosstalk or ground bounce lead to a need to verify your system timing.

The PCI specification calls for timing parameters outlined in figure 1.

All times shown in the timing budget in figure 1 are fixed by the specification, except for T_{prop}. T_{prop} is a computed value, based on the total timing budget, so factors that affect propagation time such as output driver characteristics, trace length (including trace length on adapter cards), number of loads, affect this system parameter. ***Since only some of these parameters are fully under control of the system designer, it is not possible to fully guarantee input timing under all circumstances.*** This makes it important to characterize and measure the PCI bus for timing violations.

Fundamentally, it is the input timing specifications (table 1), T_{su} and T_h, which must be met to insure proper operation. An output must drive its signal to all other devices on the PCI

Key Features

- Setup and hold time violation checking across 87 synchronous, bused signals
- Edge and glitch detection within the setup/hold window
- User adjustable window size within +/- 2 ns of both the PCI specification setup and hold time in 250 ps steps (total of up to 4 ns adjustment)
- Typical accuracy of +/- 250 ps at the PCI specification points
- Operation from 29 MHz to 35 MHz
- Generates a trigger output that can be used by a scope as a trigger
- Maskable selection of individual signals allows triggering on a single signal
- Protocol sensitive, so it doesn't operate during turn-around cycles

	T_{cyc} = 30 nsec			
33 MHz	T_{val} = 11ns	T_{prop} = 10ns	T_{skew} = 2ns	T_{su} = 7ns

Figure 1. Total Timing Budget — 33 MHz

1. The E2920 series with Timing Check capability includes the E2925B, E2926A, E2926B, E2927A, E2928A, and E2940A.

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bus to provide a stable input prior to the next rising clock edge (Tsu) and assure its stability until that following clock edge (Th). To measure if the system meets its setup time requires special measurement techniques, since the signal being measured happens before its point of reference (the PCI clock).

Speed	Setup Time (nsec min.)	Hold Time (nsec min)
33 MHz	7	0

Table 1: PCI Input Timing Specifications – Bused Signals

Challenges to measure

Measuring setup and hold time on 87 signals with a reasonable amount of accuracy requires either lots of time or lots of money. Using a DSO with a small channel count is a very effective but also very tedious method to characterize and measure setup and hold times for many signals. With one channel needed to probe the PCI clock, most scopes only allow up to three additional signals to be probed at a time. The DSO is an excellent tool to characterize the signal parametrics and to determine why a setup or hold violation has occurred, but its limited channel count makes it impractical to efficiently identify signals with timing violations.

Another choice to check for setup and hold violations is a high-speed timing analyzer. Timing analyzers have the advantage of viewing the entire bus, which allows simultaneous measurement of every signal with respect to the clock. The timing analyzer however, does not provide usable information about the signal parametric properties as a DSO does. It essentially has a one-bit D/A converter on every channel, so it is impossible to view actual signal characteristics with it, such as rise time, ringing, reflections, overshoot, etc.

A logic analyzer also needs special circuitry to detect edges or glitches, since a valid setup time means that there is an absence of signal transitions for 7 ns prior to the rising edge of the PCI clock. But how does the analyzer know when the clock edge will occur since it is after the interval of time we are interested in? The answer is that a setup time is measured starting N nanoseconds after the previous clock edge. Then it is simply a matter of calculating the cycle time and starting the edge detection circuit the appropriate time after the prior clock. This however, presents a need for more circuitry. Now the logic analyzer must be capable of accurately measuring the cycle time so it can calculate the correct time to start the edge/glitch detection circuitry. Additionally, the edge/glitch detection circuitry must be capable of being gated on and off, since it should only detect transitions during a small portion of the total cycle time. Only specially equipped logic analyzers are capable of this, but they either suffer from too small a channel count or a very high a price.

While neither the DSO nor the Logic analyzer provides an optimal solution, the DSO is the correct tool to visualize a signal when a violation has occurred because it has very high timing accuracy and can provide insight into the actual phenomena that is causing the timing violation.

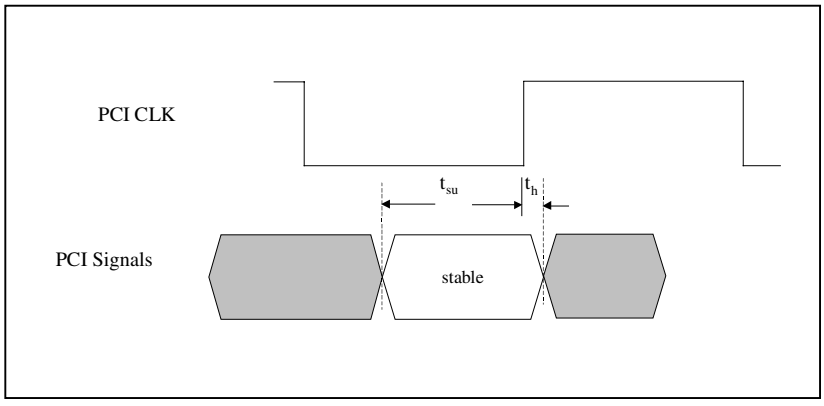

Figure 2: PCI Timing Requirements

Timing check

The Timing Check for the Agilent E2920 PCI Series operates simultaneously across all the PCI synchronous bused signals. This makes it an ideal companion to a DSO, which can be used to visualize the bad signal(s).

How it works

In order to measure setup time, which occurs prior to the reference signal, and hold time which is specified at 0ns with respect to the PCI clock, the timing check performs the following operations.

1. Measure the PCI clock frequency. The frequency is measured prior to the timing check being activated and is stored as a reference value. Prior to returning its status, the frequency is measured again and compared to the reference frequency. If they do not compare, the timing check is turned off indicating that a measurement is not possible since the clock frequency is not stable.

2. Get the user settings for the measurement window size. The default values are the actual PCI setup/hold specifications for the given bus frequency.

3. Adjust delay lines to start and stop the measurement window after the previous clock edge. This operation uses the information from steps 1 & 2 to determine the correct settings for the delay lines.

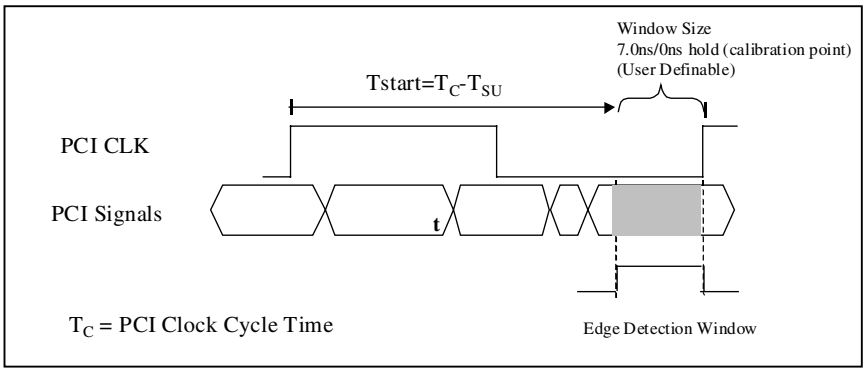

Figure 3: Calculation of Measurement Window Start

The GUI Interface

The timing check can be used either with the standard CAPI interface provided with the Agilent PCI Exerciser/ Analyzer or with the E2970A Analyzer Graphical User Interface. Both require software version R5.10.07 or greater.

When using the graphical user interface, the timing check window can be viewed using the main window menu ***Analyzer > Timing Check....*** It is shown to the right in figure 4. On the left hand side of the window, all the PCI signals are listed individually along with twelve external trigger inputs that can simultaneously be measured. Associated with each signal is a ***Mask*** and ***Status*** field. The mask field allows individual signals to be enabled to provide a trigger capability when only that signal generates a timing violation. The status field shows one of three status values. A green ***OK*** indicates that there is no detected timing violation on that signal with the current setup and hold values. A yellow ***ERROR*** indication flags the occurrence of a timing violation, but that signal was masked off. This prevents a timing violation on this signal from generating a trigger condition. A red ***ERROR*** indication flags an unmasked timing violation.

The default measurement window size is set to the PCI 33 MHz timing specification. (7 nsec setup/0 ns hold). Variations of +/- 2 ns from the default values are possible in 250 psec steps. Press the ***Edit...*** button in the Timing Check window to modify the window size (figure 5). Selecting the ***Manual*** setting allows you to modify the setup/hold time values for the desired measurement window size.

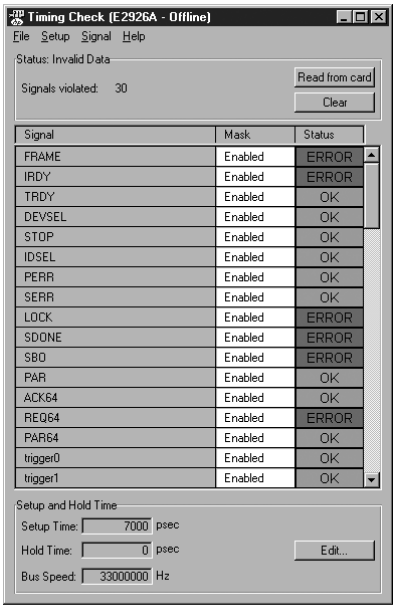

Figure 4. Timing Check Main Window

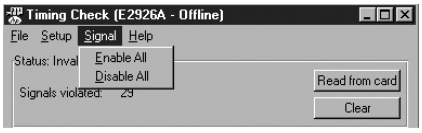

Figure 5. Timing Check Adjustment Window

Another important control in the GUI is the ***Signal*** menu, to enable or disable all signals (figure 6). This control is useful when a signal or signals have shown a timing violation and you want to isolate a trigger condition on an individual signal. All signals can easily be masked off, then you can enable the individual signal that you want to trigger on.

How to use

After installing the PCI Exerciser/Analyzer, start the GUI on your host platform (this could also be your DUT if you control the card through the PCI port). Follow the steps below to:

Check for violations at the PCI specification values

1. From the Timing Check window, verify that the PCI timing specifications are selected for your bus speed.

2. Choose the *Signal-Enable All* menu to turn on all signals.

3. The timing check will run automatically. Run some programs that exercise the different masters in your DUT to verify that they all drive the bus with valid T_{val} timing.

4. Press the ***Read from card*** button in the Timing Check window to upload the timing check output. If a timing violation occurs, go to the procedure **Trigger on a timing violation.**

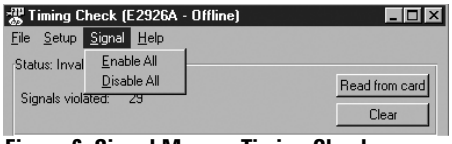

Figure 6. Signal Menu—Timing Checker Main Window

Determine PCI timing margins

The timing check can be used to check your timing margins up to 2 ns greater than both the PCI specification's setup and hold times. For a 33 MHz PCI bus, this means that the setup time margin can be checked up to 9 nsec and hold time margin to +2 nsec after the rising edge of the clock.

1. Choose the ***Signal > Enable All*** menu to turn on all signals.

2. Press the ***Edit...*** button in the Timing Check window. Select the ***Manual*** button to allow the timing check window size to be edited. Change the setup and/or hold time to their maximum values to check for the widest timing margin.

3. The timing check will run automatically. Run some programs that exercise the different masters in your DUT to verify that they all drive the bus with valid T_{val} timing.

4. Press the ***Read from card*** button in the Timing Check window to upload the timing check output. If a timing violation occurs, go to the procedure **Trigger on a timing violation.**

5. If timing violations occur, you can modify the timing check window size to determine the amount of timing margin in your system.

Trigger on a timing violation

The full power of the timing check becomes available when it is used to trigger a DSO upon a timing violation. The timing check should first be used to identify which signal or signals are causing a timing violation. After this, it is appropriate to trigger a DSO when a "slow" signal is identified for probing.

1. In the timing check window, choose the ***Signal->Disable All*** menu to turn **off** all signals.

2. In the same window, select an individual signal to enable by clicking left mouse button when the cursor is over that signal name.

3. Connect the trigger input of your DSO to the **TIO0** (Trigger I/O 0) signal on the Agilent PCI Exerciser/ Analyzer. Refer to figure 7 for the location of this signal. Note that ground signals are on all 12 pins of the trigger I/O header to the left of each signal.

4. Probe the **signal of interest** and the **PCI CLK** signals on your DUT with two channels of your DSO.

5. Open the Command Line window in the E2926 GUI from the menu **Windows-> Command Line....** Use the **File->Run Script...** menu to run "samples*gui**tmgchktr.cli*". This command line script sets up the trigger I/O sequencer to generate a rising edge on TIO0 when a timing violation has occurred.

6. Set your DSO to trigger on the external trigger input.

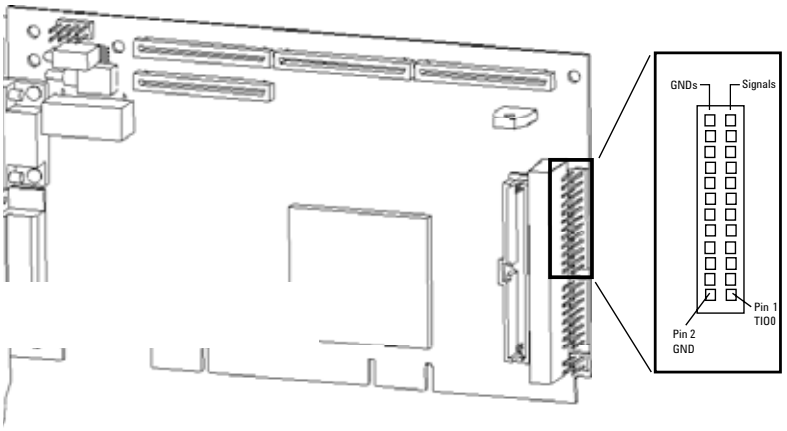

Figure 7. E2920A Trigger Output Location

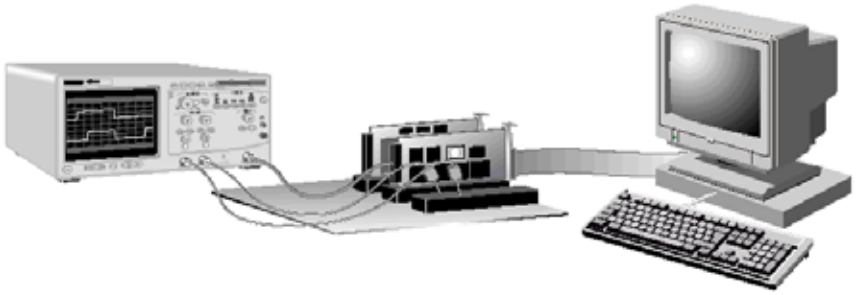

Figure 8. Typical Measurement Setup

PCI LocalBus Board Pinout Relevant Signals in Bold Face

	Universal Board			Universal Board	
Pin	**Side B**	**Side A**	**Pin**	**Side B**	**Side A**
1	-12V	TRST#	49	M66EN	**AD[09]**
2	TCK	+12V	50	KEYWAY	
3	Ground	TMS	51	KEYWAY	
4	TDO	TDI	52	**AD[08]**	**C/BE[0]**
5	+5V	+5V	53	**AD[07]**	+3.3V
6	+5V	INTA#	54	+3.3V	**AD[06]**
7	INTB#	INTC#	55	**AD[05]**	**AD[04]**
8	INTD#	+5V	56	**AD[03]**	Ground
9	PRSNT1#	Reserved	57	Ground	**AD[02]**
10	Reserved	+5V	58	**AD[01]**	**AD[00]**
11	PRSNT2#	Reserved	59	$+V_{I/O}$	$+V_{I/O}$
12	KEYWAY		60	**ACK64#**	**REQ64#**
13	KEYWAY		61	+5V	+5V
14	Reserved	Reserved	62	+5V	+5V
15	Ground	RST#		KEYWAY	
16	**CLK**	$+V_{I/O}$		KEYWAY	
17	Ground	GNT#	63	Reserved	Ground
18	REQ#	Ground	64	Ground	**C/BE[7]**
19	$+V_{I/O}$	Reserved	65	**C/BE[6]**	**C/BE[5]**
20	**AD[31]**	**AD[30]**	66	**C/BE[4]**	$+V_{I/O}$
21	**AD[29]**	+3.3V	67	Ground	**PAR64**
22	Ground	**AD[28]**	68	**AD[63]**	**AD[62]**
23	**AD[27]**	**AD[26]**	69	**AD[61]**	Ground
24	**AD[25]**	Ground	70	$+V_{I/O}$	**AD[60]**
25	+3.3V	**AD[24]**	71	**AD[59]**	**AD[58]**
26	**C/BE[3]]#**	**IDSEL**	72	**AD[57]**	Ground
27	**AD[23]**	+3.3V	73	Ground	**AD[56]**
28	Ground	**AD[22]**	74	**AD[55]**	**AD[54]**
29	**AD[21]**	**AD[20]**	75	**AD[53]**	$+V_{I/O}$
30	**AD[19]**	Ground	76	Ground	**AD[52]**
31	+3.3V	**AD[18]**	77	**AD[51]**	**AD[50]**
32	**AD[17]**	**AD[16]**	78	**AD[49]**	Ground
33	**C/BE[2]**	+3.3V	79	$+V_{I/O}$	**AD[48]**
34	Ground	**FRAME#**	80	**AD[47]**	**AD[46]**
35	**IRDY#**	Ground	81	**AD[45]**	Ground
36	+3.3V	**TRDY#**	82	Ground	**AD[44]**
37	**DEVSEL#**	Ground	83	**AD[43]**	**AD[42]**
38	Ground	**STOP#**	84	**AD[41]**	+3.3V
39	**LOCK#**	+3.3V	85	Ground	**AD[40]**
40	**PERR#**	**SDONE**	86	**AD[39]**	**AD[38]**
41	+3.3V	**SBO#**	87	**AD[37]**	Ground
42	**SERR#**	Ground	88	$+V_{I/O}$	**AD[36]**
43	+3.3V	**PAR**	89	**AD[35]**	**AD[34]**
44	**C/BE[1]#**	**AD[15]**	90	**AD[33]**	Ground
45	**AD[14]**	+3.3V	91	Ground	**AD[32]**
46	Ground	**AD[13]**	92	Reserved	Reserved
47	**AD[12]**	**AD[11]**	93	Reserved	Ground
48	**AD[10]**	Ground	94	Ground	Reserved

Related literature	Publication number
• *Agilent Technologies E2920, PCI Series -PCI and PCI-X Design Verification brochure*	*5968-9694E*
• *E2920 PCI Performance Multimedia CD*	5965-5882E
• *Agilent E2925B 32bit, 33 MHz, Agilent E2926B 32/64bit, 33 MHz PCI Exerciser & Analyzer,*	5968-3501E
• *Agilent E2940A CompactPCI Exerciser & Analyzer, technical overview*	5968-1915E
• *Agilent E2928A 32/64bit, 66 MHz, PCI Exerciser & Analyzer, technical overview*	5968-3506E

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