Designing Packet Over SONET/SDH (POS) Hardware

Agilent Technologies Broadband Series Test System
Application Note

Introduction

As a result of the evolution of wire-speed layer-3 switching from enterprise networks to the core of public data networks, Packet Over SONET/SDH (POS) has emerged as the technology of choice for interconnecting high-speed backbone routers. POS is deployed in the line cards of Gigabit and Terabit routers and is implemented in hardware in order to handle wire speeds ranging from 155 Mb/s to 10 Gb/s.

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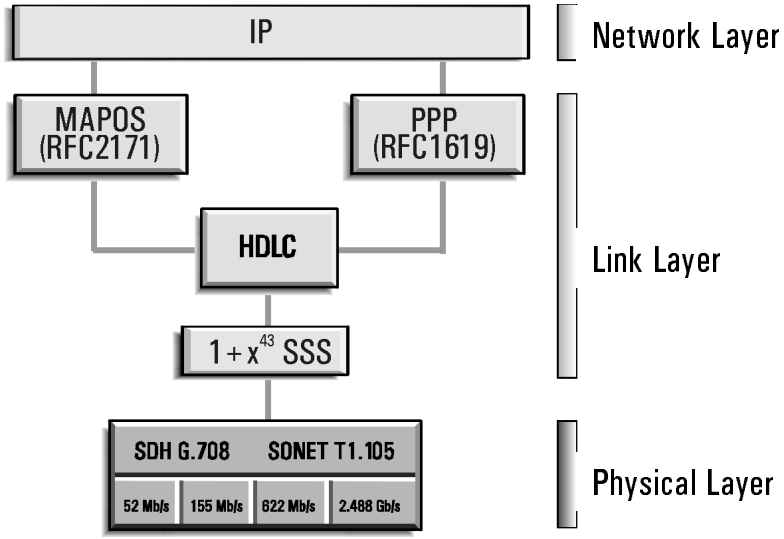
How POS works

POS is a layer-2 protocol that maps IP packets into SONET/SDH frames. It can be thought of as a replacement of the AAL-5 adaptation layer, with the advantage that it avoids the inefficient process of ATM segmentation and reassembly. There are three main elements to POS:

- A link access protocol such as PPP or MAPOS
- Octet-synchronous HDLC-like framing (RFC1662: PPP in HDLC-like Framing), hereafter referred to simply as "HDLC"
- Payload scrambling (RFC1619: PPP over SONET/SDH) prior to insertion into the SONET/SDH Synchronous Payload Envelope (SPE).



The POS protocol stack.

PPP (Point-to-point Protocol) establishes the link, exchanges IP addresses, and negotiates link parameters such as the FCS (Frame Check Sequence) size. The link establishment procedure must complete successfully before the router will forward any user data across the link. However, because PPP is handled by software, it can generally be disabled at the hardware testing stage.

MAPOS (Multiple Access Protocol over SONET/SDH) is a connectionless protocol.

It is designed to provide point-to-multipoint switching capability over SONET/SDH, which is inherently a point-to-point technology. A MAPOS Frame Switching Device provides Ethernet-like layer-2 switching between multiple routers and SONET/SDH links. MAPOS uses the address field in HDLC-like frames to provide broadcast and multicast capability.

"HDLC" framing delineates packet boundaries so that the receiver can extract them from the SONET/SDH frames. The "HDLC" frame includes Address, Control, and Protocol fields, followed by the encapsulated packet.

A 16 or 32-bit FCS protects the entire frame. The octet value 7E is used between frames to indicate the end of one frame and the start of the next. This means that the user data cannot contain the 7E-octet value. This is resolved by using an escape sequence, where 7E is converted to 7D-5E. The 7D octet is interpreted as the "escape" character. If present in the user data, it must itself be escaped by converting 7D to 7D-5D. This process, which is called octet stuffing, is reversed at the receiver.

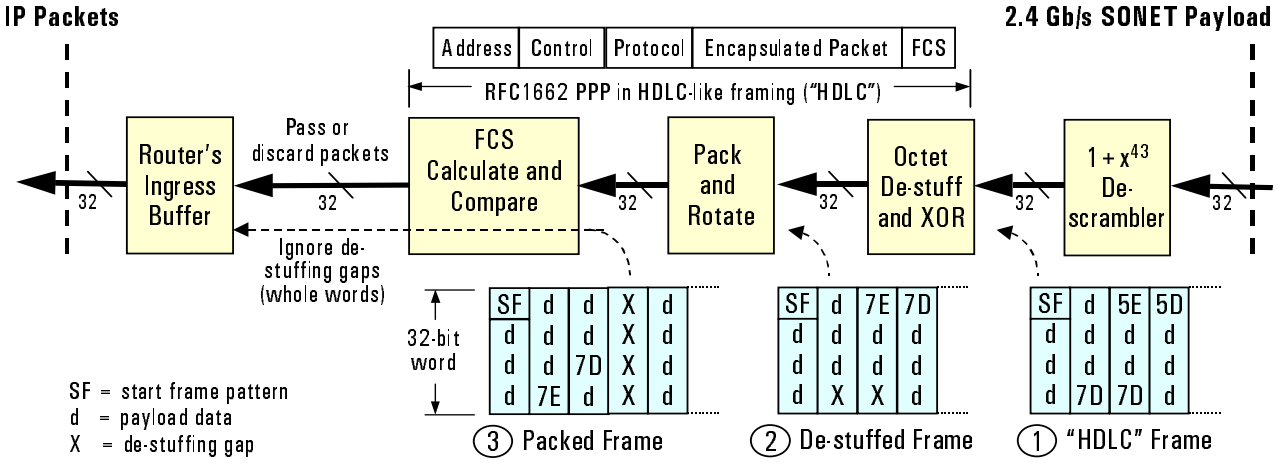
Payload scrambling prevents the occurrence of SONET/SDH framing patterns in the user data (possibly due to malicious intent) that could cause loss of SONET/SDH signal at the receiver. After the "HDLC" frame has been assembled, it is passed through a $1+x^{43}$ scrambler. This is the same algorithm as is used in ATM interfaces up to OC-48 line rates. The hardware design becomes very challenging at OC-192 rates, when you consider that it involves implementing a 43-bit serial shift register across a 128-bit parallel data bus!

POS Implementation Issues

POS line cards are currently designed using FPGAs (Field Programmable Gate Arrays), capable of clock speeds up to around 80 MHz. Higher clock speeds and narrower bus widths are possible using ASICs (Application Specific Integrated Circuits). However, until the POS standard is ratified by the IETF (Internet Engineering Task Force), it is safer to use programmable components.

Both RFC1619 and RFC1662 are currently under review by the PPP Extensions (pppext) working group of the IETF.

In low-speed WAN interfaces, HDLC framing is performed by software, but at SONET/SDH line rates it must be performed by hardware. FCS calculation, octet stuffing and de-stuffing, and payload scrambling are the major sources of complexity in implementing POS, particularly in high-speed wide-bus architectures. The design issues are best understood by considering typical traffic patterns that the line card needs to deal with. We will briefly examine three different types of packet data that act as corner cases.



POS receive-chain hardware: Processing of octet-oriented HDLC-like frames using wide-bus architectures presents the hardware designer with some serious challenges.

Typical POS line card architectures

SONET/SDH rate	OC-3c/STM-1 155 Mb/s	OC-12c/STM-4c 622 Mb/s	OC-48c/STM-16c 2.4Gb/s
Clock speed	20 MHz	40 MHz	80 MHz
Bus width	8 bits	16 bits	32 bits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Test Case #1: Send maximum stuffing-ratio traffic

An IP/PPP packet that contains all 7D or 7E octet values will result in a doubling of the payload size after insertion into the HDLC frame. A sequence of such packets will cause maximum stress on the stuffing and de-stuffing circuits. This payload pattern also tests out the effectiveness of the flow control mechanism between the POS line card and the router's egress or ingress buffer.

Test Case #2: Vary the inter-frame gap by octet increments

This test effectively introduces a "phase shift" of the octet-synchronous HDLC frame as it is presented to the wide-bus architecture and will pick up problems in the pack-and-rotate circuit. For example, in a POS line card with a 32-bit architecture, there are four different octet phases to be verified, and for a 128-bit architecture there are sixteen.

Test Case #3: Send minimum-size packets at full rate

This determines the maximum rate of FCS calculations that can be performed. It is also a good overall test of the POS line card's HDLC frame-handling capacity.

Summary

The key issue in any POS implementation is wire-speed layer-2 processing capacity. Octet-oriented processes such as octet stuffing, packing, and rotating become more complex to perform in hardware as the clock speed and bus width increases. However, with careful design and consideration of worst-case traffic patterns that need to be handled, POS line cards can be implemented at speeds of 2 Gb/s and higher using current FPGA technology.

IETF RFCs

791	Internet Protocol version 4 (IPv4)
1332	The PPP Internet Protocol Control Protocol (IPCP)
1619	PPP over SONET/SDH
1661	Point-to-Point Protocol (PPP)
1662	PPP in HDLC-like Framing
2171	MAPOS - Multiple Access Protocol Over SONET/SDH Version 1
2172	MAPOS Version 1 Assigned Numbers
2173-2175	MAPOS node switch protocol specifications

IETF work in progress

Refer to the IETF web site at: http://www.ietf.org under IETF Working Groups.

Point-to-Point Protocol Extensions (pppext) working Group:

- PPP in HDLC-like Framing (extension to RFC1662)
- PPP over SONET/SDH (extension to RFC1619)

Acronyms

ADM	Add-drop Multiplexer (SONET/SDH)
ASIC	Application-Specific Integrated Circuit
BSTS	Broadband Series Test System
FCS	Frame Check Sequence
HDLC	High-level Data Link Control protocol (layer 2)
IETF	Internet Engineering Task Force (IP protocol suite)
IP	Internet Protocol (layer 3)
IPCP	IP Control Protocol (over PPP)
IPv4	Internet Protocol version 4
LCP	Link Control Protocol (part of PPP - for establishing, configuring, and testing the data-link connection)
MAPOS	Multiple Access Protocol Over SONET/SDH
MUX	Multiplexer (SONET/SDH)
POS	Packet Over SONET/SDH
PPP	Point-to-Point Protocol (for transmission of multiprotocol datagrams over point-to-point links)
RFC	Request for Comment (IETF document)
SDH	Synchronous Digital Hierarchy
SONET	Synchronous Optical Network (transmission protocol)
SSS	Self-Synchronous Scrambler (ATM-like $1 + x^{43}$ payload scrambler)

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Specifications subject to change.

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