Passively Probing a Motorola/IBM Power PC 740/750 Target System with HP E5346A High-Density Termination Adapters

Application Note

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This application note describes how to connect the HP logic analyzer to the BGA package of a Motorola/IBM PowerPC 740/750 target system for use with the HP E2498A inverse assembler.

Signals required for inverse assembly are shown in the pinout information table and must be routed to AMP Mictor 38 connectors for connection to the logic analyzer.

Eight, 16-channel logic analyzer pods are required for inverse assembly. These eight pods are connected to four HP E5346A high-density termination adapters not included with the HP E2498A inverse assembler.

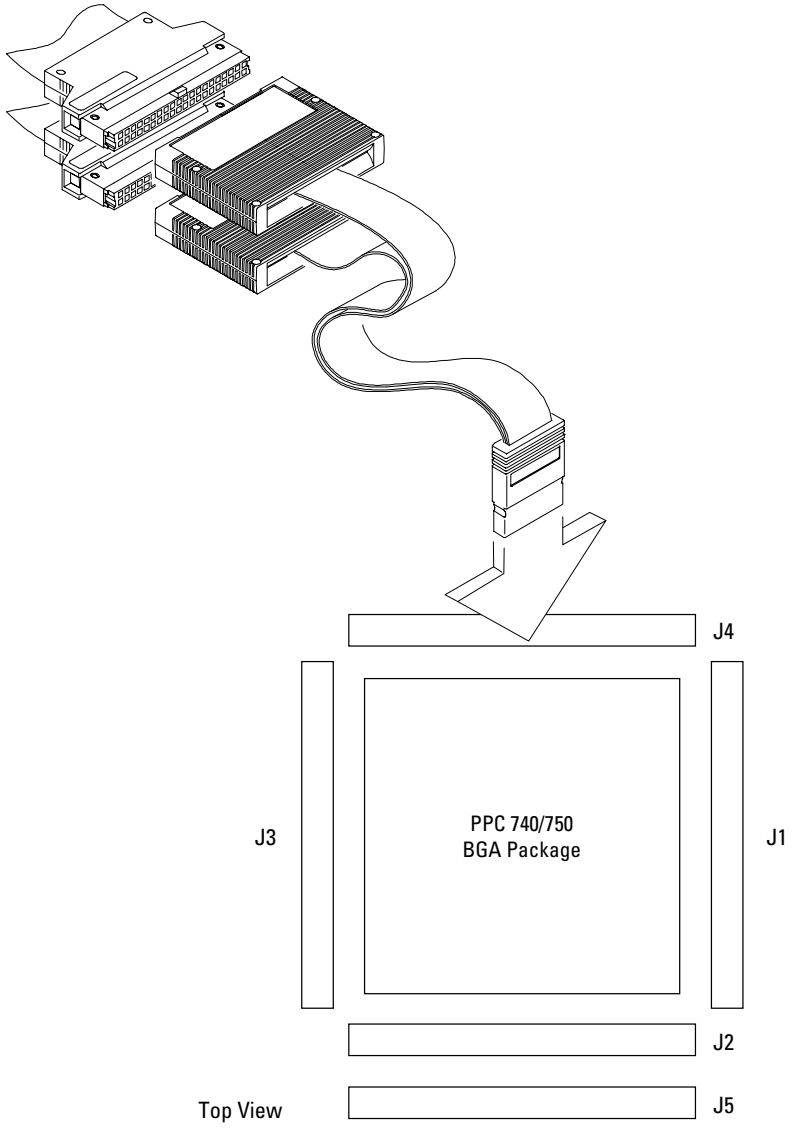


Figure 1. Connector layout for a PPC740/750 BGA target

Direct Connection through HP E5346A High-Density Adapter Cables

The HP E5346A high-density adapters use a minimal amount of board space. Each high-density adapter connects two logic analyzer pods, providing 32 channels of logic analysis per connector and access to two clock pins as shown in Figure 2.

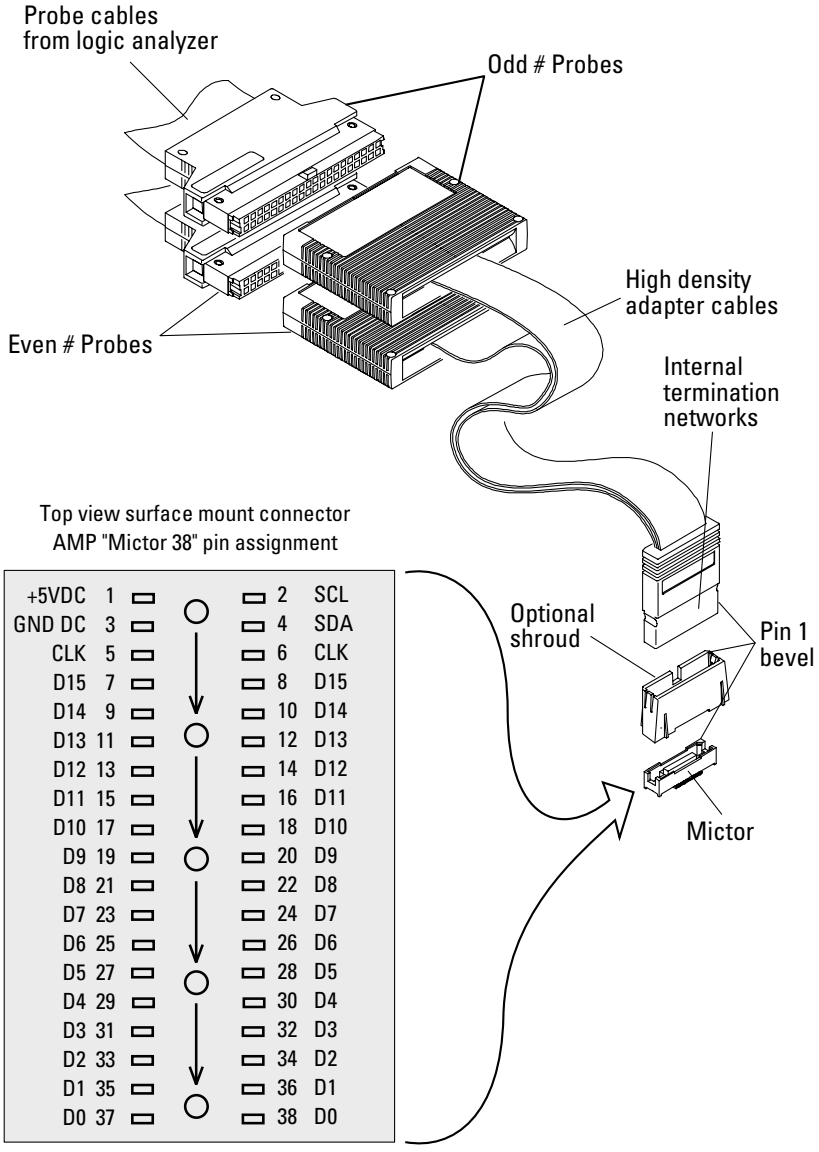


Figure 2. HP E5346A High-Density Adapter Cables

Grounds need to be connected to pin 3 of the AMP Mictor connector. SCL, +5VDC and SDA are not to be connected to the target system (pins 1,2,4 on Mictor connector).

Termination for logic analysis is included at the probe tip of the HP E5346A High-Density Termination Adapter for easy application and use. A schematic of this termination is shown in figure 3.

The AMP Mictor connector must be placed close enough to the target system so the stub length created is less than 1/5 the Tr (bus risetime). For PC board material (er=4.9) and Zo in the range of 50-80Ω, use a propagation delay of 160 ps/inch of stub.

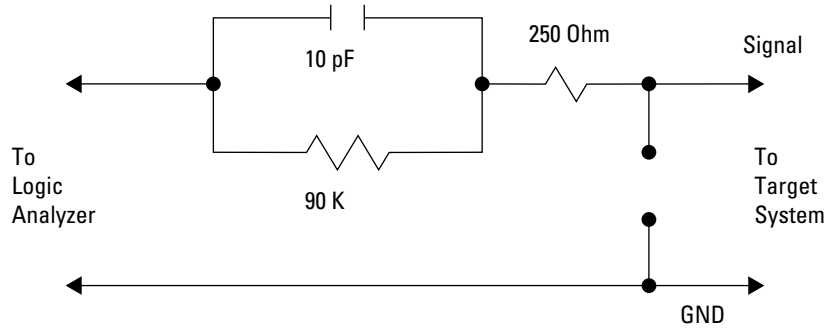


Figure 3. RC Network for Signal Termination

Mictor Connector Placement

Placing the AMP Mictor connectors as close as possible to the signal source will minimize stub length and ensure a reliable measurement. Figure 4 shows the connector layout of J1-J5. J1-J4 are required for inverse assembly, while J5 is optional for timing and state analysis of I/O ports.

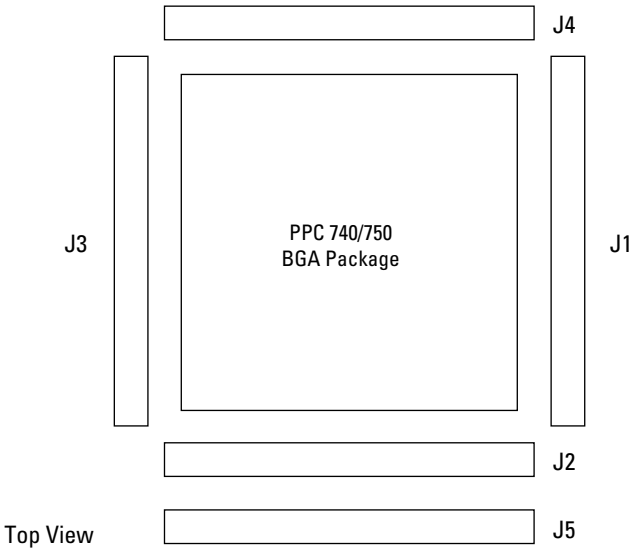


Figure 4. Mictor Connector Placement

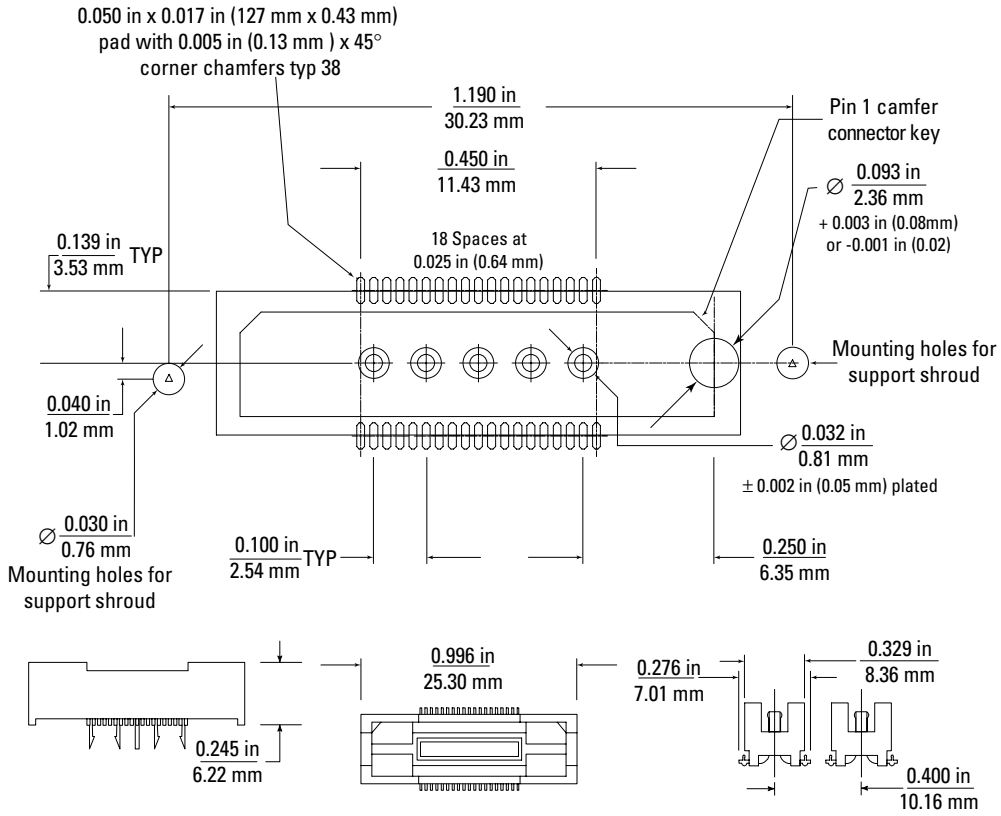


Figure 5. AMP Mictor Connector Dimension

Mictor Connector

The AMP Mictor Connectors are available directly from AMP (PN 2-767004-2) or from HP (PN E5346-68701). The HP Mictor kit contains five AMP Mictor connectors and five support shrouds. The signals +5 V DC, SCL, and SDA are not used for probing and should not be connected to the target system as shown in Figure 2.

Support Shroud

A support shroud (HP E5346-44701) is recommended to provide additional strain relief between the HP E5346A adapter and the AMP Mictor connector as shown in figure 5. The shroud fits around the AMP Mictor connector and requires two through-hole connections to the target board. Five shrouds are included with five AMP Mictor connectors in the HP E5346-68701 kit.

Inverse Assembler

An inverse assembler translates logic levels captured by the logic analyzer into PowerPC 740/750 mnemonics and identifies the microprocessor bus cycles captured, such as memory read/write, interrupt acknowledge, or I/O read/write.

For better visibility of the external bus, the instruction cache should be disabled. If the instruction cache is enabled, many instructions are executed from the cache and do not appear on the external bus.

Software Analyzer

The HP E2498A can be used with the B4620A software analyzer on the prototype analyzer. This allows you to time-correlate an acquired trace to written code. The B4620A software analyzer works by using the information provided in your object file to build a database of source files, line numbers and symbol information.

IEEE 695, OMF X86, Elf/Dwarf, A.OUT, and TI COFF symbol files are supported.

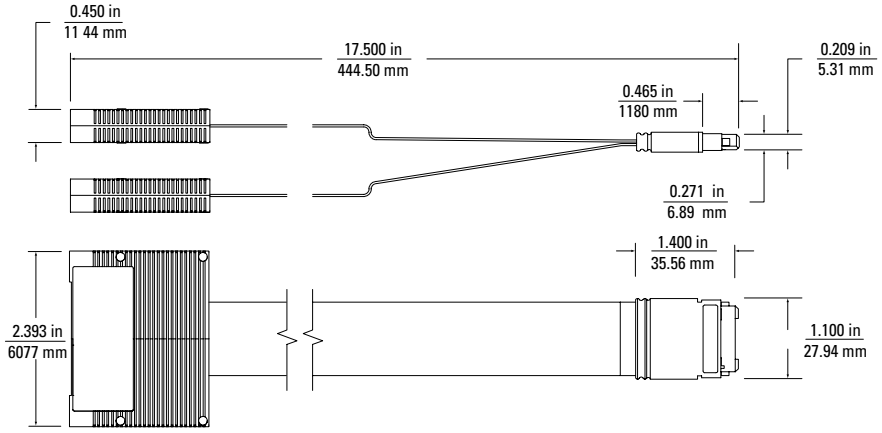


Figure 6. High-Density Termination Adapter Cable Dimension

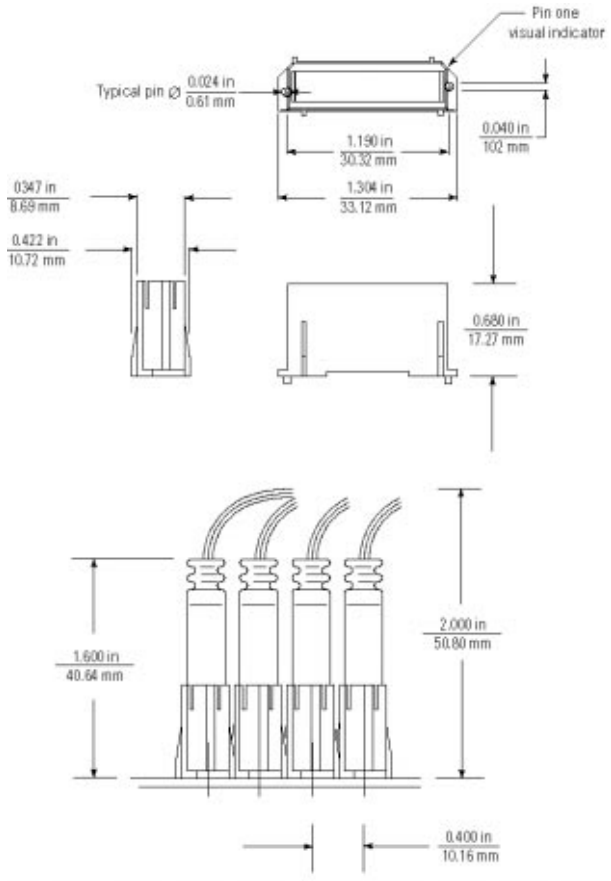


Figure 7. Support Shroud Dimensions

Related HP Literature

Pub # 5965-5475E: HP E5346A and E5351A High Density Adapters
Pub # 5962-8620E: Minimizing Intrusion Effects when Probing with a Logic Analyzer

Product Ordering Information

HP E5346A: High-Density Termination Adapter
HP E5346-68701: Kit of 5 Mictor Connectors and 5 Support Shrouds
HP E5346-63201: High-Density Right Angle Adapter
HP E 5346-44701: High-Density Termination Adapter Support Shroud
HP E2498A: Motorola/IBM Power PC 740/750 Inverse Assembler
AMP PN 2-767004-2: AMP Mictor Connector

Pinout Information of Required Signals for Inverse Assembly

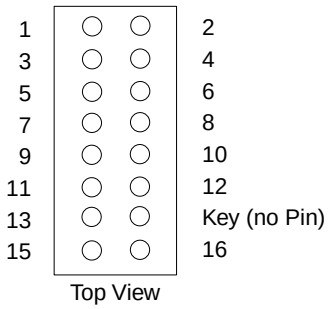
* J1-J4 are required for inverse assembly. J5 is optional.

Mictor conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J1	38	A31(LSB)	J1	37	A15
	36	A30		35	A14
	34	A29		33	A13
	32	A28		31	A12
	30	A27		29	A11
	28	A26		27	A10
	26	A25		25	A9
	24	A24		23	A8
	22	A23		21	A7
	20	A22		19	A6
	18	A21		17	A5
	16	A20		15	A4
	14	A19		13	A3
	12	A18		11	A2
	10	A17		9	A1
	8	A16		7	A0
	6	SYSCLK		5	
J2	38	ABB	J2	37	DBB
	36	ARTRY		35	TS
	34	QREQ		33	SRESET
	32	AACK		31	TEA
	30	BG		29	TA
	28	DBG		27	DRTRY
	26	DBWO		25	INT
	24	GBL		23	TT4
	22	CI		21	TT3
	20	WT		19	TT2
	18			17	TT1
	16			15	TT0
	14	BR		13	TBST
	12	CKSTP_OUT		11	TSIZ2
	10	CKSTP_IN		9	TSIZ1
	8	HRESET		7	TSIZ0
	6	QACK		5	

Mictor conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J3	38	DL31(LSB)	J3	37	DL15
	36	DL30		35	DL14
	34	DL29		33	DL13
	32	DL28		31	DL12
	30	DL27		29	DL11
	28	DL26		27	DL10
	26	DL25		25	DL9
	24	DL24		23	DL8
	22	DL23		21	DL7
	20	DL22		19	DL6
	18	DL21		17	DL5
	16	DL20		15	DL4
	14	DL19		13	DL3
	12	DL18		11	DL2
	10	DL17		9	DL1
	8	DL16		7	DL0(MSB)
	6			5	DBDIS
J4	38	DH31(LSB)	J4	37	DH15
	36	DH30		35	DH14
	34	DH29		33	DH13
	32	DH28		31	DH12
	30	DH27		29	DH11
	28	DH26		27	DH10
	26	DH25		25	DH9
	24	DH24		23	DH8
	22	DH23		21	DH7
	20	DH22		19	DH6
	18	DH21		17	DH5
	16	DH20		15	DH4
	14	DH19		13	DH3
	12	DH18		11	DH2
	10	DH17		9	DH1
	8	DH16		7	DH0(MSB)
	6			5	
J5	38	PLL_CFG3	J5	37	DP7
	36	PLL_CFG2		35	DP6
	34	PLL_CFG1		33	DP5
	32	PLL_CFG0		31	DP4
	30	LSSDMODE		29	DP3
	28			27	DP2
	26			25	DP1
	24			23	DP0
	22			21	TLBISYNC
	20			19	TBEN
	18	SMI		17	RSRV
	16	MCP		15	
	14	AP3		13	
	12	AP2		11	
	10	AP1		9	L2_TSTCLK
	8	AP0		7	L1_TSTCLK
	6			5	

HP E3454A Processor Probe Interface Information

The run control interface must be designed onto the target system using a 16-pin BERG style connector with the following pinout:



Header Pin No.	PPC 740/750 I/O	Signal Name	Resistor
1	Out	TDO	
2		NC	
3	In	TDI	1KΩ pulldown
4	In	TRST	10KΩ pullup
5		NC	
6		Power*	1KΩ series
7	In	TCK	10KΩ pullup
8		NC	
9	In	TMS	10KΩ pullup
10		NC	
11	In	SRESET	10KΩ pullup
12		NC	
13	In	HRESET	10KΩ pullup
14		KEY	
15	Out	CHECKSTOP	1KΩ pullup
16		GND	

Table 1. JTAG Interface Connections

*** The +POWER signal is sourced from the development board and is used as a reference signal. It should be the power signal being supplied to the processor (either +3.3V or +5V) It does not supply power to the HP processor probe.**

Note: NC Refers to No Connect

Notes and Information:

1. **HRESET, SRESET, and TRST from the JTAG connector must be logically Ored with the HRESET, SRESET, and TRST signals that connect to the PROCESSOR on the target system. They cannot be "dotted or "wire-ORed" on the board.**

2. **If the target board does not use the QACK signal, the board must have a pulldown resistor to pull this signal low. This allows the PowerPC to enter the state required for reading and writing processor scan string data.**

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You can also contact one of the following centers and ask for a test and measurement sales representative.

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