Agilent Technologies
Innovating the HP Way

High-Frequency Transistor Primer

Part IV

GaAs FET Characteristics

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Introduction

This primer (number four in a series) offers a brief explanation of the terms commonly used in Agilent Technologies GaAs FET data sheets, advertisements and other technical communications. Some of these terms are virtually self-explanatory and are included here primarily for the sake of completeness. Others are more specialized and potentially ambiguous due to a lack of terminology standardization among manufacturers and users of high-frequency transistors – the latter receive more thorough treatment here.

I. Basic Terminology

The last section of this primer is a comprehensive glossary of the important terms associated with GaAs FETs. To make it easier for the reader with little familiarity with GaAs FETs, however, a few of the most basic terms are presented here.

GaAs: Gallium Arsenide. A semiconductor compound.

FET: Field **E**ffect **T**ransistor. A type of transistor in which the current is controlled by the application of a varying electric field.

GaAs FET: A field effect transistor made from gallium arsenide.

Source, Drain and Gate: The three basic elements of an FET. Their functions will be explained in the text.

Epi layer: A very thin (*epi*taxial) layer of semiconducting GaAs grown on an insulating GaAs wafer.

Dopant: A material added to GaAs to make it semiconducting.

Schottky Barrier: A diode formed by a rectifying metal-semiconductor junction in which majority carriers carry the current flow. Used as the gate contact in GaAs FETs.

II. Transistor Structure

A. What Is a GaAs FET?

A basic depletion mode field effect transistor (FET) is a three port device in which the gate controls the flow of current from the source to the drain by varying the electric field and thus a depleted carrier region in the semiconducting epitaxial layer, beneath the gate (See Figure 1). A GaAs FET (or GaAs MESFET for **Me**tal **S**emiconductor) is simply an FET with a diode gate structure (similar to a junction FET, but a surface device) made from gallium arsenide (GaAs) which is a compound, as opposed to silicon, which is an element.

A FET is a semiconductor analog to a triode vacuum tube. The gate acts as the control element as does the grid in the triode. The source acts as the cathode and the drain as the plate (anode). The conductivity of the epi layer under the gate, and thus the flow of current, is varied by applying a voltage to the *gate* which is of negative polarity with respect to the *source*, while in a triode vacuum tube the *grid* is biased negative with respect to the *cathode*. The *drain* terminal of the FET is biased positive with respect to the *source*, just as the *plate* of a triode is biased positive with respect to the *cathode*.

B. Active Layer Fabrication

There are several ways to fabricate the semiconducting active layer of GaAs FETs. The two main approaches are: *Epitaxial growth* where the active layer of doping impurities is grown on the top of the substrate crystal by the liquid-phase, vapor-phase or molecular beam process; and *Ion implantation* where the doping impurities are injected directly into the crystal lattice of the substrate material (which may have an undoped epitaxial layer already fabricated – or implanted – on it by the vapor-phase process).

Agilent Technologies presently uses two approaches for GaAs FET active layer growth: Vapor phase epitaxy (VPE) and ion-implantation (I^2). The DC and RF performance of devices produced by the two approaches is virtually the same.

C. Metallization Systems

The combination of metals used to make contact to the three GaAs FET device elements (source, gate and drain) is crucial to both the reliability and performance of the device. The source and drain contacts, through which *all* of the drain current flows, must be of *very low* resistance and high stability to insure optimum device performance. Agilent Technologies presently uses a proven alloyed gold-germanium-nickel contact (Au-Ge-Ni) for contacts to GaAs FET source and drain elements.

Several different metal systems have been used by transistor manufacturers to make the Schottky-barrier diode gate contact; the two main approaches being aluminum and gold-based systems.

Aluminum creates a good Schottky barrier on GaAs, and aluminum atoms do not diffuse easily into the GaAs – such diffusion would change the device characteristics. However, aluminum is an active element and can form intermetallic compounds, particularly at the Au-Al interface, and is relatively susceptible to damage from electrostatic discharge and high RF energy levels. Gold, on the other hand, is the element which is most stable in the presence of oxidants, and is less susceptible to electrostatic or RF damage. It does, however, diffuse quickly into GaAs and, therefore, in order for gold to be used as a gate metal, barrier metals must be introduced between the gold and the GaAs. Agilent Technologies uses titanium (Ti) and tungsten (W) as barrier metals in its gold-based gate metal system. This metallization has proven to provide both high reliability and excellent mechanical and electrical performance.

D. FET Dimensions Affecting Microwave Performance

The important dimensions in FETs are the spacing from the source to the gate, and from the gate to the drain. For microwave operations, the most critical dimension is the “length” of the gate along the carrier (electron) path. The shorter the gate length, the

higher becomes the signal frequency which can be controlled by the depletion layer set up in the active channel beneath the gate. The spacing between the gate electrode and the source, and gate and drain introduces capacitance. If the FET is to handle larger amounts of signal current, the gate width must be increased appropriately. Viewing the FET pictorially (Figure 1) helps to understand that the "width" dimension is perpendicular to the carrier flow along the length of the channel from source to drain. RF power handling capability is proportional to this gate width. In general, the transconductance (g_m) – the influence of gate voltage on drain current – and the capacitances increase proportionally with increasing gate width while the resistances vary inversely with the width. Doubling the gate width doubles the transconductance and the feedback capacitance and halves the resistance.

E. Why a GaAs FET Instead of a GaAs Bipolar or Silicon Transistor?

The advantage of GaAs over silicon is that with GaAs the carriers (electrons, or electrons and holes) can reach about twice the limiting velocity with one third the applied bias voltage. Therefore, for a given geometry, a given current gain can be reached at more than twice the frequency as with silicon. However, because of the more difficult physical chemical properties of GaAs, the variously doped layers of the bipolar structure (emitter, base and collector), would be difficult to form in GaAs (GaAs bipolar transistors would also be undesirable because of the low mobility of P-type GaAs material).

The structure used for GaAs FET fabrication, while somewhat similar to that of the silicon junction field-effect transistor – with a reverse-biased diode acting as the gate, and operation in the depletion mode – is totally a surface structure. There are no vertically diffused elements, such as the "buried" base layer between the emitter and collector which is used in a silicon bipolar transistor, or the "buried" channel in a silicon JFET. This is the only technique which can tap the advantages offered by GaAs with present fabrication technology. The FET surface structure can be used with GaAs and the necessary FET half-micron geometry for microwave frequency operation can be fabricated routinely with the present state of the art in optical photolithography techniques.

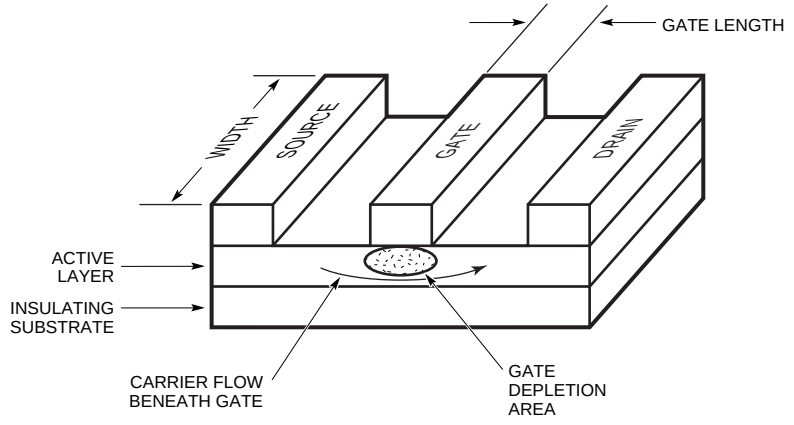

Figure 1. Basic GaAs FET Structure

There is one theoretical advantage of an FET structure as an amplifier, unrelated to the semiconductor material: the potential for low distortion. The FET is a square-law device, with its drain current proportional to the square of the ratio of the gate voltage to the pinchoff voltage.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$V_{GS(OFF)} = V_P = \text{Pinchoff Voltage} \qquad (1)$$

This means that it generates little odd-order distortion, and that the small amount of even-order distortion that it does generate can easily be suppressed with a balanced-stage circuit design. An FET looks like a biased capacitor in a circuit, while a bipolar transistor looks like a forward-biased diode junction.

III. How Does the FET Work?

Gain in an FET is proportional to the channel conductivity (the "channel" being that area within the epi material under the gate). In a depletion mode FET (of which the GaAs FET is an example), as the gate is biased more negatively, the actual conducting channel cross-section is reduced, and the drain current is also reduced. A small negative voltage applied to the gate starts to "deplete" the channel of carriers, beginning immediately adjacent to the gate electrode at the top of the channel. As the gate voltage is made increasingly negative, the

gate depletion layer is extended further into the channel until it reaches the semi-insulating GaAs substrate. When the gate is made sufficiently negative, the channel is closed, or "pinched off", and no current flows. The gate voltage at which drain current is stopped is called the *pinchoff voltage* (V_P).

Drain current will be highest, and the gain of the GaAs FET will be highest when the gate voltage is zero with respect to the source -- that is, with the gate connected directly to the source. This is the "saturated" drain-to-source current condition or I_{DSS}.

IV. Electrical and Performance Characteristics

Electrical characteristics may be described as uniquely defined, measurable electrical properties of the transistor which are not a function of the measuring circuit of apparatus (except insofar as standard terminations and measurement accuracy are concerned). Performance or operating characteristics are also electrical properties, but they are, in general, not unique because their values depend upon the measuring circuit (in particular, the source and load impedance, which may be arbitrary). As might be expected, these terms are often used somewhat loosely (and sometimes interchangeably), especially in cases where there are only subtle differences involved. The terms are generally used on transistor data sheets to segregate (for emphasis) under performance or operating characteristics those properties most directly applicable to the expected application.

A. Performance (Operating) Characteristics

The most fundamental characteristics specified for microwave GaAs FETs are:

1. Noise Figure
2. Gain at Noise Figure
3. Maximum Available Gain
4. Linear Power Output
5. Associated Small Signal Power Gain
6. Efficiency
7. Forward Transducer Gain

All of these characteristics are, of course, functions of frequency, bias, temperature, etc., and to completely characterize a transistor over its full frequency, bias and temperature ranges would be prohibitively costly. Consequently, characterization data is given only for restricted ranges of these variables. This data should portray sufficiently the capabilities of a particular device for its primary intended applications. As in the case of maximum ratings, some applications may require additional characterization by the user or applications assistance from the manufacturer.

1. *Noise Figure* – NF_O

Noise factor is a numerical value which is the common measure of the noise generated by an active two-port device – noise which sets a lower limit on amplifier sensitivity. This may be defined as:

$$F = \frac{\text{Input Signal-to-Noise Ratio}}{\text{Output Signal-to-Noise Ratio}} \qquad (2)$$

or, more generally,

$$F = \frac{\text{Total Output Noise Power}}{\text{Output Noise Power Due To Signal Source Resistance}} \qquad (3)$$

At high frequencies, the spot noise factor, or noise factor at a small bandwidth (say 1%), is used, and is usually expressed as noise figure, NF, in decibels, e.g.

$$NF = 10 \text{ Log } F \qquad (4)$$

As already discussed, noise figure is a function of source impedance (as well as being a function of frequency, bias, etc.), and hence there is an infinity of noise figures associated with a given device corresponding to the infinity of possible impedances which may be presented to the device output. The only unique noise figure, in the sense that it does not involve arbitrary source impedances, is NF_O, the minimum noise figure obtained (at given bias and frequency) when the input is tuned to optimize this parameter. It is this noise figure which is usually given on Agilent Technologies data sheets.

In practical amplifiers, involving more than one stage, the overall *numeric* noise measure, F_m, is given by:

$$F_m = F_1 + \frac{F_2 - 1}{G_1} + \ldots + \frac{F_n - 1}{G_{(n-1)}} \qquad (5)$$

$n =$ Number of Stages,
$G =$ Gain of nth Stage,
$F_n =$ Noise Factor of nth Stage

This expression emphasizes the important fact that for low noise

amplifiers the first stage must be designed for the lowest noise figure and highest gain possible. Note that the noise contribution of the second stage is divided (reduced) by the gain of the first stage. Since the optimum source impedances and bias currents for optimum gain and noise figure do not often coincide, very careful circuit design is required to minimize overall noise figure.

2. *Associated Gain at Noise Figure* – G_A

This gain is simply the small-signal gain that results from optimum noise figure tuning of the circuit in which the device is installed. Best noise matching of the input of the transistor does not necessarily coincide with conjugate input S-parameter match (S_{11}*), and therefore gain at noise figure is usually lower than the maximum available gain.

3. *Maximum Available Gain* – MAG

Of the various definitions for the measure of power flow in an active two-port device, such as a transistor, two are unique enough to allow specification without recourse to specifying the complete measuring circuit in detail. One of these definitions is termed maximum available gain, MAG. It is the power gain obtained when the input and output ports are simultaneously conjugately matched to source and load impedances, respectively. Implicit in the definition is the assumption that the two-port device is unconditionally stable: i.e., no combination of input and output tuning can result in increasing the gain of the device to the point of oscillation.

The other definition of power flow is Maximum Stable Gain or MSG. This definition is used when stability is only conditional and is the maximum gain possible with stable operation.

4. *Power Output*

This characteristic is important for both amplifier and oscillator transistors. In both cases, it is extremely circuit sensitive. For amplifiers, the maximum useful power output is often limited to that power output level ($P_{1\ dB}$) at which gain has compressed 1 dB ($G_{1\ dB}$), an indicator of the upper limit of linearity range, or may be specified at a greater gain compression, such as 2 dB or 3 dB (P_{sat}), when output power is more important than linearity. For oscillators, power output is merely a quantitative measure of RF power output for a given DC input power.

5. *Associated Small Signal Power Gain* – G_P

This gain is determined by decreasing the input power to the point that the device is operating in its linear region and then measuring the gain. This gain level will be lower than MAG primarily because the output is conjugately matched for large signal conditions and some mismatch occurs when signal levels are reduced.

6. *Power Added Efficiency* – η_{add}

The most commonly used efficiency expression for GaAs FET power devices is the *power added efficiency* which is defined as:

$$\eta_{add} = \frac{P_O - P_{IN}}{P_{dc}} \bullet 100\% \qquad (6)$$

where

P_O = R_F Output Power
P_{IN} = R_F Input Power
P_{dc} = Total DC Input Power (7)

7. *Forward Transducer Power Gain* $|S_{21}|^2$

The other unique power gain is the gain realized when the transistor is inserted between a source and load with identical impedances (in practice usually 50 + j0 ohms). This particular insertion or transducer gain happens to coincide with the usual definition of the two-port forward scattering parameter, S_{21}. More precisely, it is equal to the magnitude-squared of this parameter and is therefore often identified by the symbol $|S_{21}|^2$. For wideband applications, $|S_{21}|^2$ is important since wideband terminations “not-too-different” from 50 ohms are more easily realized than are wideband transforming networks which provide the precise matching required for MAG.

B. Electrical Characteristics

Electrical characteristics may be conveniently classified into two types, DC and AC.

1. *DC Characteristics*

The importance of DC characteristics of high frequency transistors lies primarily in biasing and reliability considerations. However, certain DC characteristics are also directly related to high frequency performance. For example, high-frequency noise figure is affected by the DC current gain. The DC characteristics which are discussed here are those usually found on high-frequency transistor data sheets.

a. *Transconductance* – g_m

This parameter is the DC common-source conductance; that is the incremental change in output (drain) current with a given change in input (gate) voltage. It is usually specified at either I_{DSS} (gate voltage = 0 V) or one-half I_{DSS} although any current value or specified percentage of I_{DSS} can be used as the measurement point.

$$g_m = \frac{\Delta I_{ds}}{\Delta V_{gs}} \qquad (8)$$

b. *Pinchoff Voltage* – V_P

This parameter is the gate voltage at which the drain-to-source current is reduced to some given value (usually 1 mA for small signal FETs and 5 mA for power FETs). See point A on the curves in Figure 2.

c. *Saturated Drain-to-Source Current* – I_{DSS}

This current occurs when the gate-to-source voltage is held to zero and the drain-to-source voltage set to a specified (usually 3 volts) value. See point B on Figure 2 curves.

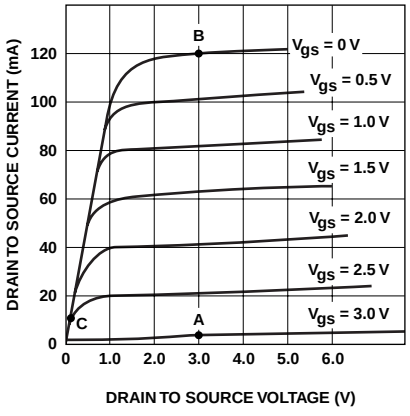

Figure 2. Typical GaAs FET DC Characteristic

d. *Low-Field Channel Resistance* – R_{do}

This is the slope of the drain I-V characteristic near the origin of the curve and is an indicator of the active channel resistivity and the drain and source contact quality. See the region around point C on Figure 2 curves.

e. *Breakdown Characteristics*

The breakdown characteristics of the gate contact can be measured in both directions (gate-to-drain and gate-to-source). In general, since the device is close to physically symmetrical, only one of the two is needed to verify device quality. Most often the gate-to-drain characteristics are used. There are two ways of characterizing the breakdown characteristics: Specifying the gate-to-drain current and measuring the voltage at that point (BV_{gd}), or specifying the voltage and measuring the reverse current (I_{gd}). In either case they are go-no-go type tests, failing when either the reverse current exceeds the specified value or the breakdown voltage is lower than the specified value, and are non-destructive as long as the current levels are kept low (in the μA range).

2. *AC Characteristics*

Of the numerous AC characteristics which are defined for transistors, only relatively few are commonly used in characterizing high-frequency transistors. Some of the more pertinent parameters are briefly covered here.

a. *S-Parameters*

The standard definitions of S-parameters are covered in a variety of sources including volumes one and two of this Primer series. That information will not be repeated here. What will be discussed is the measurement technique and fixturing utilized in Agilent Technologies' transistor S-parameter measurements.

Packaged device S-parameters are measured in 50 ohm test fixtures* using Agilent Technologies' TFP microstripline or TF coaxial test fixtures. The test fixture introduces errors which can be corrected by either a reference plane extension or a THRU/DELAY calibration[1]. The most accurate data for frequencies above 6 GHz uses the THRU/DELAY calibration, which is also referred to as de-embedded S-parameter data. This is the data in the Agilent Technologies RF Semiconductor Designers Catalog.

Chip devices are measured in the 50 ohm microstripline test fixture shown in Figure 3. The S-parameter data should be de-embedded for frequencies above 6 GHz. At present, bonding wire inductances are *not* subtracted out of the chip S-parameter values. A sketch of the standard chip test carrier is shown in Figure 3.

b. f_{max}

The maximum frequency of oscillation, f_{max}, is the frequency at which a curve of unilateral power gain (U) vs. frequency intercepts zero dB gain. The gain of both bipolar and FET transistors drops at a rate of approximately 6 dB per octave in the microwave region. If gain is measured at convenient

* TFP test fixtures and de-embedding software are available from *Intercontinental Microwave*, 2370B Walsh Ave., Santa Clara, CA 95051.

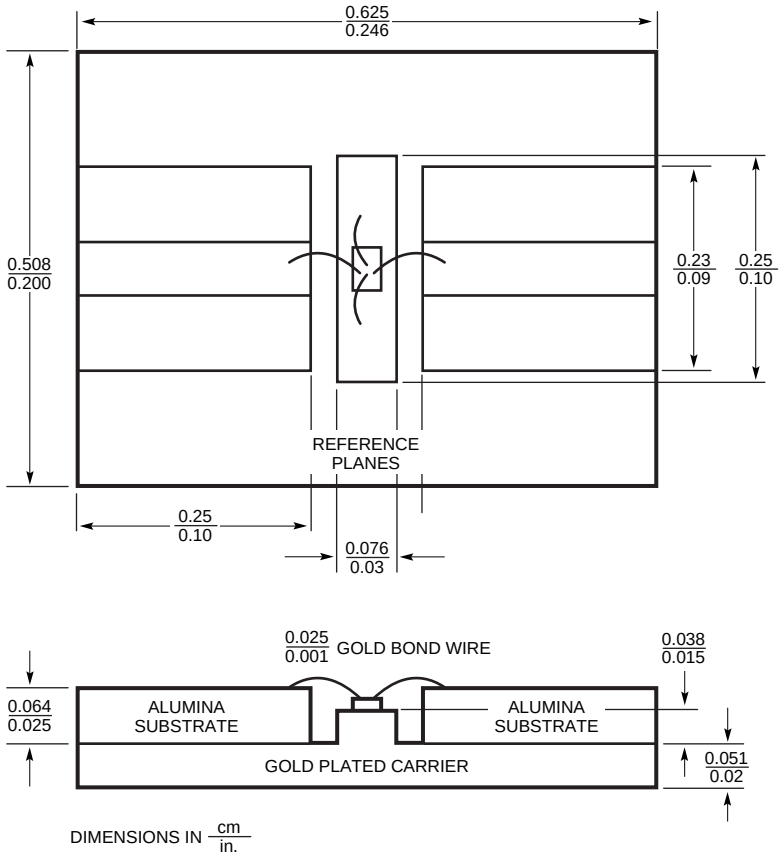

Figure 3. Test Carrier Used to Characterize Unpackaged GaAs FET Chips

frequencies between 2 and 12 GHz the points will approximately fit a straight line curve when gain in dB is plotted on a linear vertical scale against frequency plotted on a log scale horizontally. The frequency at which the unilateral power gain extrapolates to 0 dB gain is f_{max}.

c. *Gate-to-Source Capacitance* – C_{gs}

This capacitance measurement is usually made at 1 MHz, and varies with the value of DC voltage applied to the gate. A zero-volt measurement is used most often to give an idea of the gate metallization area or, more precisely, the gate length. For a given device gate width, the capacitance is directly proportional to gate length. A negatively-biased gate will result in a lower value of capacitance, because carriers have been depleted in the region under the gate. This value is more useful in estimating the gate capacitance for RF performance or device modeling.

V. Maximum Ratings

(Also refer to *Agilent Technologies High-Frequency Transistor Primer, Part I*, Section II for additional information.)

In addition to the normal maximum ratings defined for GaAs devices, which limit externally-applied stress to values below those which, if exceeded, may result in irreversible damage to the device, some manufacturers are including ratings called "recommended maximums for continuous operation." This latter set of ratings may be interpreted as the values above which the life expectancy of the device may be shortened. Of course, in situations where the device lifetime is less important than achieving the maximum possible performance, these ratings may be intentionally exceeded through any combination of temperature, voltage or current conditions.

The following parameters normally appear on Agilent Technologies GaAs FET data sheets, and provide adequate information for most applications.

A. Voltage Ratings

GaAs FET voltage ratings are usually derived from, and usually coincide with, the minimum device breakdown voltages. However, since this is not *always* true, it has become common practice to include both maximum voltage ratings and minimum breakdown voltages on data sheets.

It can be argued that such practice erodes the meaning of maximum ratings. Since, strictly speaking, maximum ratings should not be exceeded under any circumstances, strict adherence to the voltage ratings would preclude the measurement of the breakdown voltages of any but marginal devices. In fact, drain-to-source breakdown voltage measurements may be destructive tests except when conducted using a sophisticated pulsed measurement technique. Gate-to-source and gate-to-drain breakdown voltages can be measured without damage to the device, since there is no avalanche characteristic in these breakdown phenomena.

B. Current Ratings
The maximum current ratings for GaAs FETs are derived from a number of considerations, including the current-carrying capacity of the bonding wires and the performance degradation which can be produced by excessive current causing physical changes in the active region. Maximum ratings are normally only specified for *drain* current.

C. Dissipation Ratings
Besides the individual voltage and current ratings, there is also a limit to the product of voltage and current which can be safely handled by a GaAs FET. That is, there is a power dissipation rating which must be adhered-to for any device. Since the power dissipation capability of a GaAs FET is a function of the temperature of the external environment, the power dissipation rating is specified at a specific temperature or over a stated temperature range. For the DC case, this is usually the only significant functional dependence.

In the AC case, device dissipation varies significantly with time, so that power dissipation capability becomes a generally complex function of the signal waveform. Due to the complexity of the general AC case, transistors are seldom characterized completely enough to include complete AC power dissipation rating information. Most transistors are rated only in terms of maximum continuous dissipation – the maximum DC and maximum average dissipation. This rating is typically specified in terms of a maximum continuous dissipation at or below a stated reference temperature (usually 25°C), with a linear derating factor to be applied at higher temperatures.

Two external temperature reference points are commonly used. The one which is the more valid depends on the application. They are:

1. *Air ambient*, T_A, also known as free air temperature, since no forced-air or other "artificial" cooling is applied to the transistor. This is the air temperature in proximity to the transistor case as mounted in its normal manner.
2. *Case ambient*, T_C, which is the temperature of the point on the transistor package at which a heatsink is the most effective in reducing temperature.

D. Channel Temperature Rating
Another temperature reference point implicit in the previously-mentioned ratings, is the actual temperature at the transistor channel. The maximum internal reference temperature $T_{ch\ (max)}$ corresponds to the maximum channel temperature, since at $T_{ch\ (max)}$, the power dissipation of the transistor must be derated to zero. Strictly speaking, channel temperature is not properly classified as a *maximum* rating, since it is not an external stress under the direct control of the user – as opposed to power dissipation and external operating temperature which *are* user-controlled.

Thus, a more appropriate term for this rating would be *maximum operating temperature*. However, since it is a limiting factor in the transistor power dissipation capability, and since its use simplifies time-varying thermal analysis, this rating still appears on many transistor data sheets.

One key factor that should be kept in mind when specifying operating bias and calculating channel temperature is that the thermal resistance of GaAs is not constant with temperature. The thermal resistance from channel to case is a function of temperature and varies directly as the thermal resistance of bulk GaAs. This temperature variation can be approximated as:

$$\theta_{jc} = \theta_{jc}(60°C)\left\{1 = 0.00355\left(T_{CH} - 60°C\right)\right\} \quad (9)$$

where T_{CH} equals channel temperature and θ_{jc} (60°C) is the channel-to-case thermal resistance at a T_{CH} of 60°C. For a more complete discussion of thermal resistance, refer to Agilent Technologies' *High Frequency Transistor Primer Series, Part III (Thermal Properties) and Part IIIA (Thermal Resistance)*.

E. Storage Temperature Rating
This rating defines the range of temperature over which the transistor may be stored in a non-operating condition, without damage. Because of possible electrical-temperature interactions, the storage temperature range and operating temperature range do not necessarily coincide. In practice, however, they usually *do* coincide and, in the absence of stated restrictions on operating temperature range, storage temperature range may be taken to be the operating temperature range as well.

VI. Glossary of GaAs FET Terms

Active layer
The doped layer of gallium arsenide (GaAs) through which the electrons flow in a GaAs FET and upon which the source, gate and drain electrodes are placed. The region between the source and drain electrodes is known as the channel.

Avalanche breakdown
The application of excessive voltage to a semiconductor material creates an excess of high-energy (or hot) electrons. These electrons can excite additional carriers into a high-energy state, which makes the semiconductor more conductive and can, with the same voltage applied, result in a high current flow with resulting destructive breakdown of the material. Drain-to-source breakdown in a GaAs FET is an avalanche effect.

Bipolar
Refers to a transistor in which both majority and minority carriers (electrons and holes) carry current, and which is formed with PN junctions.

Breakdown voltage
The reverse bias voltage at which a rectifying junction begins to conduct a large reverse current (higher than normal reverse leakage). Reverse breakdown can be caused by avalanche breakdown (see entry) or by other electrical or thermal effects. Gate-to-source and gate-to-drain breakdown in a GaAs FET are not avalanche effects, and may take place without damage to the device so long as the reverse current is limited to a safe value.

BV_{GD}
Breakdown voltage, gate-to-drain – The reverse breakdown characteristic of the gate-drain Schottky-barrier diode in a GaAs FET. BV_{GD} is usually specified at some specific value of leakage current.

BV_{GS}
Breakdown voltage, gate-to-source – The reverse breakdown characteristic of the gate-source Schottky-barrier diode. BV_{GS} is usually specified at some value of leakage current.

Depletion layer
The portion of the epitaxial layer that lies directly beneath the gate of an FET and becomes depleted of carriers (electrons) when a negative bias is applied to the gate.

Dopant
A substance added to GaAs (or silicon or other transistor base material) to make it semi-conductive.

Drain
The terminal of an FET to which electrons flow. (See also: source, gate)

C_{GS}
Capacitance, gate-to-source – The capacitance that exists between the gate and source electrodes in a GaAs FET, and which is dependent on the Schottky diode characteristics and applied bias voltage.

Conjugate match
A transistor input or output port is conjugately matched when connected to an impedance which has the same resistance as the transistor port and a reactance of the same magnitude but opposite sign. This means that the reactances cancel, and that maximum power transmission takes place and that there is no mismatch loss.

Epitaxial (epi) layer
A doped layer of GaAs grown on top of the substrate crystal as a continuation of the crystal lattice structure. Gallium, arsenic and other dopants are carried to the substrate surface in a variety of ways, including liquid-phase, vapor-phase and molecular beam approaches.

f_{max}
Maximum Frequency of Oscillation – The frequency at which the unilateral power gain (U) of a transistor approaches unity.

FET
Field Effect Transistor – A unipolar device in which the number of carriers available to carry current in the conducting region is controlled by the application of an electric field to the surface (in the form of a capacitor or reverse-biased diode junction) of the semiconductor. As a unipolar device, the current in an FET is carried only by the free majority carriers (in an N-channel FET, *electrons*) in the conducting channel and there is little or no current carried by the minority carriers (in an N-channel FET, *holes*). Compare this to the bipolar transistor in which both positive and negative free carriers carry approximately equal current.

GaAs
Gallium Arsenide – A type III-V (from the periodic table) compound of gallium and arsenic which has a resistivity sufficiently high to fabricate field-effect

transistors. Compared to silicon, the free carriers can reach about twice the limiting velocity with one-third the applied voltage.

GaAs FET
A field effect transistor made of gallium arsenide.

Gate
The terminal of an FET that controls the flow of current from the drain to the source. (See also: drain, source)

Gate length
The distance along which the electrons must travel when moving from source to drain. That is, length is the *shorter* of the two gate dimensions (gate width is the longer dimension). The frequency response of a GaAs FET, with all other things equal, is inversely proportional to its gate length.

Gate width
The size of the GaAs FET channel that carries current. That is, width is the longer of the two gate dimensions (gate length is the shorter dimension). The power handling capacity of a GaAs FET, with all other things equal, is directly proportional to its gate width.

$G_{1\ db}$
1 dB gain compression point -- The level of gain from a device which is 1 dB less than the gain measured under small signal conditions when the device is tuned at $G_{1\ dB}$. This is usually considered to be the upper limit of linear amplification. See also $P_{1\ dB}$.

g_m
DC transconductance, which is the ratio of the change in the drain current to changes in gate voltage:

$$g_m = \frac{\Delta I_{ds}}{\Delta V_{gs}} \qquad (10)$$

G_{NF}
Small signal gain, resulting from tuning for optimum noise figure. Also designated: G_A.

G_P
Small signal gain, resulting from tuning for optimum output power.

G_T
Transducer power gain – The insertion power gain of a transistor, with no assumptions made concerning S_{12}, S_{11}, S_{22} or the source or load impedances. The maximum value of G_T for an unconditionally stable transistor is MAG. $|S_{21}|^2 = G_T$ when the source and load impedances equal 50 Ω.

G_{Tu}
Unilateral transducer power gain – Transducer power gain with S_{12} assumed equal to zero.

I_{DSS}
Saturated drain-to-source current – The current that results from a given voltage applied to the GaAs FET with the gate voltage held at zero.

I_{GD}
Gate-to-drain leakage current at a stated reverse gate-to-drain voltage.

I_{GS}
Gate-to-source leakage current at a stated reverse gate-to-source voltage.

Implanted layer
An active layer formed by the implantation of dopants directly into the substrate crystal, or an insulating layer produced by vapor-phase epitaxy.

MAG
Maximum available gain, at a frequency where the transistor is unconditionally stable and the input and output ports are simultaneously conjugately matched. Also designated: $G_{A\ (max)}$, G_{max}.

MESFET
Metal Semiconductor Field Effect Transistor – A GaAs FET can more formally be described as a GaAs MESFET.

NF_O
A measure of the noise generated by a transistor when tuned for minimum noise figure at a given frequency. Also designated NFmin and NFopt.

NF_{50}
Noise figure of a transistor at a given frequency, when inserted in an untuned 50 ohm circuit. This figure is most often used for the calculation of noise resistance.

$P_{1\ dB}$
Power output at the 1 dB gain compression point – Essentially the maximum output power available from the transistor while providing linear amplification. Also designated: P_{OUT}, $P_{O\ -1\ dB}$, and in numerous other ways. See also $G_{1\ db}$.

P_{sat}
Saturated power output – Usually specified at some level of small signal gain compression, such as 2 dB or (most usually) 3 dB.

P_{max}
Maximum continuous power dissipation at or below a stated reference temperature (usually 25°C), or linearly derated at a higher ambient temperature.

R_{do}
Low field drain-to-source resistance – The slope of the drain I-V characteristic near the origin of the curve, and an indicator of the active channel resistivity and the drain and source contact quality.

R_N
Equivalent noise resistance, used in the GaAs FET model to predict noise figure performance.

S_{11}
S-parameter input reflection coefficient – Expresses the magnitude and phase of the input match with respect to a pure resistance of 50 ohms.

S_{12}
S-parameter reverse transfer coefficient – Expresses the reverse isolation magnitude and phase, measured with the input terminated in 50 ohms.

S_{21}
S-parameter forward transfer coefficient – Expresses the forward gain amplitude and phase, measured with the input terminated in 50 ohms.

S_{22}
S-parameter output reflection coefficient – Expresses the magnitude and phase of the output match with respect to a pure resistance of 50 ohms.

Schottky diode
A rectifying junction formed by depositing a layer of metal onto the surface of a semiconductor. This creates an electrostatic barrier which gives the metal-semiconductor interface rectifying properties, with the metal acting as the anode and the N-type semiconductor as the cathode. Since the Schottky diode is a surface device, and since its metal layer can be fabricated at the same time as ohmic (drain and source) contacts, it is used to provide the gate structure of GaAs FETs. Also designated: Schottky-barrier diode, metal-semiconductor diode, hot-carrier diode.

Source
The terminal of an FET from which electrons flow (see also: drain, gate).

T_{ch}
Channel Temperature – The measured or estimated temperature of the GaAs FET channel under operating conditions.

T_{stg}
Storage Temperature – For an unbiased transistor.

V_P
Pinchoff Voltage – The gate-to-source voltage at which the drain current is reduced to some small, specified level. Also known as $V_{GS(OFF)}$.

Pinchoff Voltage
See: V_P

Transconductance
See: g_m

U
Unilateral Power Gain – The power gain of a transistor amplifier when lossless feedback has been used to neutralize the reverse transfer coefficient (S_{12}) to zero; the input reflection coefficient (S_{11}) has been matched to zero with lossless circuit elements; and the output reflection coefficient has been matched to zero with lossless circuit elements. The unilateral power gain is the highest power gain which can be achieved from the transistor, and the frequency where this gain is unity (or zero dB) is f_{max}.

Γ_o
Optimum Source Reflection Coefficient – The input source reflection which results in the lowest device noise figure. This value does not coincide with the S_{11} conjugate match. Also sometimes designated Γ_{opt}.

η_{add}
Power Added Efficiency – The ratio of RF power output minus RF input power to the DC input power:

$$\eta_{add} = \frac{P_O - P_{IN}}{P_{dc}} \bullet 100 \qquad (11)$$

VII. References

1. *Measurement and Modelling of GaAs FET Chips*, Agilent Technologies Application Note ATP-1054, 0ctober, 1983.

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5966-0779E (11/99)