Sample Test Plan for Switch Statistics

Using the HP E5200A Broadband Service Analyzer

Introduction

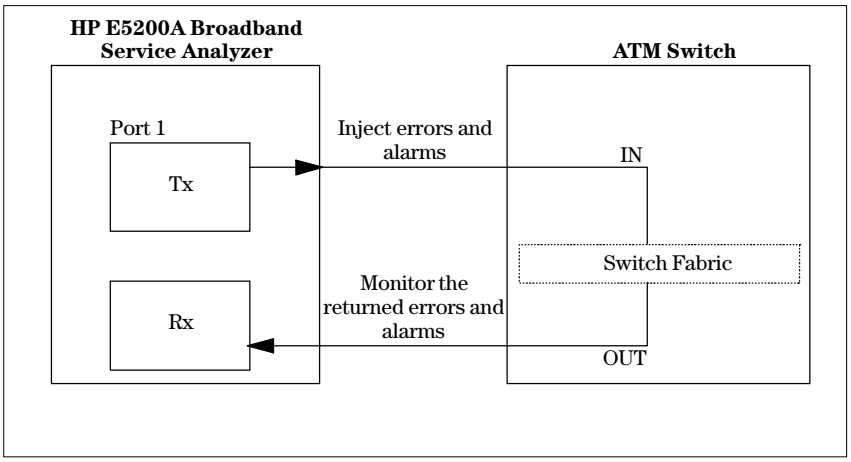
Switch statics is one of the test categories described in the *Evaluating ATM Switch Performance* solution note. This solution note provides a sample test plan and expected results for this test category.

This solution note deals with PVC (Permanent Virtual Circuit) connections carrying CBR (Constant Bit Rate) or VBR (Variable Bit Rate) services. All tests described in this paper can be performed by the HP E5200A Broadband Service Analyzer.

The service analyzer evaluates switch statistics performance in an ATM switch by measuring its response to various conditions such as

- increasing bandwidth through the switch port
- F4 and F5 OAM alarms
- high-rate OAM fault management cells (more than one cell per second)
- cell header and payload errors
- physical layer alarms and errors

HP E5200A Broadband Service Analyzer



Testing for switch statistics

Switch Statistics: Example Test Plan

Description

Test the ability of the switch to report ATM layer and physical layer alarms and error conditions.

Configuration

1. Connect the service analyzer port (Tx/Rx) to a switch port (IN/OUT) as shown on page 1.

2. Configure a PVC between the IN and OUT port connections on the switch–refer to the switch manufacturer's instructions.

Test Equipment

HP E5200A Broadband Service Analyzer with a single interface pod.

Test Procedure

For more information about how to use the simulator and monitor, refer to the HP E5200A Broadband Service Analyzer *User* online help.

Test A - Bandwidth Measurements

Generate traffic to check the bandwidth measurement capability of the switch. For example, generate ATM traffic at 10%, 20%...100% of MAXBW, where **MAXBW** is the maximum possible cell bandwidth a particular physical interface can carry (for example, OC-3 MAXBW = 149.76 Mb/s).

Test B - OAM Alarms (1 OAM cell per second)

Transmit OAM cells at the nominal 1 cell per second rate to generate OAM alarms. Check that the switch detects and responds to OAM alarms correctly. Refer to the HP E5200A *User* online help for more information about simulating OAM alarms. Generate F4 alarms VP-AIS and VP-RDI on various VPIs. Generate F5 alarms VC-AIS and VC-RDI on various VPI/VCIs. **Note:** RDI (Receive Defect Indicator) is also referred to as FERF (Far End Receive Failure).

Test C - High Rate OAM Cells

Generate high-rate OAM cells (at greater than 1 cell per second) to check that the switch performance is not degraded by processing high-rate OAM cells. For example, generate OAM cells at a rate of 10 cells per second.

Test D - Cell Header and Payload Errors

Generate cell header and payload errors to check that the ATM switch can correct single bit errors in the header. Refer to the HP E5200A *User* online help for more information about simulating ATM errors. Generate single bit errors, multiple bit errors, and bursts of errors (errors in consecutive cells) in the cell header and payload.

Test E - Physical Layer Alarms and Errors

Generate various physical layer error conditions and alarms. Monitor the response of the ATM switch. Refer to the HP E5200A *User* online help for information about the particular physical layer interface you are testing.

Test A - Bandwidth Measurements

Test Condition	Expected Behaviour of the ATM Switch
CBR traffic	Check that the switch measures the correct bandwidth transmitted by the tester. The bandwidth measurement accuracy of the switch should be within the limits specified by the manufacturer. **Note:** The test results also provide an estimate of the bandwidth resolution of the switch's traffic policing capability.

Test B - OAM Alarms (1 OAM cell per second)

Test Condition	Expected Behaviour of the ATM Switch
VP-AIS, VP-RDI at 1 cell/second (F4)	The ATM switch detects VP-AIS, VP-RDI. It sends back VP-RDI in response to VP-AIS.
VC-AIS, VC-RDI at 1 cell/second (F5)	The ATM switch detects VC-AIS, VC-RDI. It sends back VC-RDI in response to VC-AIS.

Test C - High Rate OAM Cells

Test Condition	Expected Behaviour of the ATM Switch
VP-AIS, VP-RDI, VC-AIS, VC-RDI OAM cells at greater than 1 cell/second	The ATM switch does not become overloaded when attempting to process high rate OAM cells. **Note:** In some cases, high rate OAM cells can cause the ATM switch software to crash.

Test D - Cell Header and Payload Errors

Test Condition	Expected Behaviour of the ATM Switch
Single bit errors in the cell header	The ATM switch detects and corrects single bit errors in the cell header.
Multiple bit errors in the cell header	The ATM switch discards cells with multiple bit errors in the cell header.
Bursts of single or multiple bit errors in the cell header	The ATM switch declares LOCS (Loss of Cell Synchronization) after detecting a burst of 7 or more bad headers (cells with single or multiple bit errors in the header).
Cell payload errors	No effect on the ATM switch.

Test E - Physical Layer Alarms and Errors

Test Condition	Expected Behaviour of the ATM Switch
Errors e.g. Parity, BIP	The ATM switch detects the error condition, e.g. BIP. It might send back an error count in response, e.g. FEBE.
Alarms e.g. LOS, LOF, AIS	The ATM switch detects the alarm, e.g. BIP. It might send back an alarm in response, e.g. RDI, FERF.

Test Equipment Features

Use the following features of the HP E5200A Broadband Service Analyzer to carry out switch statistics performance tests.

- **Traffic generation**
  Use the traffic simulator to control the bandwidth of the transmitted ATM traffic.

- **ATM errors and alarms**
  Use the simulation and monitoring capability of the HP E5200A to inject ATM errors into cell header or payload bytes and activate F4 and F5 OAM alarms and monitor the response of the switch.

- **Physical layer errors and alarms**
  Use the simulation and monitoring capability of the HP E5200A to inject physical layer errors and alarms and monitor the response of the switch.

- **Interface pods**
  Each interface pod has a single transmit and single receive port. Up to two interface pods can be installed in the service analyzer at one time. A range of interface pods are available including
  - E3 (34 Mb/s)
  - DS1/DS3 (1.5 Mb/s and 45 Mb/s)
  - OC-3/STM-1 (155 Mb/s) single mode and multimode optical
  - STM-1 Electrical (155 Mb/s)

Conclusions

This solution note provides examples of the types of alarm and error conditions that you can generate and monitor to evaluate ATM Switch Statistics performance.

For information on evaluating other ATM switch characteristics, refer to the *Sample Test Plan* solution notes for
- latency, jitter, and throughput (P/N 5965-6205E)
- traffic management (P/N 5965-6206E)

Other solution notes in this series deal with the end-to-end testing requirements for ATM networks including topics such as Quality of Service (QoS).

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