Cell Transfer Time Measurement Using the Parallel Cell / Traffic Generator and Analyzer

How to use the HP E4829B custom / UTOPIA Level 1 implementation for cell transfer time variation measurements

Product Note

Product Number
HP E4829B

Figure 1: HP E4829B entry system

Introduction

In order to achieve quality of service in an ATM switch, any variations in the cell transfer time of channels carrying voice data must be closely monitored. When the delay variation exceeds certain limits, the quality of voice sent to the user is reduced. The designer's goal, therefore, is to ensure that any variation in the transfer time of the traffic at the switch fabric is minimized. The ATM forum also recommends that the cell transfer time variation is carefully evaluated (see [1]).

Current developments in the field of voice compression have resulted in a new adaptation class, the real-time variable bit rate (VBR-RT), which stipulates that the adaptation process must guarantee defined end-to-end delay-and-delay jitter. This protects up to 60% of the bandwidth which is normally wasted when other techniques, such as TDM, are used (see [2]).

To measure cell transfer time variation in a communication system interacting with ATM cells, the HP E4829B test system is able to log and extract time-stamp information flowing into and from the payload of ATM cells. This measurement can be made at parallel to parallel (UTOPIA) ports, either at the switch fabric ports or at the ATM layer device interfaces, as shown in figure 2.

Application

Network equipment manufacturers

For hardware and software engineers in the communications industry, designing ICs and modules for ATM switches, or working in system integration, the HP E4829B parallel cell / traffic generator and analyzer system, which can measure cell transfer time variation, is the basic tool for the evaluation of complex ATM designs at parallel interfaces (UTOPIA).

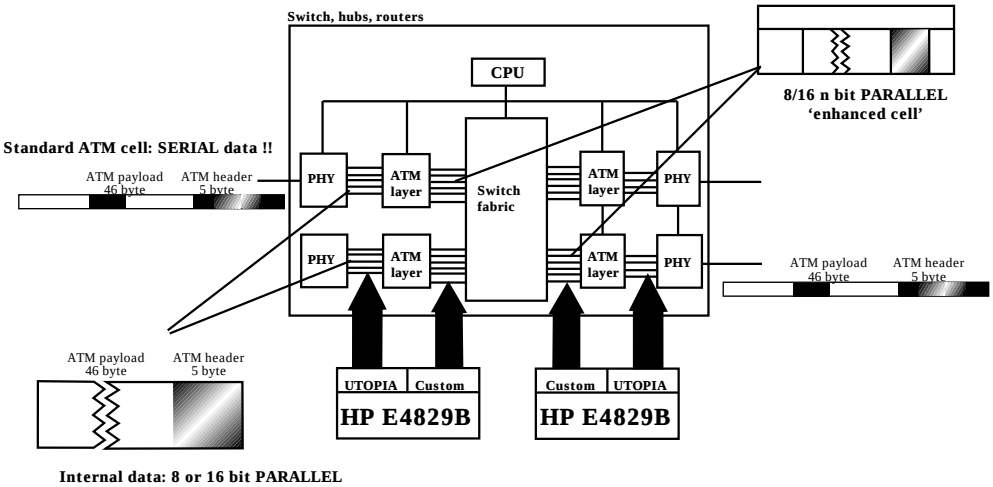

Figure 2: Block diagram showing how the HP E4829B connects to an ATM switch with parallel interfaces

Component Test

Semiconductor manufacturers provide a large variety of off-the-shelf devices for the ATM industry, including line interface ASICs, ATM layer controllers and chip and chip sets for the switch fabric itself.

In order to achieve high standards of quality throughout the system, the individual chip or chip set must have already been characterized for its share of the overall cell transfer time variation budget.

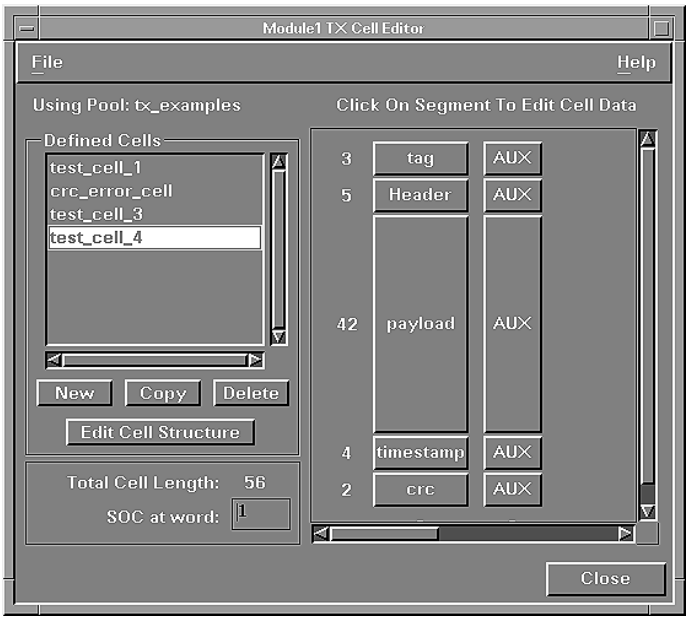

Figure 3: Cell editor of the HP E4829B showing a cell including a time-stamp segment

Instructions for use

Cell definition

The time-stamp is a segment available when the cell structure is defined. The length of the segment is fixed at 32 bits, which is equivalent to four bytes in an ATM-8 or two words in an ATM-16 application, and it can be placed anywhere within the payload of the cell. Figure 3 shows a cell including a time-stamp segment.

The definition of cells on the transmitter and receiver is identical. As soon as the cell is generated, the time-stamp segment, situated on the transmitter, is filled with bits generated by the time-stamp counter. On the receiver, it defines the bytes / words which are used for calculating the cell transfer time. The trigger cell can also be used to specify other parameters, such as the measurement of the transfer time of specific cells (e.g. matching cells for a dedicated VPI/VCI) within the incoming cell stream.

Analysis

The HP E4829B offers a new feature called 'measure time,' which actually performs the cell transfer time variation measurement. The receiver is forced to generate a time-stamp when the cell arrives, which is then compared with the time-stamp extracted from the cell's payload. From this, the transfer time is calculated. To guarantee the validity of these measurements, the transmitter and the receiver queue paths are compensated and the time-stamp counters are synchronized.

The received cells are sorted into three categories: early, in-time and late, although the user has to provide the values for both limits. Figure 4 illustrates the principle of the system, whereas figure 5 shows the setup in the processing editor window.

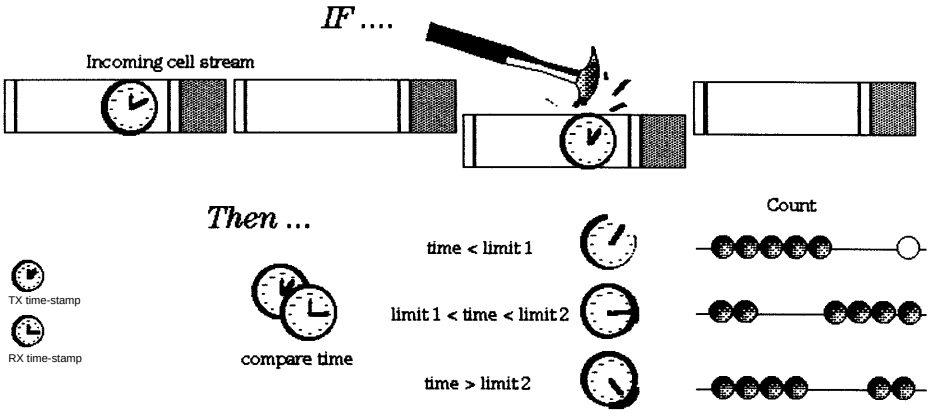

Figure 4: Principle of cell transfer time measurement

Results

The counter window, illustrated in figure 6, displays the results of a cell transfer time variation measurement. There are three counters, each assigned to one of the three categories (early, in-time and late), which display the number of cells generated according to specific limits. Once the receiver has started, the counter window is updated in specific measurement intervals, as defined by the user.

Implementation

Cell transfer time variation measurements can be performed on the 8 and the 16 bit solution of the HP E4829B, which is equipped with the necessary features (including software revision A.2.3.0) to carry out these measurements.

Time-stamp segment

- fixed length of 32 bits:
  ATM-8 = 4 bytes,
  ATM-16 = 2 words.
- can be placed anywhere in the payload of a cell, but not after a CRC-10 segment.
- maximum one segment / cell.

Time-stamp analysis

- action: compare time.
- conditions:
  early (< limit 1),
  in-time (> limit 1 < limit 2),
  late (> limit 2).
- upper and lower limit
  (limit 1, limit 2):
  range: 0 to 40 seconds,
  resolution: 20 ns.
- both limits can be programmed to the same value.

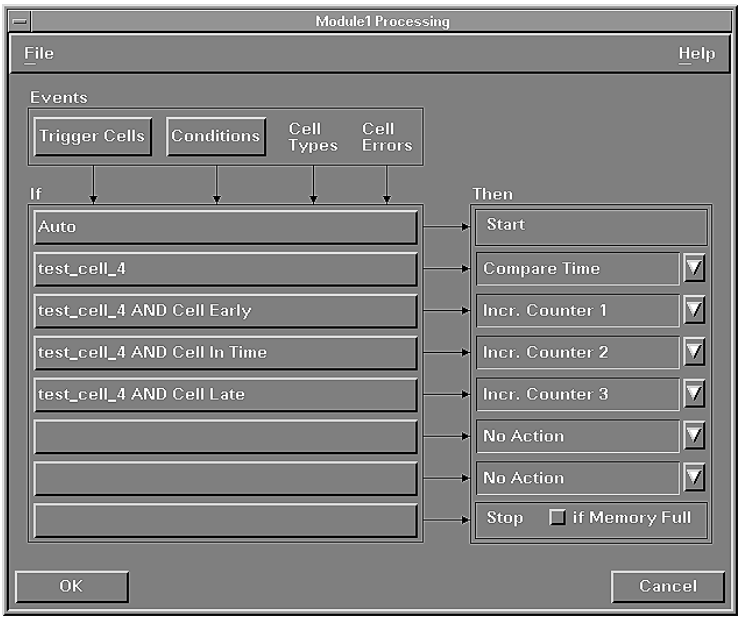

Figure 5: Processing editor window

Synchronization

Before starting a measurement, the time-stamp generators of the transmitter and receiver need to be synchronized. This is achieved by using the 'sync' command for the TX and RX with one module. However, for a system containing more than one module, the 'sync' is distributed via the VXI trigger lines on the VXI back plane. It is also possible to select a trigger line for each module.

External clock

Any external clock can be used for the TX or RX. However, to achieve the highest measurement accuracy, the system software uses the given value for the

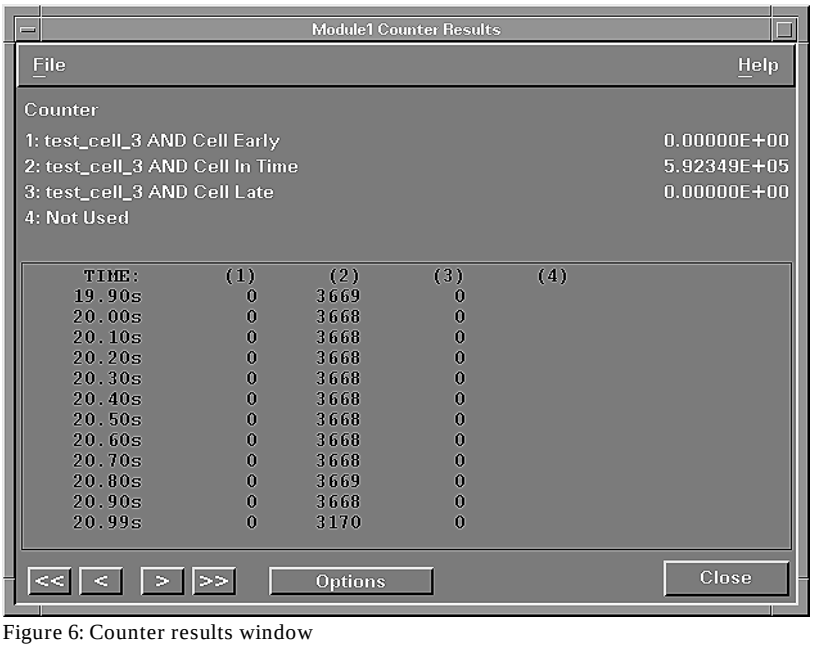

Figure 6: Counter results window

applied frequency in the 'timing / interface' editor window to compensate internal pipeline delays.

Exit and entry event time

According to the ITU recommendation (see [3]), the exit event time is measured when the first byte / word of a cell is transmitted at the outputs of the transmitter POD. The entry event time occurs when the last byte / word of a cell is received at the inputs of the receiver POD. Consequently, a transfer time measurement for a cell on an infinitesimally short media produces a value which is equivalent to the length of the cell. Therefore, internal path delays of the HP E4829B are compensated accordingly. If the handshake conditions avoid a cell transmission, the cell is buffered to the output queues. The length of time from the possible exit to the real exit event is added to the cell transfer time using a DUT.

References

[1] ATM Forum, Introduction to ATM Forum Test Specifications, af-test-0022.00, Dec. 94.

[2] TELECOMMUNICATIONS, International Edition, Jul. 96, Voice over ATM - A Winning Technology, page 49.

[3] ITU-T Recommendation I.353, Chapter 2, General Definitions.

Related HP literature

- real-time bit error rate analysis at parallel interfaces (UTOPIA) with the HP E4829B, product note, p/n 5965-4855E.
- UTOPIA Level 2 support, product note, p/n 5965-4856E.

For more information:
http://www-europe.hp.com/dvt

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