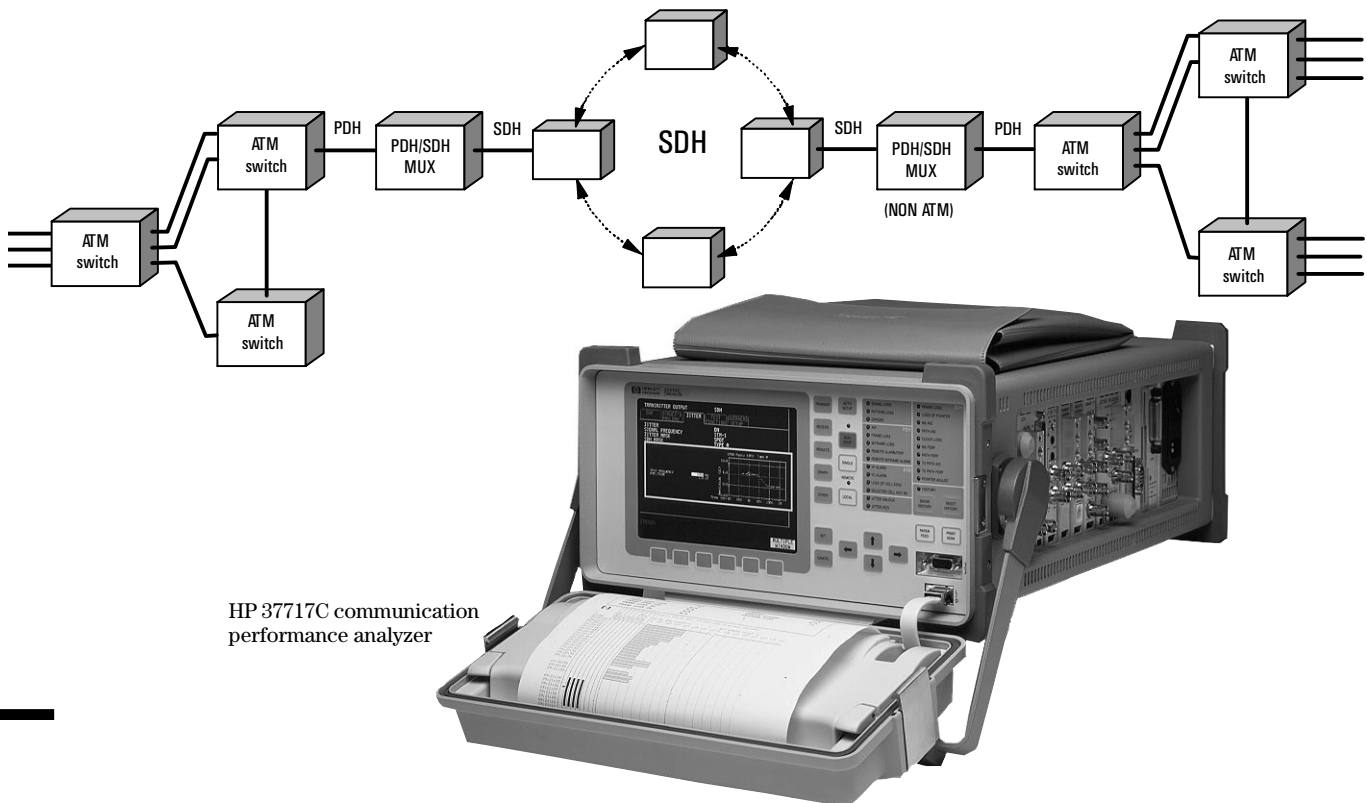# Physical layer jitter testing in an ATM environment

HP 37717B/C communications performance analyzer

HP 37717C communication performance analyzer

It is often assumed that all the problems associated with ATM lie at or above the ATM layer. This is not always the case. For example, in today's multi-technology transmission network, ATM cells are often carried in PDH circuits which, in turn, are transported over an SDH or SONET network. In such situations, physical layer jitter can occur on the ATM bearing PDH signal and if ATM network equipment is not tolerant to this jitter, problems will occur at the ATM layer and above.

This product note discusses the nature of these problems and describes a method for testing an ATM network element's susceptability to physical layer jitter.

Measuring jitter tolerance of ATM network elements

Introduction

The physical layer jitter present in ATM traffic arriving from a SONET or SDH network element (NE) results from two primary sources:

- The "bit-stuff justification" process which is performed when a plesiochronous signal is mapped into the synchronous transport signal.

- Pointer adjustments which compensate for asynchronous operation between different nodes within the SONET/SDH network.

The effect of jitter at an interface not sufficiently tolerant to this type of degradation is to introduce bit errors into the signal. Depending on where these bit errors occur in the signal can affect the type of error exhibited. For example,

- Bit errors introduced into the PDH frame overhead may, if excessive, cause loss of frame with the consequential loss of the ATM cell stream.

- Bit errors which impact the header of a cell may cause loss of the cell (if the error is uncorrectable) or cause the header to be corrupted into another "correct" or "correct-able" header value; if another virtual connection exists in which this corrupted cell's VPI-VCI is valid, then the cell becomes misinserted in that connection.

- Bit errors which occur in the cell payload will have higher layer effects. Depending on the ATM adaptation layer (AAL) in use, these errors are detected at the AAL or at higher layers. Retransmission of data may result, adding to the probability of network congestion.

Testing methodology

There are established methods for measuring bit errors in PDH or SDH networks. Bit error testing is used to derive a bit error ratio (BER) which provides an indication of transmission quality. In addition, bit error checks, for example bit-interleaved-parity

(BIP) checks, are used to alert network management to transmission problems. However, because ATM switches and multiplexers always terminate the physical layer while extracting ATM cells, measuring bit errors directly is not possible.

The solution is to measure jitter tolerance indirectly. This involves generating an appropriate ATM signal into a previously configured ATM virtual connection in the system-under-test, then observing the ATM impairments that result when physical layer jitter is added to the ATM test signal.

The kinds of impairment that can be anticipated are loss of cell, errored cells (defined as cells containing any payload errors) and loss of frame (although this has a lower probability since framing is usually tolerant of bit errors).

Note that correctable header errors are only detected and corrected by the NE itself and

Figure 1. Set-up for measuring jitter tolerance of an ATM network element
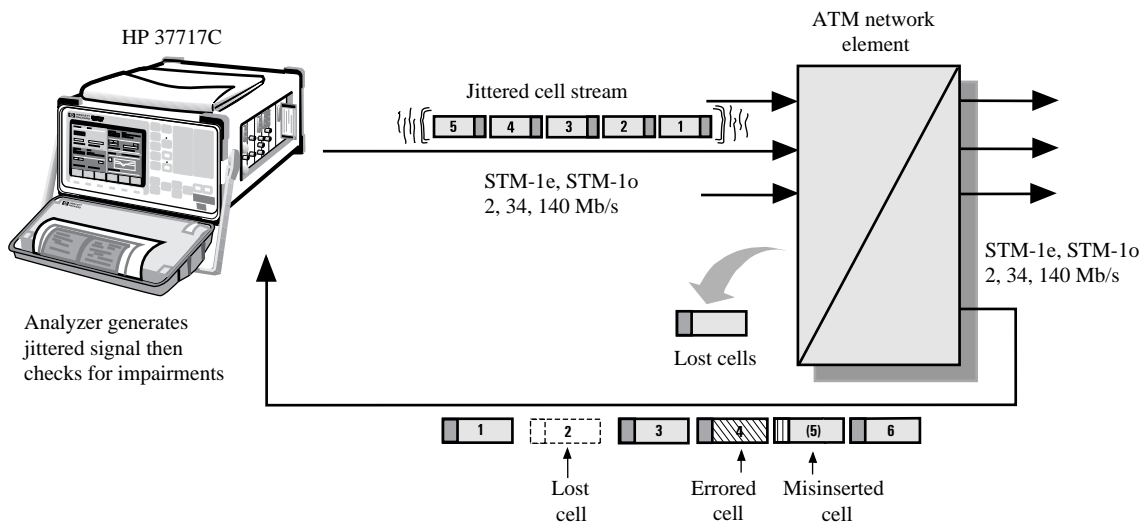
therefore can't be observed externally. Uncorrectable header errors are discarded by the NE so are viewed externally as cell loss in the test channel.

Occassionally, headers that are excessively corrupted may pass the header error control (HEC) check when the VPI-VCI field is corrupt. This can happen due to corruptions also occuring in the HEC field. Cells associated with such headers are lost from the test channel but could be inserted in any existing channel with the same VPI-VCI. The probability of this misinsertion occuring is related to the number of other channels present and to the Hamming distance of the header involved.

Practical testing

Unlike other ATM analyzers, the HP 37717B/C communications performance analyzer has the capability to add jitter to its internally generated ATM test source. This allows ATM and physical layer jitter to be tested simultaneously. Jitter can be generated and analyzed to ITU-T O.171, G.823, G.825 and G.958 standards.

For ATM, the analyzer generates and analyzes test cells to ITU-T O.191. This provides the means for detecting cell loss and cell errors; the LOF alarm can also be identified.

Detecting these error modes has, in the past, meant manual tracking. The HP 37717B/C communications performance analyzer, however, has an automatic jitter tolerance facility that allows an interface to be checked against a tolerance mask.
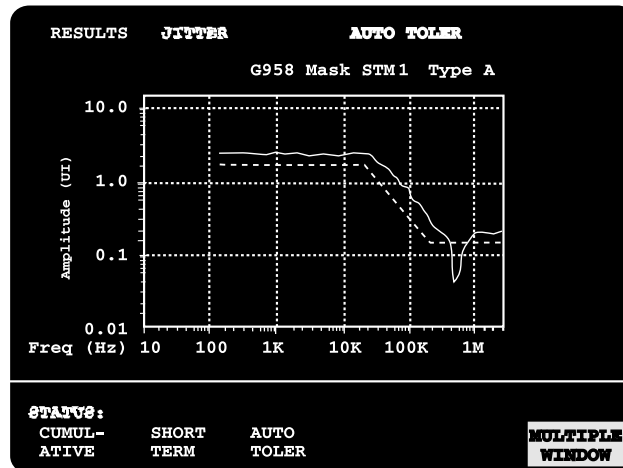

Figure 2. Comparing an ATM NEs tolerance to jitter to an ITU-T standard.

To establish the tolerance of an ATM NE, the analyzer generates jitter at different frequencies and at each frequency gradually increases the amplitude of the jitter is until an error event occurs. A point is plotted on the tolerance graph corresponding to the jitter amplitude and frequency at which the event occured. Once all points on the mask are plotted, an easy-to-interpret graphical representation of jitter tolerance is displayed (see figure 2).

In detecting these error and alarm events, the analyzer applies its "TroubleScan" feature. In this mode, the analyzer systematically searches for appropriate detectable errors or alarms caused by the generated jitter, including those associated with ATM.

Performing the analysis

1. Configure the equipment as shown in figure 1.
2. Set up a virtual channel connection or virtual path connection through the system-under-test (SUT).
3. Configure the HP 37717B/C communications performance analyzer to generate test cells at full rate on the virtual connection already set up in the SUT.

4. Configure the analyzer to analyze the test cells received from the SUT (the VPI-VCI may be different).
5. Select the JITTER folder in the TRANSMIT screen and choose AUTO TOLERNCE; press RUN/STOP and observe the auto-tolerance graph plot.

Printing your results

Connecting an external printer or using the HP 37717C's graphics printer allows you to log the jitter auto tolerance plot. This is easily accomplished by enabling logging and viewing the jitter tolerance plot in the results screen, then pressing the print key.

Instrument configuration

The HP 37717B/C communications performance analyzer must be configured to include an ATM cell layer option and a jitter generator option. Additional options may include SDH/SONET and optical options (for ATM at 155 Mb/s), a jitter analyzer option and a broadband auxiliary/services option. For further information, refer to the HP 37717C configuration guide publication number 5964-1662E.

HP 37717B/C communications performance analyzer

Offers a modular, upgradeable one-box solution for installation, commissioning, and field maintenance. This rugged, portable tester allows comprehensive functional testing of SDH, PDH and ATM equipment including jitter generation and test. The HP 37717C has a color display and

HP 37717B communications performance analyzer

graphics printer, with the HP 37717B monochrome version providing a budget solution, and a 20-column printer. Both instruments include a 3.5-inch disk drive to ease results retrieval, test firmware upgrades, and analysis.

Related literature

- HP 37717B/C generic brochure, 5964-0106E

- HP 37717B/C jitter brochure, 5965-5618E

- HP 37717B/C ATM brochure, 5965-4968E

- HP 37717C photocard, ATM testing and LAN connectivity measurements under one handle, 5965-1259E

- HP 37717B/C technical specifications, 5964-2255E

- HP 37717B configuration guide, 5965-5764E

- HP 37717C configuration guide, 5965-5621E

- HP 37717B/C product note: Tributary jitter testing of SDH network equipment using ITU-T G.783 pointer sequences, 5965-4862E

- HP 37717B/C product note: Automatic verification of network equipment to ITU-T jitter tolerance recommendations, 5965-4863E