Implementation of UTOPIA Level 2 for Parallel Cell / Traffic Generator and Analyzer

How to use the HP E4829B with UTOPIA Level 2 implementation

Product Note

Product Number
HP E4829B

Figure 1: HP E4829B entry system

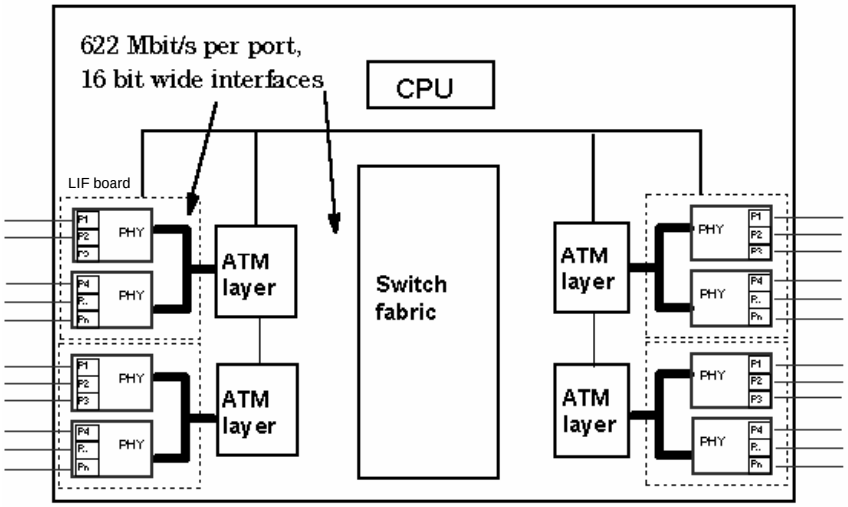

Figure 2: Block diagram of an ATM switch showing the HP E4829B connecting to parallel interfaces

Introduction

The latest design of ATM layer devices and ATM switches allows a bandwidth of up to 622 Mbit/s per port. However, typical line rates in ATM backbones are still in the range of 25 to 155 Mbit/s. In order to allow multiple physical interfaces to connect to one ATM layer, the ATM forum defined the UTOPIA Level 2 MultiPHY standard. Not only does higher integration lead to lower costs, but there is also a greater bandwidth.

Application

In “UTOPIA, an ATM-PHY Interface Specification, Level 2” [1], the ATM forum released the specification for multiple interfaces (MultiPHY). The various interfaces are described in chapters 4.2, 4.3, and in the appendix of the ATM forum’s UTOPIA Level 2 specification. The most important modes are: single Clav polling (chapter 4.2) and direct status indication (chapter 4.3).

The MultiPHY interface usually occurs between PHY devices/line interface cards (LIFs) and the ATM layer device. PHY/LIFs host one or multiple ports with typical line rates ranging from 1.5 to 155 Mbit/s. The ATM layer itself typically handles 622 Mbit/s.

Following the industry’s trends, the HP E4829B supports UTOPIA Level 2 according to chapters 4.2 and 4.3, with the PODs HP E4885A/ E4886A handling the UTOPIA Level 2 handshake and signaling.

Existing HP E482xA/B systems can be upgraded by adding new software and PODs. UTOPIA Level 2 is supported from software revision A.2.4, which detects which interfaces are connected and automatically adapts the system software so that it functions properly. UTOPIA Level 1 and custom interfaces are supported by HP E4889A PODs. It is possible to mix operating modes in a system which has more than one module. Table 1 summarizes which interfaces support the UTOPIA specification. It is not possible to mix Level 1/ Level 2 operation within one module.

With UTOPIA Level 2, the test system emulates the ATM layer device as well as one or multiple physical ports (PHY device or LIF board). It handles the address polling and port selection for up to 31 physical ports in single Clav polling mode (chapter 4.2) and up to four static Clav signals in direct status indication mode (chapter 4.3). Individual traffic rates per port can be emulated. The interface is 8/16 bit wide, running at a clock speed of up to 50 MHz (equivalent to 400/800 Mbit/s). In this description, the following terminology is used:

- TX ATM: transmits data to the PHY layer.
- TX PHY: receives data from the ATM layer.
- RX PHY: transmits data to the ATM layer.
- RX ATM: receives data from the PHY layer.

ATM layer emulation

The system replaces the TX ATM and the RX ATM, as indicated in figure 3. The emulation of the TX ATM is performed by the TX POD (HP E4885A), whereas for the emulation of the RX ATM, the RX POD (HP E4886A) is used. Both PODs generate the address signals normally provided by the ATM layer device.

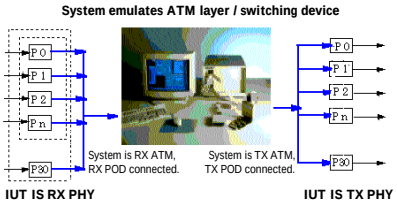

Figure 3: ATM layer emulation

PHY device emulation

The system replaces the RX PHY and the TX PHY, as indicated in figure 4. The emulation of the RX PHY is performed by the TX POD (HP E4885A), whereas the TX PHY is emulated with the RX POD (HP E4886A). Both PODs are capable of detecting addresses, a function normally performed by the PHY layer device. In order to bring up and debug boards, the system can also emulate single missing PHY devices on the test board.

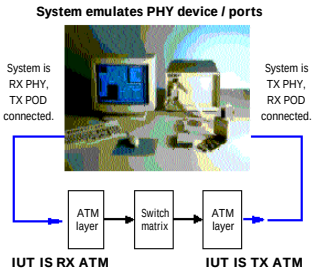

Figure 4: PHY device emulation

Compatibility

The functional verification of ATM designs can be carried out by a UTOPIA Level 1-compliant system. The compatibility between UTOPIA Level 1 and Level 2 allows Level 2 interfaces to be interconnected and act as a single port. However, this only permits functional verification.

In the same way, a Level 1-compliant device can be fully tested by a Level 2 solution (in direct status indication mode). The system can be set up to deal with only one port to ensure that Clav signals which have not been used are de-asserted.

Polling and selection

As described in chapter 4.2 of the UTOPIA Level 2 specification, the different MPHY ports must be polled during one cell transfer cycle. Two clock cycles are needed for the ATM layer to poll the status of one MPHY port. If the cell size is 27 words/53 bytes, typically 13/26 different ports can be polled during one cell transfer (in the 16/8 bit mode).

The HP E4829B supports any combination of ports to be active. The active ports are always polled in ascending order. The port address can be selected from the complete five bit address range (0 to 31).

Specification	Level 1	Level 2, chapter 4.2	Level 2, chapter 4.3
Terminology	single PHY	MPHY, single Clav polling	MPHY, direct status indication
Number of ports	1	1 to 31	1 to 4
Number of Clav signals	1	1	1 to 4
Priority	required	required	optional
Interface	HP E4889A (TX)	HP E4885A (TX)	HP E4886A (RX)

Table 1: UTOPIA specification and interfacing of the HP E4829B

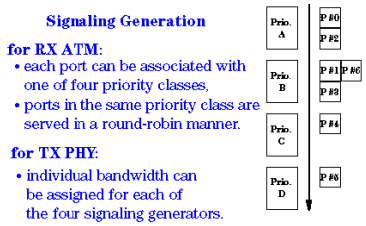

Figure 5: Signaling generation for a system using the RX POD

Depending on the polling results, the HP E4829B (ATM layer) has to decide which port to serve first. Together with the TX POD (HP E4885A), the system provides an individual cell sequence for each port which is defined from one of the four prioritized traffic generators according to the parameters T_{cell} and T_{pause}.

Clav signaling

Together with the RX POD (HP E4886A), the system offers four priority encoded signaling generators. Any port can be flexibly assigned to any one of them. For the RX ATM, the signaling generators are priority encoded. The higher priority ports are served first, while ports within the same priority class are served in a weighted round-robin manner.

In the case of the TX PHY, for each of the signaling generators, a bandwidth equivalent to the expected traffic rate is specified. The parameter is T_{cell}, similar to the traffic generation at the transmitter.

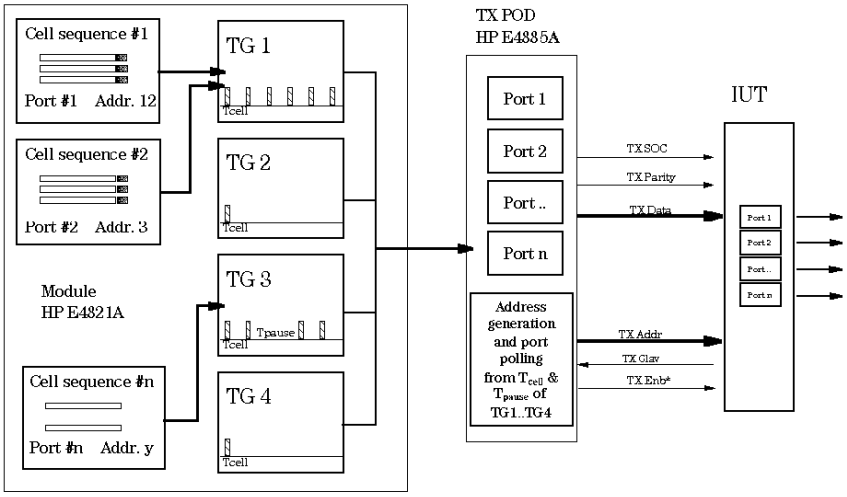

Figure 6: ATM layer emulation: system is TX ATM, TX POD (HP E4885A) is connected

ATM Layer Emulation

Test case TX ATM

The system emulates the ATM layer and sends traffic to a MultiPHY device (IUT). Therefore, the TX POD (HP E4885A) is connected to the IUT as shown in figure 6.

Step 1:
For each individual port, a dedicated cell sequence is set up. The sequence may contain any kind of cells. A cell is built in a flexible manner from single memory-based and real-time generated data segments (see [2] and [3]). The physical port number is linked to each cell sequence.

Step 2:
One of the four traffic generators must be linked to a traffic sequence. The traffic generator shapes the cell streams and passes the cells over to the POD ports (cell buffers). Traffic generator #1 has the highest priority, whereas traffic generator #4, the lowest.

Step 3:
The POD carries out polling as defined by the traffic profile resulting from all the traffic generators together. Depending on the polling result, the POD will transfer the appropriate cell to the UTOPIA interface. If more than one port signals acceptance of a cell, the port with the lowest address will be served first.

If an IUT port does not accept cells, the cells coming from the traffic generator may overflow the POD port buffer (which has a depth of three cells). In this case, the cell from the traffic generator will be discarded until the IUT accepts further cells and frees up the POD port buffer. The discarding of cells is ongoing, which is indicated by the system's monitor screen.

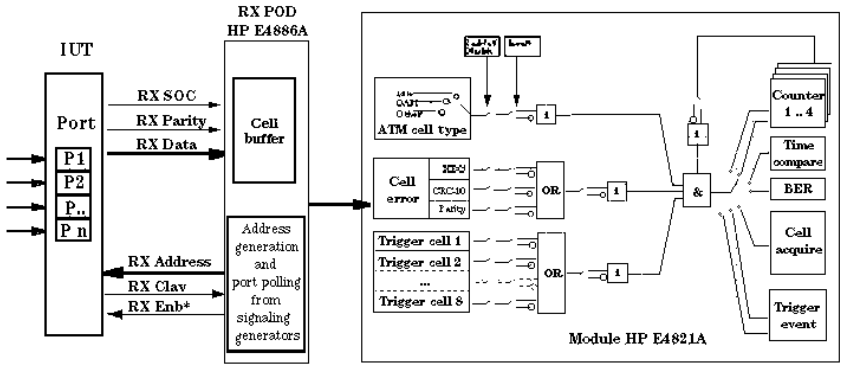

Figure 7: ATM layer emulation: system is RX ATM, RX POD (HP E4886A) is connected

Test case RX ATM
The HP E4829B emulates the ATM layer and receives data from a MultiPHY device (IUT). The RX POD (HP E4886A) is connected to the IUT as shown in figure 7.

Step 1:
The POD handles the polling (address generation) in ascending order for all activated ports. When several ports signal cell availability, selection of a certain port takes place according to the assigned priority. The higher priority ports are served first, while ports within the same priority class are served in a weighted round-robin manner.

Step 2:
Available cells are received from the IUT and are marked with port information. The POD transfers the cells immediately to the module, where cells are analyzed and processed in the same way as with Level 1 implementation (see [3]). The trigger masks are enhanced and allow the specification of a physical port number, together with the cell data itself.

Step 3:
Typically, the system acts as an ideal ATM layer which never delays any cells from transferring. Therefore, a bandwidth of 100 % is always provided. The absolute bandwidth is defined only by the receiver clock.

PHY Device Emulation

Test case RX PHY
The system emulates a MultiPHY device and sends traffic to an ATM layer device. The TX POD (HP E4885A) is connected to the IUT as shown in figure 8.

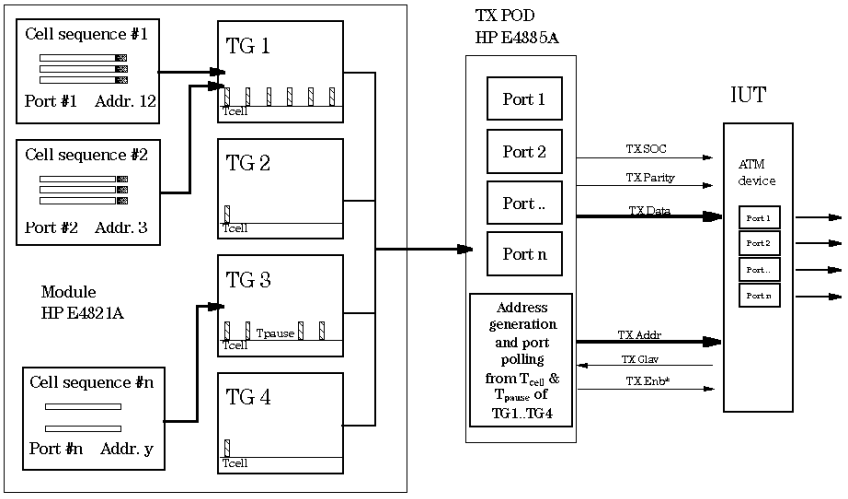

Figure 8: PHY device emulation: system is RX PHY, TX POD (HP E4885A) is connected

Step 1:
For each individual port, a dedicated cell sequence is set up. The sequence may contain any kind of cells. The physical port number is linked to each cell sequence.

Step 2:
One of the four traffic generators must be linked to a traffic sequence. The traffic generator shapes the cell streams and passes the cells over to the POD ports (cell buffers). Traffic generator #1 has the highest priority, whereas traffic generator #4, the lowest.

Step 3:
A POD port can buffer three cells. The POD monitors the address bus, and signals available cells (RXClav) according to the parameters T_{cell} and T_{pause} when cells are in buffer. If more than one port signals acceptance of a cell, the one with the lowest address will be served first.

Cells transferred by the traffic generator without request from the IUT (ATM layer) are discarded. The discarding of cells is indicated by the system's monitor screen.

Test case TX PHY
The HP E4829B emulates the MultiPHY device and receives data from an ATM layer device (IUT). The RX POD (HP E4886A) is connected to the IUT as shown in figure 9.

Step 1:
To activate a port, the TX POD is assigned to one of the four signaling generators. For each generator, an individual bandwidth representing expected traffic can be specified. The bandwidth specification defines the maximum traffic which the test system can serve for the corresponding port.

Step 2:
The POD monitors the address bus. With the TXClav asserted, the POD signals cell transfer into its buffer. After a cell transfer to a certain port is completed, the TXClav for this port will not be asserted again until the actual data rate is lower than the specified bandwidth. The system acts as an ideal PHY device which never discards any cells from transfer.

Step 3:
The POD immediately transfers the cells, including the port information, to the module, where cells are analyzed and processed in the same way as with UTOPIA Level 1 implementation.

The trigger masks are enhanced and allow the specification of a physical port number, together with the cell data itself.

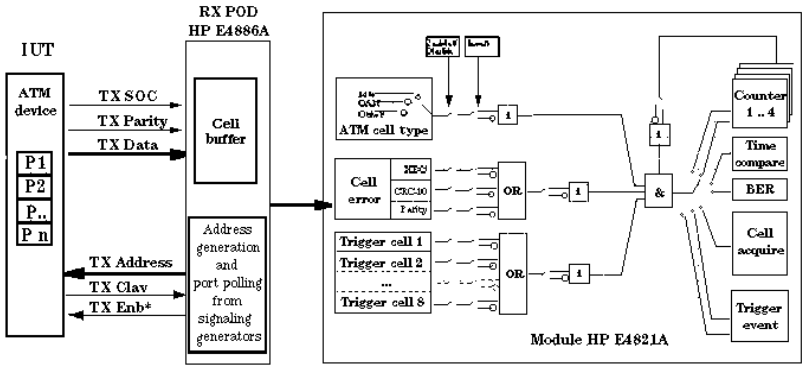

Figure 9: PHY device emulation: system is TX PHY, RX POD (HP E4886A) is connected

Software

Configuration

The system software adapts automatically according to the PODs connected. Figure 10 shows the configuration screen for configuring a UTOPIA Level 2 operation after a system boot.

Either 8 or 16 bit wide operation is available for the module. The TX and RX PODs can be individually assigned for either ATM or PHY emulation. Both can be selected individually for single Clav (chapter 4.2) or direct status (chapter 4.3) modes.

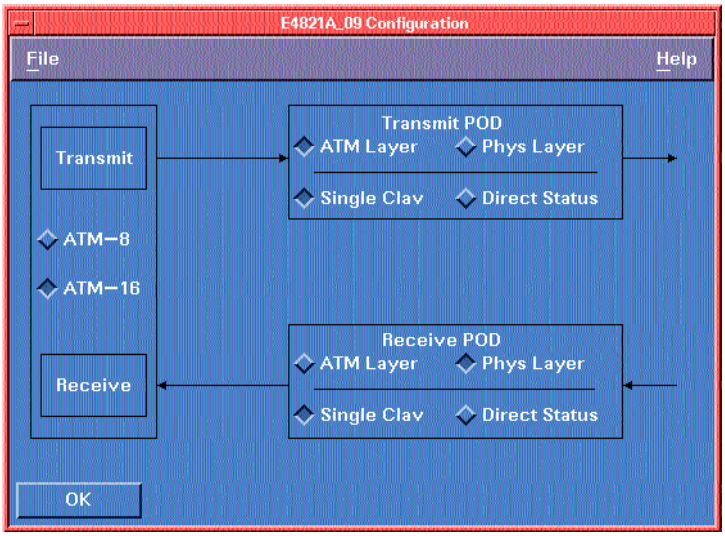

Figure 10: Configuration screen

Traffic generation

Traffic generators are capable of handling more than one sequence of cells. A sequence of cells can be assigned for each port. Figure 11 shows the screen for traffic editing.

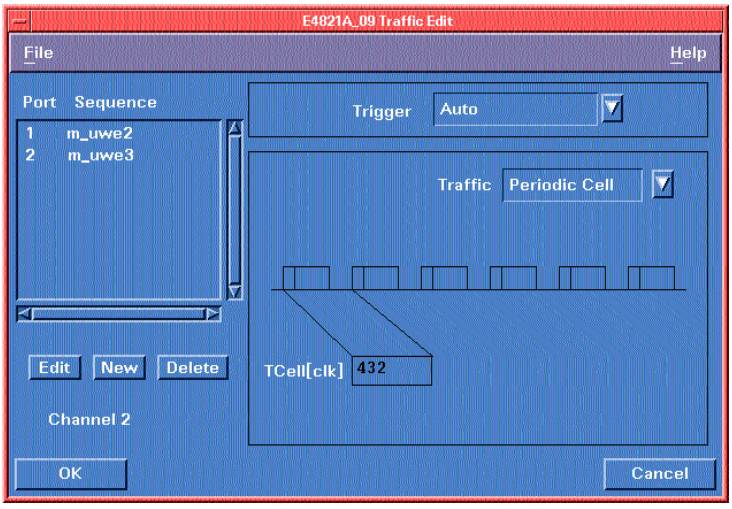

Figure 11: Traffic generation setup with port and sequence control

Clav signaling

Figure 12 shows the screen for a setup with the Clav signaling for a TX PHY. There are four individual signaling generators, and a bandwidth in terms of expected cell rate can be specified for each one by the parameter T_{cell}.

A port becomes active by assigning it to one of the four signaling generators.

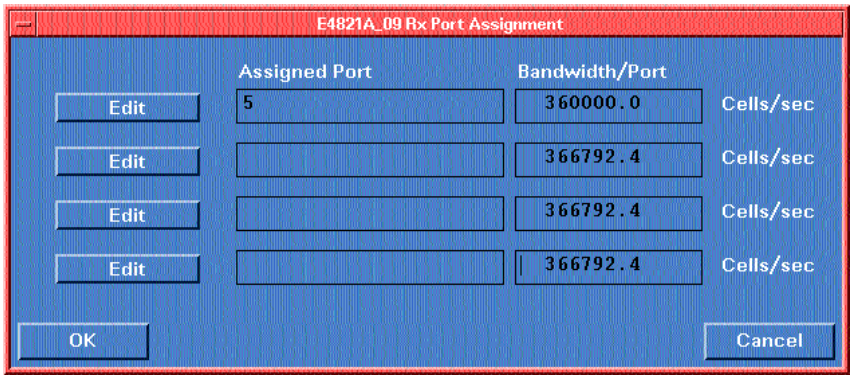

Figure 12: Signaling generator port and expected traffic control

Monitor screen

The system's monitor screen is shown in figure 13. It provides graphical feedback on the status of transmitter ports. Any non-active port is marked gray. As long as an active port is able to transmit cells, it is shown in green; as soon as cells have to be discarded, it is shown in red. There are two indications: one is called "Current", which gives an indication of the current status, and the other is called "Overall", which retains the status from the last click on the "Reset" button.

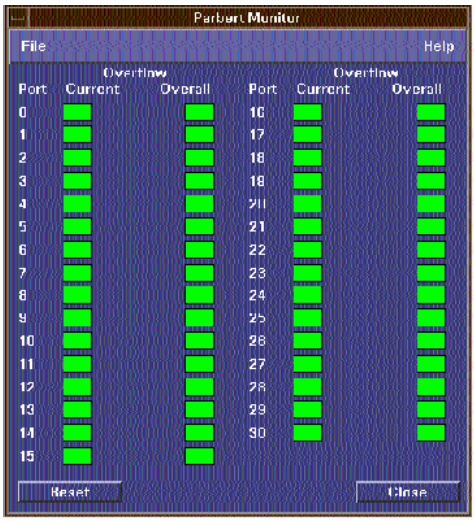

Figure 13: Monitor screen

Main window
The main window, shown in figure 14, is enhanced for:

- sequence edit: “Sequence”,
- port edit: “Port”,
- monitor: “Port”,
- connect status: “Disconnect/Connect”.

The monitor screen in figure 13 can be viewed by clicking on the “Port” button. The possible multiple sequences are edited from the “Sequence” button, and the port configuration for the receiver, including the signaling generators, is set up from the “Port” button in the receiver setup.

“Connect/Disconnect” are new keys which handle the connection status. In “Disconnect” mode, all system outputs are in a high impedance state. In “Connect” mode, all outputs are driven and the clock is applied to the device-under-test. The system will start cell generation and analysis after clicking on the “Run” button.

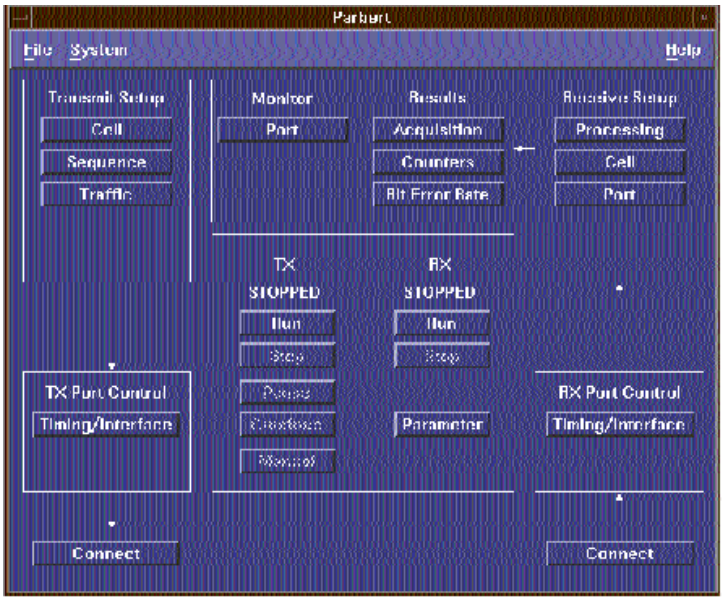

Figure 14: Main window

Interfacing

HP E4885A/E4886A

Figure 15 shows the TX/RX POD (interchangeable), together with a 120 mm 80 pin cable assembly and an adapter for reducing the signal density to 40 pin. The 80 pin cable belongs to the POD, whereas the adapter shown is part of the optional interface kit for Level 2 (HP E4821A option #502).

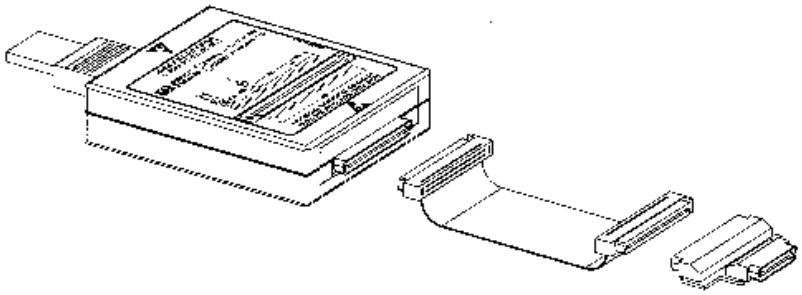

Figure 15: POD with an 80 pin connector, 120 mm ribbon cable and 40 pin adapter

There are several ways of connecting a POD to the IUT:

- connect the POD via the 80 pin test cable and connectors on the test board,
- connect the POD via the 80 pin test cable (PC-edge).

Used in conjunction with the interface kit, the following methods of connection are also possible:

- connect the POD via the 80 pin cable and the 80 to 40 pin adapter.
- connect the POD with the flexible lead cable by using the 80 to 2 x 50 pin adapter.
- connect the POD with 50 pin ribbon cables by using the 80 to 2 x 50 pin adapter.

POD connector

The POD connector pin layout is shown in figure 16 and is defined in table 2.

Pin #	Signal	Pin #	Signal
1	AUX0	3	AUX1
5	AUX2	7	AUX3
9	AUX4	11	AUX5
13	AUX6	15	AUX7
17	D0	19	D1
21	D2	23	D3
25	D4	27	D5
29	D6	31	D7
33	D8	35	D9
37	D10	39	D11
41	D12	43	D13
45	D14	47	D15
49	PRTY	51	SOC
53	LENB	55	A0
57	A1	59	A2
61	A3	63	A4
65	CLAV0	67	CLAV1
69	CLAV2	71	CLAV3
73	CLKIO	75	EXTREF
77	TRG_IN	79	TRG_OUT
all even	GND		

Table 2: Signals on an 80 pin connector

Note: all even pins carry Gnd.

Using connectors on the IUT test board

The 80 way cable plugs into the connectors provided on the test board. The following list includes connector part numbers and manufacturers for parts which can be used on a test board.

- 80 pin vertical plug
  e.g. AMP-2-557102-1.
- 80 pin right angled plug
  e.g. AMP-2-557100-1,
  MOLEX 71661-2080.
- 80 pin vertical plug for SMT
  e.g. MOLEX 71661-5080.

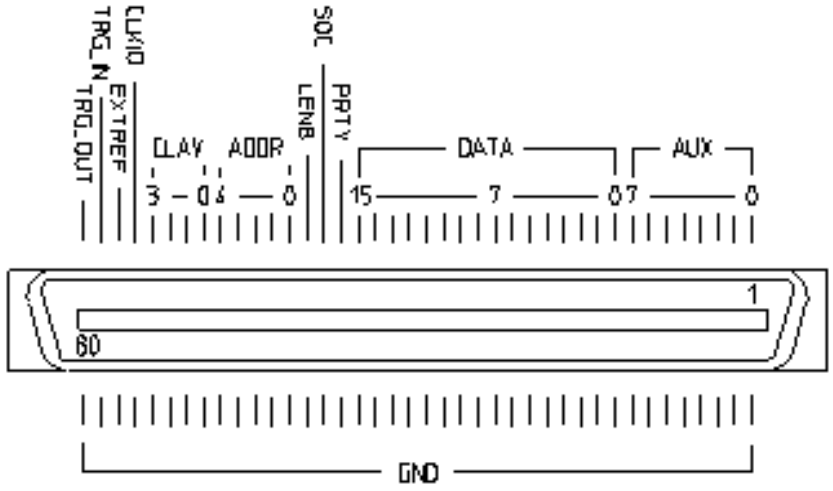

Figure 16: Signals at an 80 pin POD connector (HP E4885A/E4886A interchangeable)

PC-edge connection

This method allows a connection to the test board by a method similar to that of PC-edge connectors. It can therefore be performed without additional connectors, as long as the PC board layout is prepared, as shown in figure 15. The PC board thickness is 1.6 mm.

The layout requirements are outlined in figure 17.

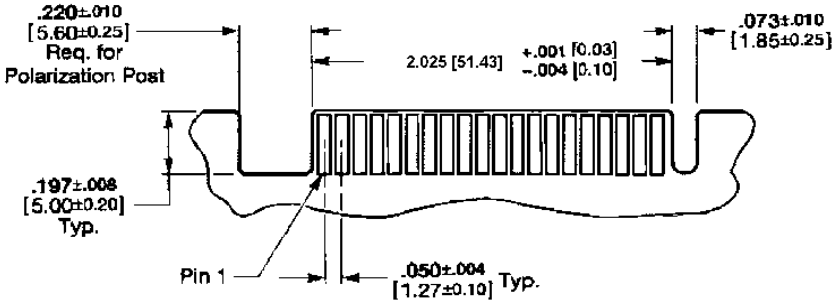

Figure 17: Layout details for a PC-edge connection with an 80 pin cable

Connection via 80 way cable and 80 to 40 pin adapter
Table 3 shows the signal assignment at the 40 pin adapter. The adapter is provided in both vertical and right angled versions.

Pin #	Signal	Pin #	Signal
1	GND	21	GND
2	AUX0	22	AUX1
3	AUX2	23	AUX3
4	D0	24	D1
5	D2	25	D3
6	D4	26	D5
7	D6	27	D7
8	D8	28	D9
9	D10	29	D11
10	D12	30	D13
11	D14	31	D15
12	PRTY	32	SOC
13	LENB	33	A0
14	A1	34	A2
15	A3	35	A4
16	CLAV0	36	CLAV1
17	CLAV2	37	CLAV3
18	CLKIO	38	EXTREF
19	TRG_IN	39	TRG_OUT
20	GND	40	GND

Table 3: Signal assignment of 80 to 40 pin adapters

The 40 pin adapter is a signal concentrator. It supports the smallest footprint on the test board by compromising the number of grounding pins. Therefore, it is recommended that you place the connector on the test board as close as possible (less than 2 inches) to the IUT.

The following list includes connector part numbers and manufacturers for parts which can be used on a test board when using the 40 pin adapter.

- 40 pin vertical plug
  e.g. AMP-557102-5.
- 40 pin right angled plug
  e.g. AMP-557100-5,
  MOLEX 71661-2040.
- 40 pin vertical plug for SMT
  e.g. MOLEX 71661-5040.

Flexible probes
The flexible lead cables available with the UTOPIA Level 1 interface kit are also usable for Level 2 interfacing. The Level 2 interface kit provides four flexible cables, together with two 80 to 2 x 50 way adapters for connection to both of the Level 2 PODs.

Ribbon cables
As well as the flexible cables, 50 pin ribbon cables are also provided. These can be used by standard 50 pin (IDC) headers in the 0.1 inch spacing included in the test board layout.

Electric characteristics
All POD signals, both in and out, are driven from FCT technology.

DC parameters for TTL levels are:
Ioh/Iol = 24 mA,
Iih/Iil = 1 µA.

AC impedance is typically a total of 50 pf when used with a 120 mm ribbon cable.

ESD protection is provided per MIL-STD-833.

Signal transition time is typically 1.5 ns. It is therefore highly recommended that you apply transmission line techniques to a test board layout in order to guarantee proper signal distribution over the custom design. Transmission line techniques keep the number of errors, which can cause significant overshoot and ringing due to fast edge rates, to a minimum. This also avoids coupling and noise between adjacent signals and other lines.

Signals View

Single Clav polling

(according to UTOPIA Level 2, chapter 4.2).

The figures on this page show the transmission of one cell from the ATM layer to the PHY layer. In this example, the test system's transmitter emulates the TX ATM, and the test system's receiver emulates the TX PHY. Three activated ports are shown in this example: 03, 07 and 0C.

Figure 18 shows the start of transmission. In the polling phase, all ports (03, 07 and 0C) signal their ability to receive a cell. Port 03 is then selected and transmission to this port begins (data = 0301, which indicates the first word of the cell transfer to port 03).

In figure 19, the cell transfer is paused at word #15. It is possible to set this up from the graphical user interface, where the start and length of the pause can be controlled. It can be seen that polling continues and that ports 07 and 0C still signal their ability to receive a cell.

In figure 20, the end of the cell transfer is shown. You might ask why the last word (0327) stays there longer; this is due to the high impedance of the bus. The data is only valid for the cycle after 0326; additional cycles are only required for discharging.

By controlling the bandwidth of the port emulated by the test system, port 03 signals that it is unable to take another cell at this moment. Ports 07 and 0C are still able to receive a cell, and so port 07 will be the next to be selected.

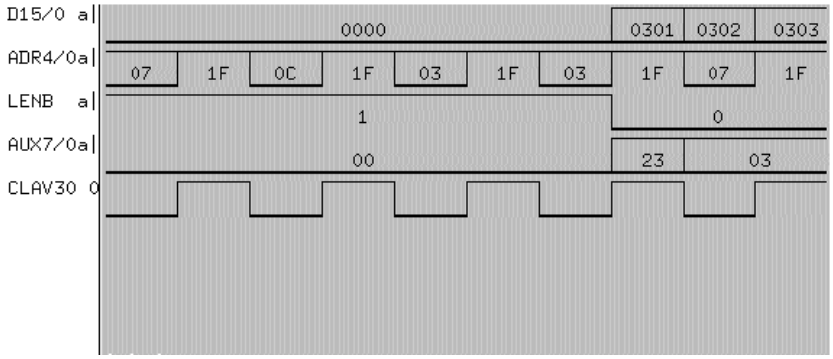

Figure 18: Polling, selection and start of transmission of a cell

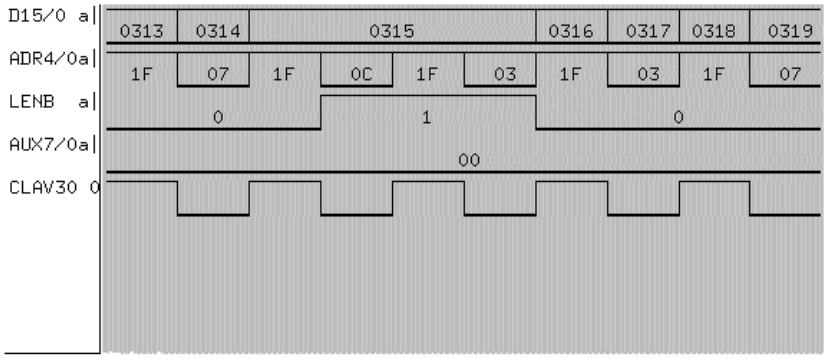

Figure 19: Transmission paused

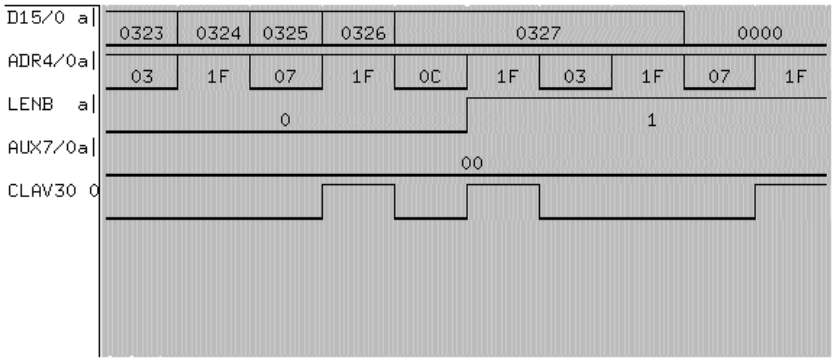

Figure 20: End of cell transmission

In case the HP E4829B (ATM layer) has to pause the data transmission because no data is available, polling is continued. On a first come first served basis, the HP E4829B will start cell transfer.

References

[1] ATM Forum, "UTOPIA, an ATM-PHY Interface Specification, Level 2", Version 1.0, 7/96.

[2] Parallel cell/traffic generator and analyzer HP E4829B, product overview, p/n 5964-1667E.

[3] Parallel cell/traffic generator and analyzer HP E4829B, technical specifications, p/n 5963-9923E.

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